A Novel Approach for Glitch and Leakage Power Reduction in CMOS VLSI Circuits

Ruchiyata singh, Atul S. M. Tripathi

***Abstract*— Now a days leakage power has become a major concern in nanometer CMOS technologies. Dynamic and leakage power both are the main contributors to the total power consumption. In the past, the dynamic power has dominated the total power dissipation of CMOS devices. However, with the continuous trend of technology scaling, leakage power is becoming a main contributor to power consumption. In this paper, a technique has been proposed which will reduce simultaneously both delay and leakage power. The results are simulated in Tanner Tool in 180nm, 130nm and 100nm Technologies.**

***Index Terms*— Dynamic power; Leakage power; Multi-threshold; Variable body biasing; Glitch.**

I. INTRODUCTION

Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power.

According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are several process technology and circuit-level solutions to reduce leakage in processors, in this paper a novel approaches for reducing both leakage and dynamic power with minimum possible area and delay tradeoff are proposed.

For the most recent CMOS feature sizes (e.g., 90nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. For deep-submicron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This to an extent reduces the dynamic (switching) power dissipation. However, the sub-threshold leakage current increases exponentially thereby increasing static power dissipation [1].

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18µ technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction. However, as the feature size shrinks, e.g., to

0.09µ and 0.065µ, static power has become a great challenge for current and future technologies.

Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology. Power consumption has two components: Dynamic Power and Leakage power [2]. Dynamic and leakage power both are the main contributors to the total power consumption. Dynamic power includes both switching power and short circuit power. Spurious transitions (also called glitches) in combinational CMOS logic are a well-known source of unnecessary power dissipation. Reducing glitch power is a highly desirable target [3]. The dynamic power cannot be eliminated completely, because it is caused by the computing activity. It can, however, be reduced by circuit design techniques.

Static power refers to the power dissipation which results from the current leakage produced by CMOS transistor parasitic. Traditionally static power has been overshadowed by dynamic power consumption, but as transistor sizes continue to shrink, static power may overtake dynamic power consumption. To alleviate the rising significance of static power in digital systems, static power reduction techniques have been developed like transistor stacking, dual threshold voltage , MTCMOS etc. Some of these techniques are state saving and some are state destructive techniques. For example: Sleep transistor is a state destructive technique. Despite the rising significance of static power in CMOS circuits, the dynamic power is still the major contributor to power consumption. Dynamic power is mostly consumed by glitches which are the unwanted transitions and need to be eliminated. Glitch and leakage power both are the main contributors to the power consumption and needs to be reduced

II. POWER DISSIPATION FACTORS

In CMOS, power consumption consists of leakage power and dynamic power Dynamic power includes both switching power and short circuit power. Switching power is consumed when the transistors are in active mode and short circuit power is consume when a pull-up and pull-down network are on turning on and off. For 0.18µ and above leakage power is small compared to dynamic power but 0.13µ and below leakage power is dominant. Dynamic power dissipation is proportional to the square of the

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supply voltage. In deep
sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation [4].

Static power dissipation is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The sub-threshold leakage current increases exponentially, thereby increasing static power dissipation.

The leakage current of a transistor is mainly the result of reverse biased PN junction leakage and Sub threshold leakage. Compared to the sub-threshold leakage, the reverse bias PN junction leakage can be ignored. The Sub-threshold conduction or the sub-threshold leakage or the sub-threshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage [5].

It is given by:

$$I_{sub} = I_{so} e[V_{gs}/V_t - {}_{th}/v_t][1-e^{V_{ds}/V_t}] \quad (1)$$

$$I_{S0} = \mu_0 C_{ox} (W_{eff}/L_{Eff}) \quad (2)$$

where μ_0 is the zero bias electron mobility, n is the sub-threshold slope coefficient, V_{gs} and V_{ds} are the gate to source voltage and drain-to-source voltage, respectively, V_T is the thermal voltage, V_{th} is the threshold voltage, C_{ox} is the oxide capacitance per unit area, and W_{eff} and L_{eff} are the effective channel width and length, respectively. Due to the exponential relation between V_{th} and I_{sub}, an increase in V_{th} sharply reduces the sub-threshold current.

A. Leakage Current Reduction

Reduction in threshold voltage results in the increase in sub-threshold leakage current. One of challenge with technology scaling is the rapid increase in sub-threshold leakage power due to V_t reduction. In such a system it becomes crucial to identify techniques to reduce this leakage power component. The development of digital integrated circuits is challenged by higher power consumption [6].

Leakage current is a primary concern for low-power, high-performance digital CMOS circuits. The exponential increase in the leakage component of the total chip power can be attributed to threshold voltage scaling, which is essential to maintain high performance in active mode, since supply voltages are scaled. Numerous design techniques have been proposed to reduce standby leakage in digital circuits. Leakage power has become a serious concern in nanometer CMOS technologies, and power-gating has shown to offer a viable solution to the problem with a small penalty in performance [7].

Devices which are operated on battery are either idle (Standby) or Active mode. Leakage power can be divided in to two categories based on these two modes [8].

1) Leakage Control in Standby Mode: Techniques like Power gating and super cutoff CMOS are used for leakage reduction in standby mode. In these techniques, circuit is cutoff from the supply rails, when it is in idle state.

2) Leakage Control in Active Mode: Techniques like forced stacking and sleepy stack can be used during the run time or active mode for leakage current reduction.

Leakage is becoming comparable to dynamic switching power with the continuous scaling down of CMOS technology. To reduce leakage power, many techniques have been proposed, including dual-Vth, multi-Vth, optimal standby input vector selection, transistor stacking, and body bias.

Multiple thresholds can be used to deal with the leakage problem in low-voltage high-performance CMOS circuits. The dual-V_{th} assignment is an efficient technique for decreasing leakage power. In this method, each cell in the standard cell library has two versions, low Vth and high Vth. Gates with low Vth are fast, but have high sub-threshold leakage, whereas gates with high Vth are slower but have much reduced sub-threshold leakage. The generation, distribution, and dissipation of power are at the forefront of current problems faced by the integrated circuit industry. The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity [9]. Already existing methods like stack, sleepy stack, and sleep transistor are shown in Fig. (1)-(3).

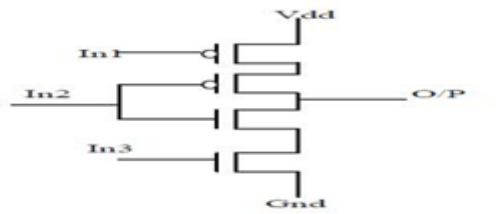


Figure (1) Sleep Transistor.

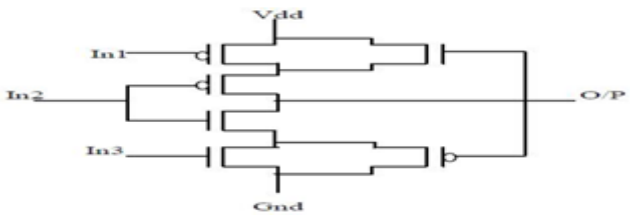


Figure (2). Sleepy Keeper

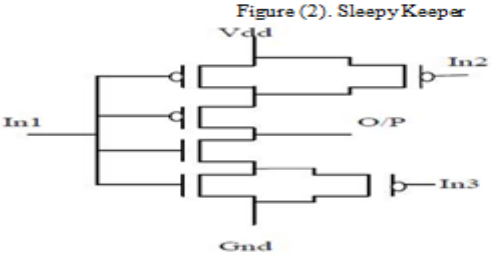


Figure (3).Sleepy Stack

Circuit optimization provides low power and high performance. Circuit optimization can be obtained through simultaneous gate sizing and threshold voltage (V_t) assignment [10,11]. The sleep transistors are turned off when the logic circuits are not in use. By isolating the logic networks using sleep transistors, the sleep transistor technique dramatically reduces leakage power during sleep mode. Sleep transistor method provides good reduction in leakage power, but it is a state destructive technique. It is shown in Fig.(1).

State -destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors. Both dynamic and leakage power reductions can be achieved through threshold voltage adjustment [12]. Sleepy keeper technique shown in Fig.(2) uses the traditional sleep transistors with two additional transistors to save state during sleep mode. Dual threshold voltages can also be applied in the sleepy keeper approach to reduce sub threshold leakage current [13].The sleepy stack approach combines the sleep and stack approaches. The stack approach uses a stack effect by breaking down an existing transistor into two half size transistors [14, 15, 16]. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. Fig.(3) shows its structure.

B. CMOS Glitch Elimination

One of the major factors contributing to the power dissipation in CMOS digital circuits is the switching activity. Dynamic power comprises of two parts: Logic switching power and glitch power. Whenever a logic gate changes state, power is consumed. The state change can be due to the essential logic value changes as well as due to glitches. Every signal transition consumes a finite amount of energy. For the correct functioning of a logic circuit, every signal needs to transition at most one time in one clock cycle. But in reality, the gate outputs transition more than once and these unnecessary transitions are called glitches. These transitions consume energy and are quite unnecessary for the correct functioning of the circuit.

Because switching power consumed by the gate is directly proportional to the number of output transitions, glitches reportedly account for 20%–70% dynamic power. Delay elements are components inserted into a digital circuit that do not alter the signal value, but deliver the same waveform at the output with some extra delay. Different delay elements can be used to insert delay at the inputs of gate. By inserting these delay elements glitches can be eliminated. A buffer is the simplest of the delay elements. Insertion of the buffer as the delay element is one of the way to remove glitches or unwanted transitions. Buffer as delay elements are simple and reliable, but their problem is increased dynamic power. NMOS, Transmission Gate, Cascaded Inverters are some of the other delay elements.

A combinational circuit is minimum transient energy design, i.e., there is no glitch at the output of any gate, if the difference of the signal arrival times at every gate's inputs remains smaller than the inertial delay of the gate. Hazard filtering, when used alone for glitch elimination, can increase the overall input to output delay. Path balancing does not increase the delay but requires insertion of delay elements. A combination of the two procedures can give an optimum design.

III. PROPOSED MODEL

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift, where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit: Static and Dynamic Power. Static (Leakage) power: includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling.

Among these, sub-threshold leakage is the most prominent one. Dynamic power: Includes charging and discharging (switching) power and short circuit power. In Dynamic power, power consumption due to switching activity is more prominent. It can be concluded from the above discussion so far that glitch and leakage power both are the main contributors to the power consumption.

The existing leakage reduction techniques like sleep transistor, sleepy keeper, stack etc. are having the drawbacks like: increased delay, area etc. and the buffer used as delay elements for elimination of glitches also has the drawbacks of large area overhead and increases the number of transitions in the output. Therefore, in this section new approach has been proposed keeping in mind all the drawbacks mentioned above, which will simultaneously reduce both glitch and leakage power.

A novel technique has been proposed in this section, which will reduce both glitch and leakage power in CMOS VLSI circuits. The new technique is Sleep Variable body biasing with transmission gate. The circuit diagram of un-optimized circuit 1 and optimized circuit 1 is shown in the Fig.4-5.

This proposed design includes variable body biasing technique along with sleep insertion technique. Sleep transistors are crucial part in any low leakage power design. The source of one of the sleep transistor is connected to the body of other PMOS sleep transistor for having body biasing effect. So, leakage reduction in this technique occurs in two ways. Firstly, the sleep transistor effect and secondly, the variable body biasing effect. This technique uses aspect ratio W/L=3 for NMOS transistor and W/L=6 for PMOS transistor. Due to the minimum aspect ratio the sub-threshold current reduces.

Since the sources of the NMOS sleep transistor is connected to the body of PMOS transistor as shown in Fig. 5, the threshold voltage of the sleep transistors increases due to the body biasing effect during sleep mode. This increase of threshold voltage of the transistors reduces the leakage current. That's why the static power consumption also lowers.

The variable biasing will be useful in reducing leakage power.

Sleep transistor method provides good reduction in leakage power in idle mode, but it is a state destructive technique.

Stacking approach is also utilized here to some extent to retain the state in active mode. Variable body biasing will be useful in increasing threshold voltage to reduce leakage current.

A novel technique has been proposed in this section, which will reduce both glitch and leakage power in CMOS VLSI circuits. The new technique is Sleep Variable body biasing with transmission gate. The circuit diagram of optimized circuit 1 and optimized circuit 2 is shown in the Fig.4-5.

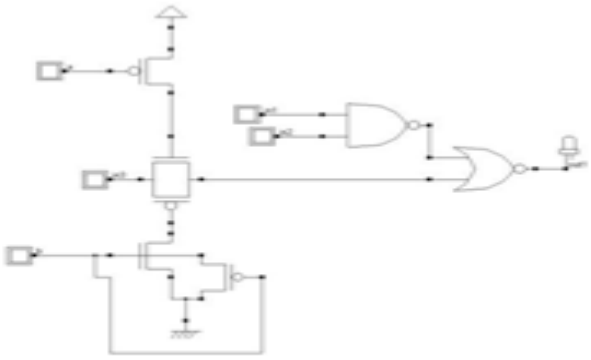


Figure (4).Optimized Circuit 1.

For the reduction of glitch power a transmission gate is also included. The transmission gate is used as a delay element for the elimination of the glitches. The transmission gate has a less area overhead as compared to other delay elements. The technique has been used on non-critical paths to reduce glitches.

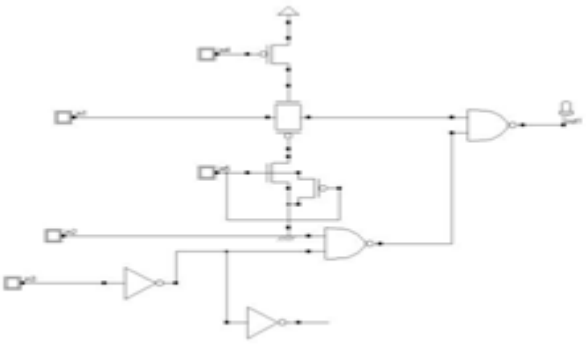


Figure (5).Optimized Circuit 2.

IV. RESULTS AND CONCLUSIONS

In this section, simulations of the proposed methods Comparisons between optimized circuit1 & optimized circuit2 are shown in tabular form. Simulations are obtained in Tanner Tool. First step in obtaining the simulations is to compile the Verilog file in T-spice V 14.1.

Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in T-spice V 14.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in W-Edit V 14.1. After that simulations are performed on the layout generated using Verilog files. The results are simulated at 180nm, 130nm and 100nm

Simulations of circuits given in Fig. 4-5 are shown below in Fig.6-11.Simulations shown in these figures include the waveform of Voltage Vs. Time (ns). Simulations for optimized circuit1 and optimized circuit 2 shown in Fig. 4-5 are given for 180nm, 130nm and 100nm, technologies.

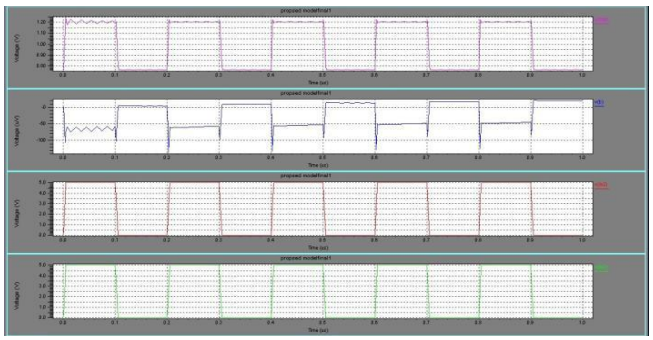
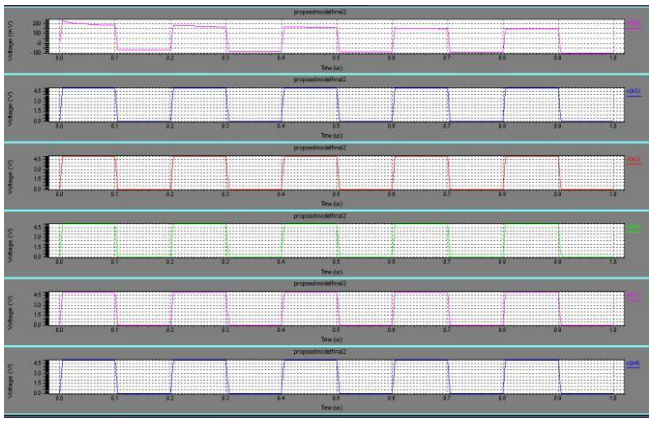


Figure 6. Simulations of optimized circuit1(180nm)

A. Results

Simulations of an optimized circuit1 and optimized circuit 2 are shown in Fig.6 and Fig.7. It can be observed from the simulations that power and delay. In optimized circuit2 reduce the power in comparison of optimized circuit1.And also delay in an optimized circuit2 is also less as compared to optimized circuit1.

Simulations for Fig.4 are shown in Fig.6 for 180nm technology. Simulations of optimized circuit2 shown in Fig.5 are shown in Fig.7 for 180nm technology. Power and delay are reduce both circuits comparison on 180nm technology.



Figure(7). Simulations of optimized circuit1(180nm)

Simulations of an optimized circuit1 and optimized circuit 2 are shown in Fig.8 and Fig.9. It can be observed from the simulations that power and delay. In optimized circuit2 reduce the power in comparison of optimized circuit1.And also delay in an optimized circuit2 is also less as compared to optimized circuit1.

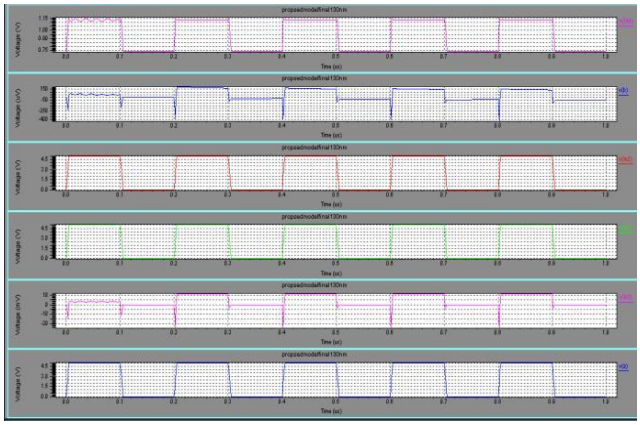
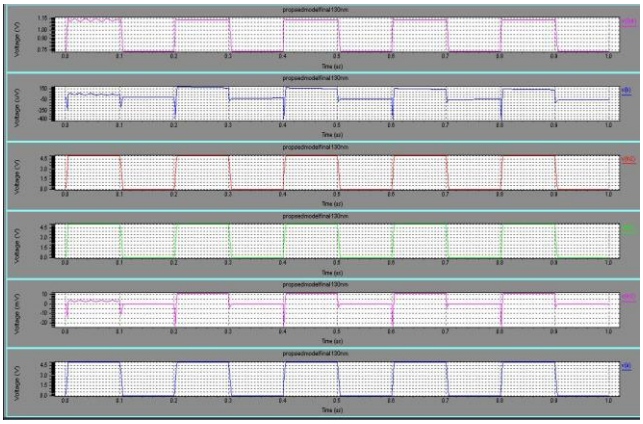
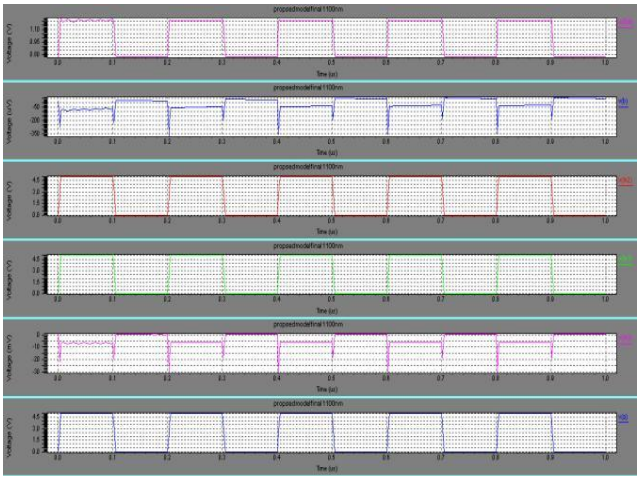


Figure (8). Simulations of optimized circuit1(130nm)

Simulations for Fig.4 are shown in Fig.8 for 130nm technology. Simulation
s of optimized circuit2 shown in Fig.5 are shown in Fig.9 for 130nm technology. Power and delay are reduces both circuits comparison on 130nm technology.

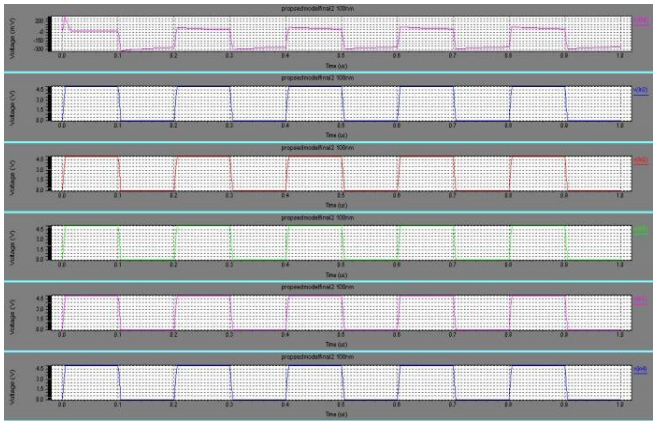


Figure(9). Simulations of optimized circuit (2) (130nm)



Figure(10). Simulations of optimized circuit1(100nm)

Simulations of an optimized circuit1 and optimized circuit 2 are shown in Fig.10 and Fig.11. It can be observed from the simulations that power and delay. In optimized circuit2 reduce the power in comparison of optimized circuit1.And also delay in an optimized circuit2 is also less as compared to optimized circuit1.



Figure(11). Simulations of optimized circuit2(100nm)

Simulations for Fig.4 are shown in Fig.10 for 100nm technology. Simulations of optimized circuit2 shown in Fig.5 are shown in Fig.11 for 100nm technology. Power and delay are reduces both circuits comparison on 180nm technology.

TABLE I. COMPARISON BETWEEN OPTIMIZED CIRCUIT 1 AND OPTIMIZED CIRCUIT 2(180 nm)

Circuit/Parameter	Optimized Circuit1	Optimized Circuit2
Power	6.0220340e-004watts	1.886437e+015watts
Delay	1.0317e-007	0.0000e-000

TABLE II. COMPARISON BETWEEN OPTIMIZED CIRCUIT 1 AND OPTIMIZED CIRCUIT 2(130 nm)

Circuit/Parameter	Optimized Circuit1	Optimized Circuit2
Power	5.749456e-004watts	3.019896e+015watts
Delay	1.0266e-007	0.0000e-000

TABLE III. COMPARISON BETWEEN OPTIMIZED CIRCUIT 1 AND OPTIMIZED CIRCUIT 2(100 nm)

Circuit/Parameter	Optimized Circuit1	Optimized Circuit2
Power	6.944558e-004watts	3.019892e+015watts
Delay	1.0308e-007	0.0000e-000

V. CONCLUSION

Scaling down of the technology has led to increase in leakage current. Nowadays, a leakage power has become more dominant as compared to Dynamic power. But, Dynamic
Power consumption due to glitches can't be neglected. Therefore, in this paper, the efficient technique has been proposed for reducing power and delay reduction in CMOS VLSI Circuits. The proposed method results in ultra low power consumption. Two optimized circuits are giving good results in terms of power and delay. The comparison is shown in Table I given below. The results are simulated using Tanner tool in 180nm technology at

room temperature for the circuits shown in Fig. 4-5.

Circuits shown in Fig.4-5 are simulated in Tanner tool for 130 nm. Comparison table given in Table II has shown above. The results are simulated using Tanner tool in 180nm technology at room temperature for the circuits shown in Fig. 4-5. Circuits shown in Fig.4-5 are simulated in Tanner tool for 100 nm. Comparison table given in Table III has shown above. The results are simulated using Tanner tool in 100nm technology at room temperature for the circuits shown in Fig. 4-5.

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