Full Adder Design by Area Minimization

Vinayak yadav, Rajesh Mehra

***Abstract*— The design of a new full adder which is simulated at 45nm CMOS technology. This design is based on a 3-transistor XOR Gate, two 2X1 multiplexers and one CMOS inverter. The main objectives to design this circuit are minimum power and small size of full adder.various methods are available for making full adder using more no. of transistor designing but these captured more area on chip. So this design required less area using small building blocks. The design performance is analysed using Microwind Layout Editor on 45nm Fabrication Technology.**

***Index Terms*— *Fulladder*, MOS, Multiplexer, NoiseMargin, chiparea**

I. INTRODUCTION

The high end improvements in the applications of circuits is the driving force to find new directions in the design of high performance circuit designs. Now a day's low power consumption along with minimum delay and mininum area is one of important design consideration for IC designers. Most the required applications in integrated circuits needed arithmetic and logic circuits for calculations.The basic unit that can be used for designing the arithmetic calculation is a binary adder or full adder circuit. Binary addition is basic and most frequently used arithmetic operation in microprocessor, digital signals processors (DSP) and Application specific circuit etc. Hence the high performance of this basic unit directly improves the performance of the overall design. The performance parameters that are very important in today's application technology are low power and high speed circuit designs. A structural level optimized designed of full adder is derived here for small size circuit applications.

II. FUNDAMENTALS

A full adder is under comes in the category of combinational circuits which adds upto three binary digits. the design of full adders which forms the basic building blocks of all digital circuits.

Conventional Equations of outputs of a full adder are: Sum = A xor B xor C
Carry = AB + BC + CA

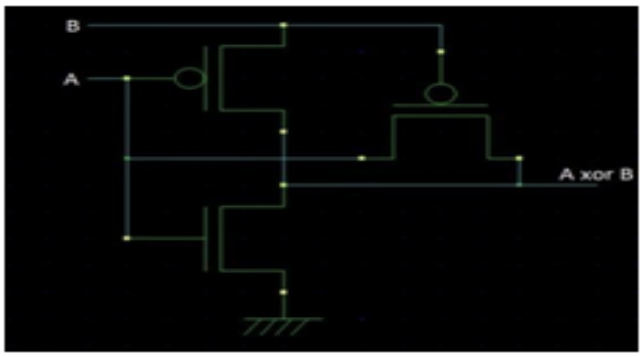
III. PROPOSED DESIGN

Proposed design of full adder with transistors is shown in figure. The design is basically divided into three building blocks.In this design one xor gate, two multiplexer circuits and one inverter has present and all these combined make a full adder circuit and perform operations of binary addition. This design is made in DSCH tool.On the basis of design the resultant SUM and CARRY equations of full adder are- SUM=(A xor B)not C +not(Axor B) C CARRY=(A xor B)C +not(A xor B)not C

IV. BASIC BLOCKS

A. *3Transistor XOR Gate:*

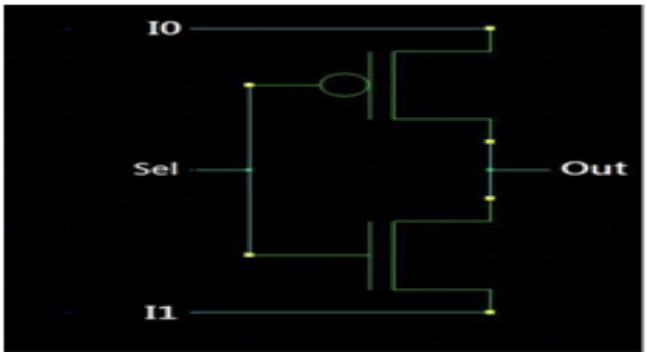
XOR gate is the basic building block for full adder. 3T XOR Gate used in this design shown in fig(1).the XOR consists of three transistors which are two PMOS and one NMOS. design is based on a modified version of a CMOS inverter. When the input B is at logic high, the inverter on the left functions like a normal CMOS inverter. Therefore the output Y is the complement of input A. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M3 is enabled The and the output Y gets the same logic value as input A. The operation of the whole circuit is thus like a 2 input XOR gate.



Fig(1)

B. *2X1 MUX:*

The proposed design will consider such another building block. 2X1 MUX used in design shown in fig(b).The MUX consists of one PMOS and one NMOS transistor. whose gate terminals are connected to each other and make another input select line.



Fig(2)

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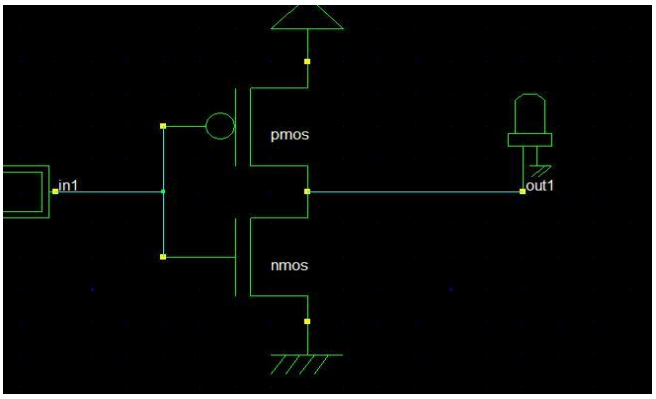
C. Inverter:

This is the last building block of the design. Which shown in fig(c).this block made up of one PMOS and one NMOS transistor connected in complementary manner. in DSCH tool the square block shows input of the circuit and LED shows the output.all transistors are shown in green colour and line matching them is blue. Colour depends on the tool which we use inthe designing.



V. GATE LEVEL DESIGN:

The module (integrated circuit) is implemented in terms of logic gates and interconnections between these gates.the gate-level diagram of the design should know is very important.

In general, gate-level modeling is used for implementing lowest level modules in a design like, full-adder, multiplexers, Etc.

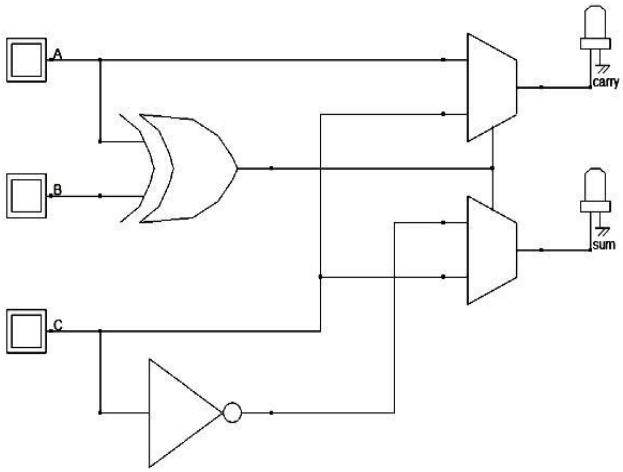


Fig.(3)

VI. LAYOUT OF FULL ADDER:

These three basic blocks combined together and make a full adder. . the main objective behind layout designing of any logic smooth flow of work, material, and information through a system. There are five pmos transistors which shows by brown colour and four nmos transistors shows by green colour. which is shown in fig(4).

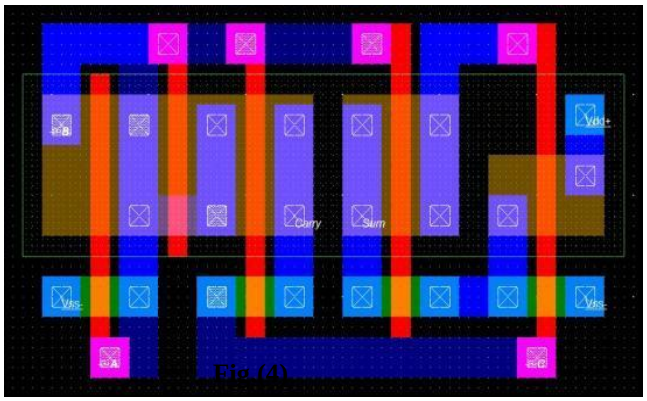
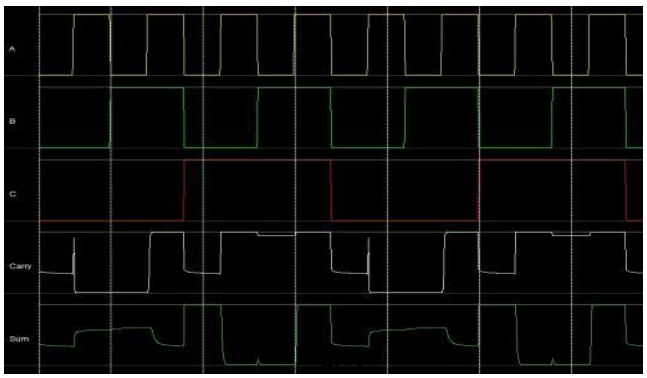


Fig.(4)

VII. SIMULATION RESULT:

The simulation results has got on microwind layout editor tool which gives complete outer structure of any digital logic including output of full adder in sum and carry form. which is shown in fig(5). VDD=1.4V and VSS=0V

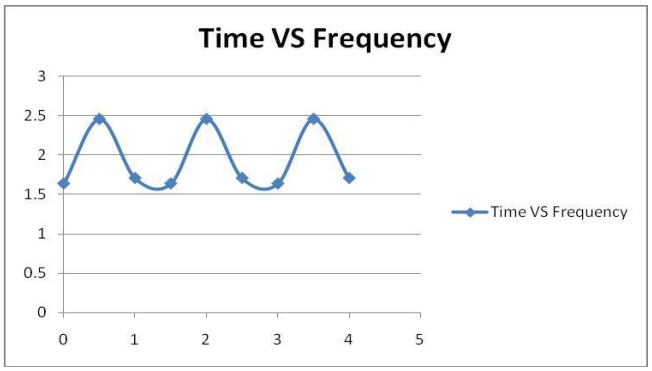


VIII. TABLES RELATED OUR DESIGN

Input			Output	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Design	No of Transistors	Comparison Parameters	
		Technology	Power
Proposed	9	45nm	0.099uW
[1]	8	0.35um	550.7272uW
[2]	10	0.6um	0.891uW
[6]	10	0.35um	0.409uW
[8]	8	90nm	89.57uW

This comparison table gives the effective results than other designs. Which compares between different CMOS technologies and no. of transistors used for making full adder designs. proposed design gives better power and output voltage results than other technologies. here another comparison table in our design which gives comparison between different technologies and area of the chip.



The graph b/w time and frequency shown in fig(g). which gives the information about output of full adder which is sum and carry. Time is in ns and frequency is in GHz. In simple way we can say that the o/p of full adder has very high frequency that means less errors has occurred so noise margin of total circuit is very low.

Design	No of Transistors	Comparison Parameters	
		Technology	Area(um2)
Proposed	9	45nm	15.12um2
[1]	8	0.35um	16.51um2
[2]	10	0.35um	15.12um2
[6]	14	0.35um	15.95um2
[8]	16	0.35nm	18.26um2

IX. SUMMARY

This is the complete description of our proposed design. The design has 45nm CMOS technology which has many advantages then other designs ie high power output, high fan out and area effective. the design gives all the outputs of full adder logic very accurately.and the schematic designing of this digital logic on DSCH tool. The proposed full adder can operate at low voltages, yet giving quite a good speed.

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