VHDL Code of Vedic Multiplierwith Minimum Delay Architecture

Vaibhav Jindal, Mr. Navaid Zafar Rizvi, Dinesh Kumar Singh

***Abstract*— The ever demand in enhancing the ability of process or the time of process will be as low as possible. The delay in the processes is affected by the root delay and the logic delay. The logic delay plays main role in calculating the delay of any process. The logic delay of any process is reduced by using minimum hardware architecture. So which architecture of Vedic multiplier used in the process so the delay is minimum.**

***Index Terms*— Vedic multiplication, VHDL, Hardware Design,Half Adder, Full Adder**

I. INTRODUCTION

With the latest advancement of VLSI technology the demand for high speed and portable digital signal processing system. Digital signal processing is present in every engineering discipline. In the fastest growing technology, it poses tremendous challenges to the engineering community to make fastest addition and multiplication. Therefore DSP engineers are constantly looking for new architecture with minimum delay.

Multiplication isthe most common and important arithmetic operations having wide applications in different areas of engineering and technology. The performance of any circuit is evaluated mainly by estimating the silicon area and speed (delay). Hence, continuous efforts are being made to achieve the same. In order to calculate the square of a binary number, fast multipliers such as Braun Array, Baugh-Wooley methods of two's compliment, Booth's algorithm using recorded multiplier and Wallace trees are in use. Recursive decomposition and Booth's algorithm are the most successful algorithms used for multiplication. Other methods include Vedic multipliers based on 'Urdhva Tiryagbhyam' and the "Duplex" properties of 'Urdhva Tiryagbhyam'. [1]

Vedic mathematics is the name given to the ancient system of mathematics, which was rediscovered, from the Vedas between 1911 and 1918by Sri Bharati Krishna Tirthaji. The whole of Vedicmathematics is based on 16 sutras[2]. In this paper we will discuss the possible multiplier architecture of Vedic mathematics with its hardware implementation and VHDL code. A simple concept of digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra is presented. [2] The organization of this paper is as follows. Section 1 present the basic logic for 4X4 multiplier block and Section 2, explainhow the 4X4 multiplier is implemented with minimum hardware use.

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II. VEDIC MULTIPLICATION

4X4 Multiplier: Let's take two inputs, each of 4 bits, say $A_3A_2A_1A_0$and $B_3B_2B_1B_0$. As inputs are of 4 bits the result is of maximum 8 bits, or if the input is of maximum n bits the multiplication is of maximum 2n bits.

A_3	A_2	A_1	A_0
B_3	B_2	B_1	B_0

S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

The Vedic *Sutras along with their brief meanings are enlisted below alphabetically.* [3]

1. (Anurupye) Shunyamanyat -If one is in ratio, the other is zero.
2. ChalanaKalanabyham -Differences and similarities.
3. EkadhikinaPurvena- By one more than the previous One.
4. EkanyunenaPurvena -By one less than the previous one.
5. Gunakasamuchyah-Factors of the sum is equal to the sum of factors.
6. Gunitasamuchyah-The product of sum is equal to sum of the product.
7. NikhilamNavatashcaramamDashatah -All from 9 and last from 10.
8. ParaavartyaYojayet-Transpose and adjust.
9. Puranapuranabyham -By the completion or noncompletion.
10. Sankalana- vyavakalanabhyam -By addition and by subtraction.
11. ShesanyankenaCharamena- The remainders by the last digit.
12. ShunyamSaamyasamuccaye -When the sum is same then sum is zero.
13. Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14. Urdhva-tiryakbhyam -Vertically and crosswise.
15. Vyashtisamanstih -Part and Whole.
16. Yaavadunam- Whatever the extent of its deficiency.

Method1:

This Vedic multiplication method based on one of the sutra of Urdhva Tiryakbhyam, In this method S_0 is vertical product of bit A_0 &$B_{0,}S_1$the sum of$A_{0*}B_1$and A_1*$B_0$and tens bit of previous sum (S_0). All the multiplication is done with the same process. The ten's and the hundred's position bit are forward as the carry to next addition. Only the S_7 bit of answer will comes from the tens bit S_6 in the 4 bit multiplication process. In the n bit multiplication process the 2n-1 bit of answer is calculated like the same way as S_7 bit. The 4 bit multiplication process with different architectures of same method is shown in next section. The multiplication process shown in the figure.1

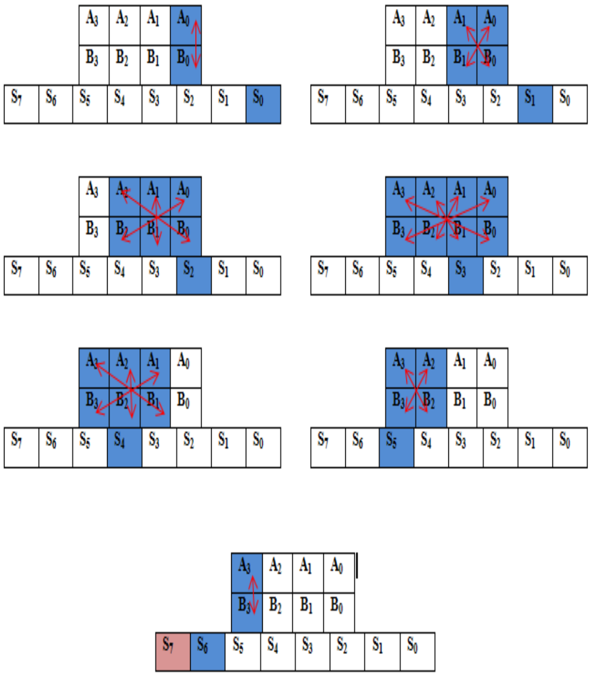

Figure.1 Method -1 of 4-bit Vedic Multiplier

For the multiplication of single bit a simple AND gate is used; now only the thing is how to make the addition process with minimum hardwareso the delay is as low as possible.

The vedic multiplication of 4-bit is process using the following equations-

$X=a_3\ a_2\ a_1\ a_0$

$Y=b_3\ b_2\ b_1\ b_0$

P_0- $a_0.b_0$

$P_1=a_1.b_0\ +a_0.b_1$

$P_2=a_2.b_0+a_1.b_1+a0.b_1+P_1(1)$

$P_3=a_3.b_0+a_2.b_1+a_1.b_2+a_0.b_3+P_2(1)$

$P_4=a_3.b_1+a_2.b_2+a_1.b_3+P_3(1)$

$P_5=a_3.b_2+a_2.b_3+P_4(1)$

$P_6=a_3.b_3+P_5(1)$

$Product=P_6\&P_5(0)\&P_4(0)\&P_3(0)\&P_2(0)\&$
$P_1(0)\&P_0$

The architecture for the equations are given the third section of this paper.

Method2:

Another Method for the multiplication of 4bit number is shows in Figure.2. This method is also based on one of the sutra of UrdhvaTiryakbhyam,In this method the 4 bit number is break in two parts higher and lower order bits and 2-bit Vedicmultiplication is performed as First 2x2 bit multiplier inputs are A_1A_0 and B_1B_0. The last block is 2x2 bit multiplier with inputs $A_3\ A_2$ and $B_3\ B_2$. The middle one shows two 2x2 bit multiplier with inputs $A_3\ A_2$ & B_1B_0 and A_1A_0 & $B_3\ B_2$. So the final result of multiplication, which is of 8 bit, $S_7\ S_6S_5S_4\ S_3\ S_2\ S_1\ S_0$.

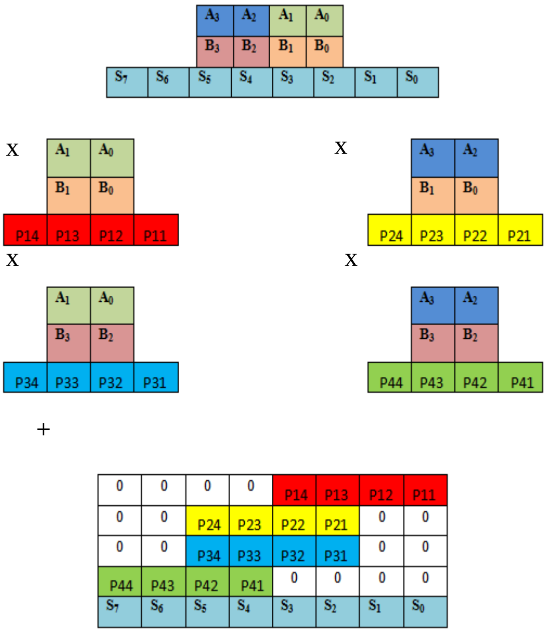

Figure.2 Method -2 of 4-bit Vedic Multiplier

To get the multiplication bit ($S_7\ S_6S_5S_4\ S_3\ S_2\ S_1\ S_0$) need of 8 bit adder. If same process is done with n-bits than the number is break into n/2 bits accordingly and 2n bit adder is used to get final result.

III. Hardware Implementation

Method1:

The hardware needed for the method 1 is the AND & OR gates, Half Adder (HA) and Full Adder (FA).The basic flow diagram is shown in the Figure.3.In this approach the delay is $(Pd_{AND}+(5xPd_{FA})+Pd_{HA})$

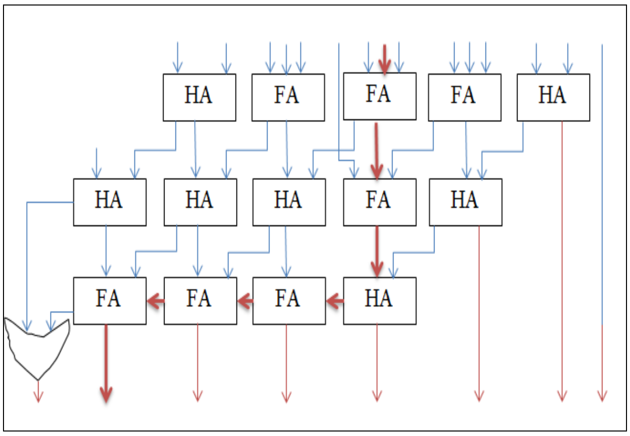

Figure.3 4-bit Vedic Multiplier Architecture1 of Method1

Where $Pd_{AND}$is delay of AND Gate,Pd_{HA} is delay of Half Adder and Pd_{FA} is Delay of Full Adder.

$$Pd_{FA}= 2xPd_{HA}+Pd_{OR}$$

$$Delay_{Method1Architecture1}=Pd_{AND}+11xPd_{HA}+5xPd_{OR}\ (1)$$

Now some how to reduce the delay, the design shown in the Figure.4 is with the less delay than the previous design. In this design the groups of FA are replaced by some HA. So, the delay of the path is affected.

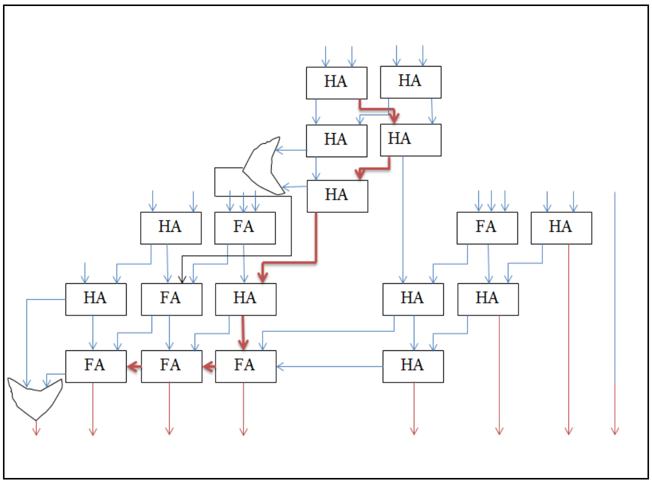

Figure.4 4-bit Vedic Multiplier Architecture2 of Method1

$$\text{Delay}_{\text{Method1Architecture2}}=Pd_{AND}+10xPd_{HA}+4xPd_{OR}(2)$$

From the equation 1&2 it is clear that propagation delay of the circuit is reduced.

Method2:-

For the method 2 of 4 bit Vedic multiplication the hardware requires is 4x2-bit Vedic multiplier and 3x8 bit adder. The architecture of the method 2 is given by KabirajSethiet all shown in Figure.6.Delay is more as 8 bit adder is used, some delay can reduced by using 8 bit adder still the delay is more so it has to be reduced. The 4-bit Vedic multiplier with less hardware is shown in Figure.7The delay of first architecture of method 2 is($Pd_{2vedic\_mul}+3xPd_{8bit\_adder}$)Where Pd_{2vedic_mul} is delay of 2-bit Vedic multiplier can give as $Pd_{AND}+2xPd_{HA}$and Pd_{8bit_adder} is delay of 8-bit adder given as Pd_{HA} + $7xPd_{FA.}$The delay of method-2 architecture is given as:-

$$\text{Delay}_{\text{Method2Architecture1}}=Pd_{AND}+47xPd_{HA}+15xPd_{OR}(3)$$

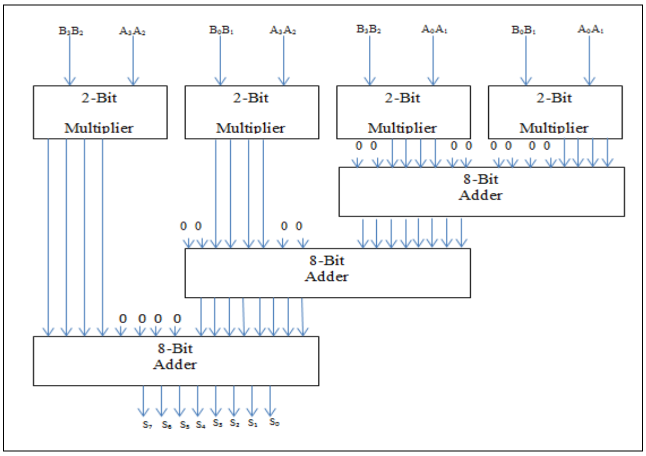

Figure.6 4-bit Vedic Multiplier Architecture2 of Method1 [1]

In the second architecture of method2 the 8-bit adder is replace by 4 bit adder. 4-bit adder needs the less hardware than the 8 bit added so, the path delay is reduced this architecture. The path delay of architecture2 is ($Pd_{2vedic\_mul}+3xPd_{4bit\_adder}$). Where $Pd_{2vedic_mul}$is delay of 2-bit Vedic multiplier given as ($Pd_{AND}+2xPd_{HA)}$ and Pd_{4bit_adder} is delay of 4 bit adder can be given as (Pd_{HA} + $3xPd_{FA}$).The delay of this architecture is given as:-

$$\text{Delay}_{\text{Method2Architecture2}}=Pd_{AND}+23xPd_{HA}+6xPd_{OR}(4)$$

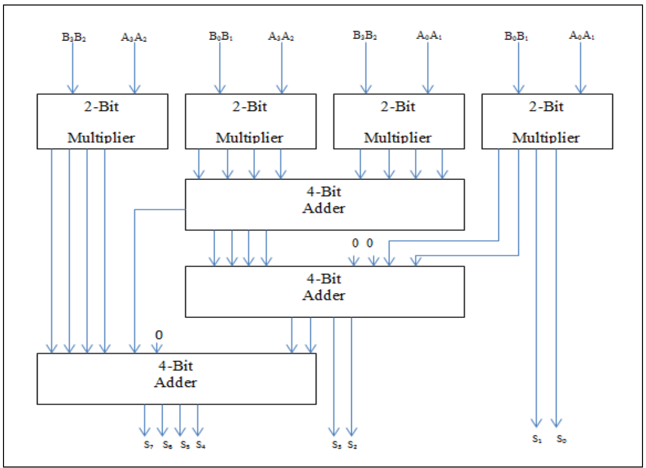

Figure.7 4-bit Vedic Multiplier Architecture2 of Method2 [1]

IV. Results

Now it has to be calculating that which architecture has the minimum path delay. To calculating the path delay hardware description code (HDL) is to be written for all architectures and has to be synthesis in xilinx path delay is the addition of logic delay and root delay.The root and logic delays are separately shown in the Figure.8Thedelays of all architecture are shown in Table.1 calculating using Xilinx ISE. In the table the total delay is the addition of root and logic delays.

	Delay Manually calculated	Slice Occupied	Total Delay (ns)
Method1 Arch.1	$Pd_{AND}+11xPd_{HA}+5xPd_{OR}$	20	14.310
Method1 Arch.2	$Pd_{AND}+10xPd_{HA}+4xPd_{OR}$	19	13.155
Method2 Arch.1	$Pd_{AND}+47xPd_{HA}+15xPd_{OR}$	20	17.829
Method2 Arch.2	$Pd_{AND}+23xPd_{HA}+6xPd_{OR}$	19	15.779

Table.1 Delay calculation of Different Architecture of 4- bit Vedic multiplier

From the above table it is clear that Architecture 2 of Method 2 is the fast one and its path delay is less than any other architecture.

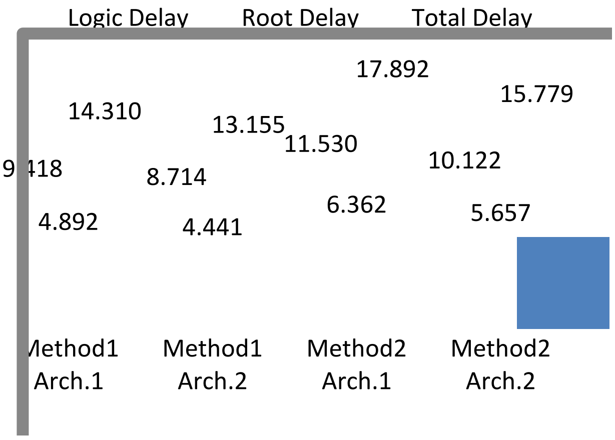

Figure.8 Delay Graph of Different Architectures of Vedic Multiplication

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