Design and Simulation of CMOS Cells using adiabatic technique for Low Power Consumption

Mr. Gaurav kumar, Atul S. M. Tripathi

***Abstract*—In the paper we will compare power consumption between conventional CMOS circuit and adiabatic logic circuit at 100nm technology for various power. Power consumption is the important and basic parameters of any kind of digital integrated circuit (IC). There is always a tradeoff between power and performance to meet the systems requirement. System cost is directly affected by power. Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. All simulation result and analysis are perform on 100 nm PTM technology using tanner tool [1].**

***Index Terms*— Low Power, Dynamic Power Dissipation, Static Power Dissipation, Adiabatic logic, Capacitor, Tanner Tool.**

I. INTRODUCTION

The main objective of this project is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have, is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and the dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this paper work, a new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy [4].

This project work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques. A family of full-custom conventional CMOS Logic and Adiabatic Logic units for example, an inverter, a two-input NAND gate, a two-input NOR gate [4].

Gaurav Kumar, Department of Electronics & Communication Engineering, IET, Mangalayatan University, Aligarh, India, +91-9568157019.

Atul S. M. Tripathi, Department of Electronics & Communication Engineering, IET, Mangalayatan University, Aligarh, India, +91-9837493088

II. STATIC POWER

The static or steady state power dissipation of a circuit depends upon logical state of circuit rather than switching activities and is expressed as[1]

$$P_{static} = I_{static} V_{DD}$$

where, Istatic is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power as in steady state there is no direct path from VDD to ground because PMOS and NMOS transistors are never becomes on simultaneously. Therefore static power dissipation is due to leakage currents and substrate injection currents. Another form of static power dissipation that occurs is called Ratioed logic. Pseudo-NMOS is an example of a Ratioed CMOS logic. In this, the PMOS pull-up transistor is always in on condition and acts as a load device for the NMOS pull-down network. Therefore, when the gate output is in low-state, there is a direct path from V_{DD} to ground and the static currents flow. In this state, the exact value of the output voltage depends on the ratio of PMOS and NMOS network hence the name. The static power consumed by these logic families can be considerable [1], shown in Figure (1)

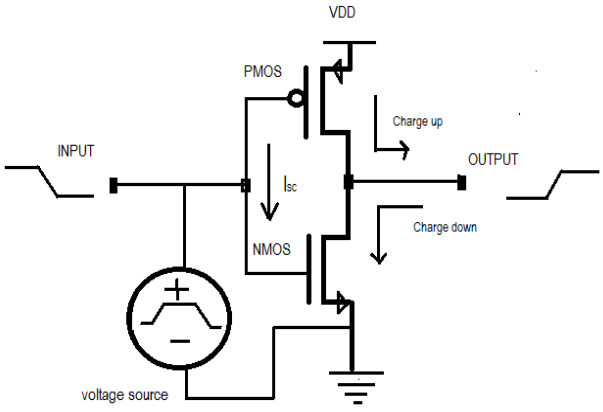


Figure 1: CMOS Inverter for power analysis

III. DYNAMIC POWER

Dynamic power dissipation is related to switching activities of device. At some point during the switching transient time, both the NMOS and PMOS devices become turned on [1].

The situation is modeled in Figure 1, where the parasitic capacitances are lumped at the output of the inverter. Consider the behavior of the circuit over one full cycle of operation with the input voltage going from VDD to ground and back to VDD again. As the input switches from high state to low state, the NMOS pull-down network is in cutoff region and PMOS pull-up network is in linear region charging the load capacitance C up to VDD. This charging process draws energy equal to CV_{DD}^2 from the power supply. Half of this is energy is dissipated immediately in the PMOS transistors, while the other half part is stored on the load capacitance. After that when the input returns to VDD, the process is reversed and the capacitance is discharged, its energy is being dissipated in the NMOS network. In other way , every time a capacitive node switches from ground to VDD (and back to ground), energy of CV^2_{DD} is consumed. This leads to the conclusion that CMOS power consumption depends on the switching activity of the signals involved. Now we can define activity, α as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, f is the clock frequency in a synchronous system, then the effective frequency of nodal charging is given by the product of the activity and the data rate: αf. Therefore average CMOS power consumption is[1]

$$P_{dyn} = CV^2_{DD}f$$

IV. ADIABATIC TECHNIQUE

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle. In the following section adiabatic switching analyzed in detail[1].

V. ADIABATIC SWITCHING

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant current source, as shown in Fig. 2. Here, R represents the on-resistance of the PMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage VC is zero initially, the variation of the voltage as a function of time can be found as[1]

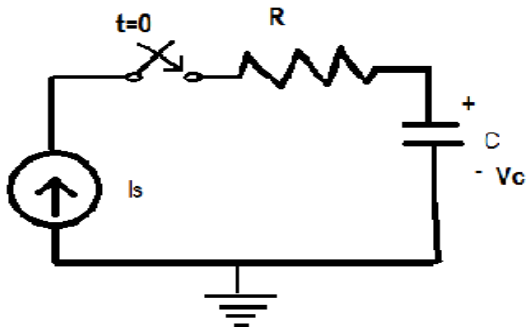


Figure 2: A Simple Adiabatic Logic Gate

In this we will examine simple circuit configurations which can be used for adiabatic switching. A general circuit topology for the conventional CMOS gates and adiabatic counterparts is shown in Figure 3. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up transistor and the pull-down transistor networks must be replaced with complementary transmission-gate (T-gate). The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull down function drives the complementary output node. Note that all the inputs should also be available in complementary form.

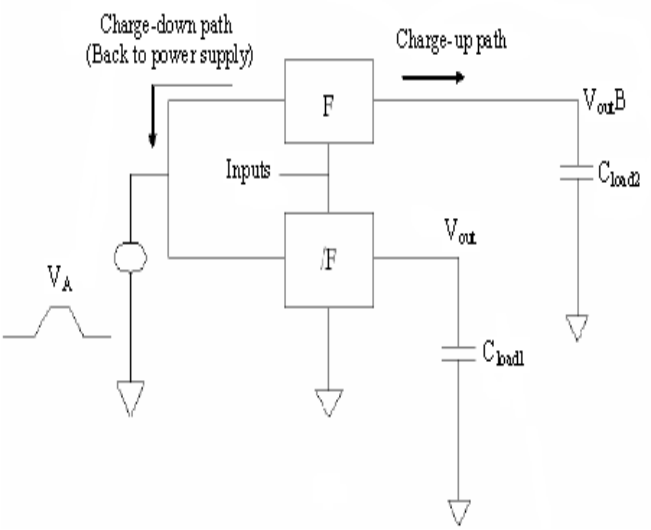


Figure 3: The topology of an adiabatic logic gate implementing the same function [1]

Both the pull-up and pull-down networks in the adiabatic logic circuit are used for charging as well as discharging the output node capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle shown in Figure (3).

To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a varying power supply with the ramped voltage output.

VI. SIMULATION OF ADIABATIC LOGIC CIRCUITS: NAND, NOR & INVERTER AND RESULT

In this section the study and implementation of combinational logic circuit using adiabatic logic and conventional CMOS techniques at transistor level is carried out along with the Power analysis[3].

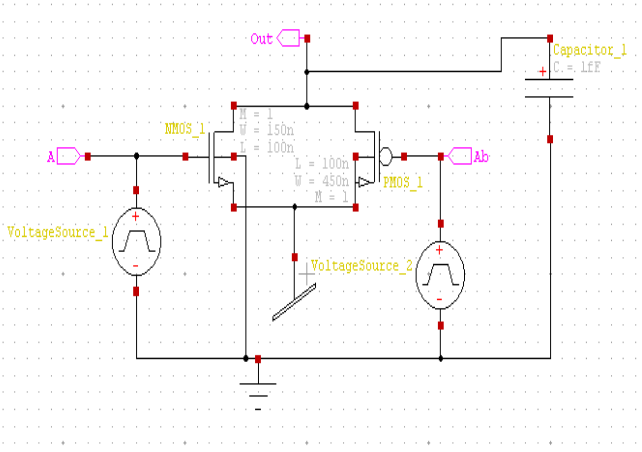


Figure 4.1: Schematic of Adiabatic inverter

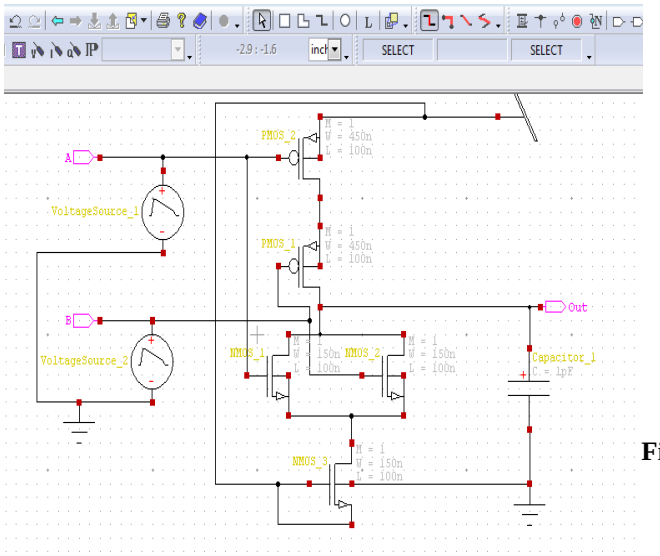


Figure 4.2: Proposed DFAL NOR gate circuit

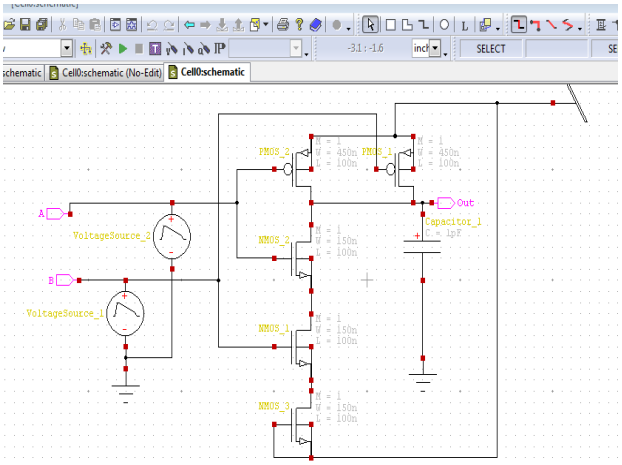
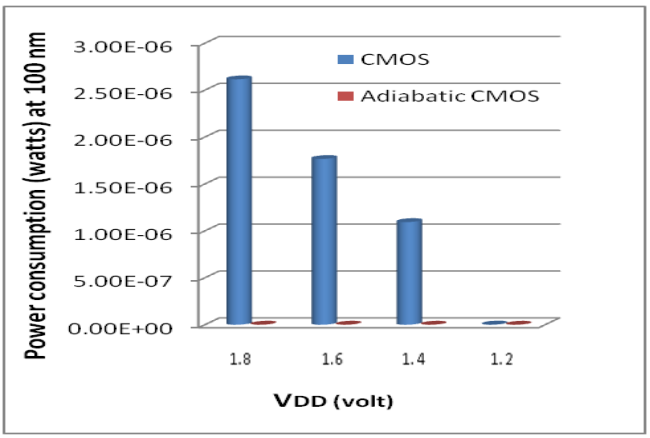


Figure 4.3: Proposed DFAL NAND gate circuit

The power consumed for conventional CMOS circuits and with Adiabatic power reduction technique for NAND, NOR gate and Inverter is calculated on 100nm technology with various voltage supply[3]. The graphical representation of power consumption in different Combinational Circuits is shown in Figure 4.1, 4.2, 4.3.

Table 1: Average Power Consumption comparison of CMOS Vs Adiabatic CMOS at 100 nm.

V_{dd} (Volt)	Average Power Consumption (Watts) at 100 nm	
	CMOS Inverter	Adiabatic CMOS Inverter
1. 8	2.62E-06	9.07E-10
1.6	1.77E-06	6.84E-10
1.4	1.09E-06	4.96E-10
1.2	1.91E-09	3.46E-10



Fie Figure 5.1: Graph of Average power consumption at various power supply.

Table 2: Average power consumption comparison of Conventional NOR gate Vs Adiabatic NOR gate at 100 nm

V_{dd} (Volt)	Average Power Consumption (Watts) at 100 nm	
	Conventional NOR GATE	Adiabatic NOR GATE
1.8	6.16E-07	3.34E-09
1.6	4.14E-07	2.59E-09
1.4	2.55E-07	1.96E-09
1.2	1.37E-07	1.42E-09

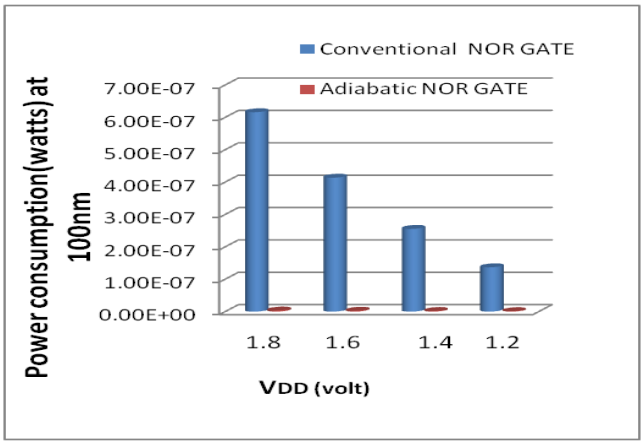


Figure 5.2: Graph of Average power consumption at various power supply.

Table 3: Average power consumption comparison of Conventional NAND GATE V/s Adiabatic NAND GATE at 100 nm.

Vdd (Volt)	Average Power Consumption (Watts) at 100 nm	
	Conventional NAND GATE	Adiabatic NAND GATE
1.8	5.26E-07	4.00E-09
1.6	3.57E-07	3.15E-09
1.4	2.22E-07	2.39E-09
1.2	1.18E-07	1.73E-09

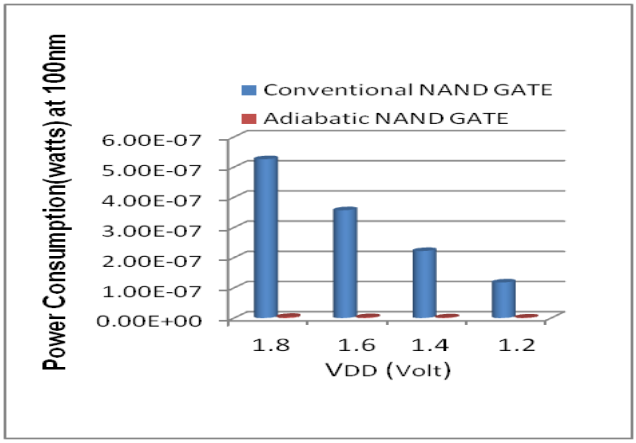


Figure 4.3: Graph of Average power consumption at various power supply

VII. CONCLUSIONS

Simulated Result are achived from proposed adiabatic NAND gate, NOR gate and CMOS iverter for low power consumption at the low frequency. The comparison of proposed adiabatic logic circuit with conventional logic circuit has proved that power consumption of adiabatic logic circuit is very less as compared to CMOS based technology. All simulated results are shows at 100nm technology using Tanner tool.

REFERENCES

[1] M. Sharma. Design and Analysis of CMOS Cells using Adiabatic Logic, Vol.1, No.2, International Journal of Networks and Systems, Mewar University Chittorgarh, Rajasthan (India) . November 2012, ISSN 2319 – 5975.

[2] Shipra Upadhyay , R .A . Mishra , R . K . Nagaria and S . P . Singh. Diode-Free Adiabatic Logic Circuits – ISRN Electronics, Volume 2013 (2013), Article ID 673601, December 2012, 12 pages.

[3] Pooja Chaudhary et al Int. Journal of Engineering Research and Applications ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013, pp.1603-1606.

[4] M.Sowjanya, S.Abdul Malik / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 3, Issue 4, Jul-Aug 2013, pp.1277-1280.

Gaurav Kumar: Mr. Gaurav Kumar is currently pursuing M.Tech. (E&C) from Mangalayatan University, Aligarh.

Atul Mani Shankar Tripathi : Mr. Atul Mani Shankar Tripathi is currently Asst. Professor at Mangalaytan University, Aligarh, India. He has completed his M.Tech. in Microelectronics from IIT(BHU) Varansi, India.