De-Multiplexer Design Using Transmission Gate on 90nm Technology

Shipra Sharma, Rajesh Mehra

***Abstract*— Power dissipation in low powered devices is one of the most important consideration now a days. It is very evident that hand held devices such as smartphones, calculators, tablets and laptops etc., which run on battery power, consume very low power for calculations and other operations. In this paper de-multiplexer has been designed using CMOS and transmission gate. The performance of both designs have been compared in terms of power consumption and transistor counts. The schematic of developed de-mux has been designed and simulated using DSCH and its equivalent layout has been created using Microwind. The result shows that transmission gate based de-multiplexer consumes 18 percent less power and 22 percent less transistor count as compared to conventional CMOS design on 90nm technology.**

***Index Terms*— De-multiplexer, CMOS, Power dissipation, Transmission gate,**

I. INTRODUCTION

Multiplexers and de-multiplexers are common building blocks of data paths and are used extensively in numerous applications including processor buses, network switches and digital signal processing stages incorporating resource sharing. The reduction of the power consumption by any VLSI circuit basically depends on the some parameters viz. reducing the number of transistor, reducing the size of the transistor, input re-ordering, reducing the capacitance etc. Transistor size optimization is one method to reduce the power dissipation of CMOS VLSI circuits. It is generally believed that low power designs need to have minimum transistor size. Most of the low-power design techniques are effective only for specific types of circuits and applications. Delay and power dissipation of a circuit have also emerged as majorconcerns of designers and depend on the number of transistors used in the circuit. When the number of transistors is more the capacitance is more due to which the delay is more [1] so here our aim is to reduce the delay and power dissipation. In this paper the author is applying technique like reducing the number of transistors, switching off some part of circuitduring different input conditions and using different elements in the implementation of the

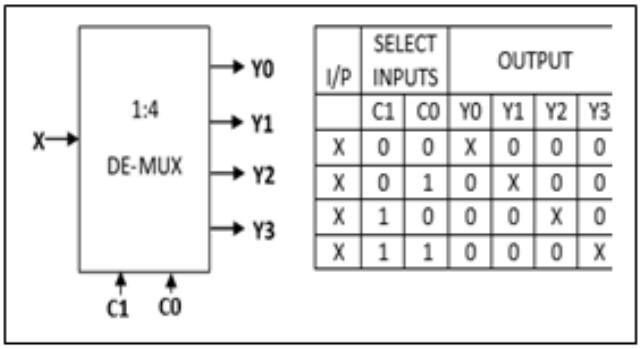
circuit to reduce the overall power consumption. The rest of the paper is organized as follows: The section II explains the working of a de-multiplexer circuit, the section III explains the two circuits of de-multiplexer one made using AND gates and another made using transmission gates and their timing diagram, section IV shows the layout diagram of two circuits with their analog simulation results provides comparison result between two designs. Finally the paper is concluded in section V.

Shipra Sharma, ME Scholar, ECE Department, NITTTR, Chandigarh, India

Rajesh Mehra, Associate Professor, ECE Department, NITTTR, Chandigarh, India

II. DE-MULTIPLEXER

Digital computers process and transfer tremendous amount of digital signal. It would be prohibitive to make separate straight wire connections for the transfer of all this data within the computer [2]. With the procedure of multiplexing, a single wire is used to transfer data from multiple sources from the sending end. Now at the receiving end this data from various sources needs to be segregated for distribution to intended recipients. The device catering this need is a de-multiplexer. The graphical symbol and truth table of a de-multiplexer circuit is shown in Fig. 1.



I/P	SELECT INPUTS		OUTPUT			
	C1	C0	Y0	Y1	Y2	Y3
X	0	0	X	0	0	0
X	0	1	0	X	0	0
X	1	0	0	0	X	0
X	1	1	0	0	0	X

Fig. 1 Demultiplexer and its truth table

In the above circuit C1 and C0 are selection bits and X is the data bit. Depending upon the states of the selection bits, the data X is transferred to one of the four output connections. The routing of data bit on different output connections based on states of the selection bits is shown in Fig. 1.

III. DE-MUX DESIGN SIMULATION

Conventional de-multiplexer circuits are made using AND gates and inverters (NOT gates). In order to design a 1x4 de-multiplexer circuit, two invertersand four numbers of three input AND gates are required.A single AND gate with three inputs requires eight transistors to be used for implementation.In this way the number of transistors used for implementing total four numbers of three input AND gates becomes thirty two. In addition to this, the number of transistors required to implement two inverters are four. In all the implementation of 1x4 multiplexer using the conventional method requires thirty six transistors.The implementation of conventional de-multiplexercircuit using AND gates and inverters is shown in Fig. (2).

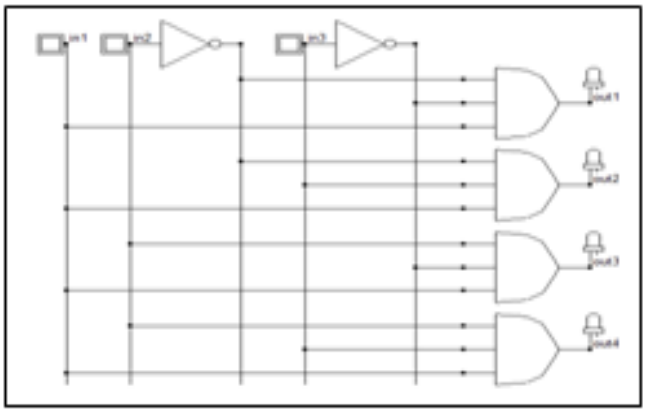


Fig 2. Conventional De-multiplexer

The de-multiplexer circuit shown in above figure works in the following manner: For the time when the input IN2 and IN3 are low, the first AND gate output will be high and the input will be redirected to the OUT1 LED. When IN1 and IN2 are 0 and 1 respectively, the input is directed to OUT2 LED. Next condition is when the IN1 and IN2 are 1 and 0 respectively, in this condition the third AND gate from top becomes active and input is directed to OUT3 LED. Last condition is when IN1 and IN2 both are 1, in this condition, the last AND gate from top becomes active and input is directed to OUT4 LED. The timing diagram of the de-multiplexer is shown in Fig. 3.

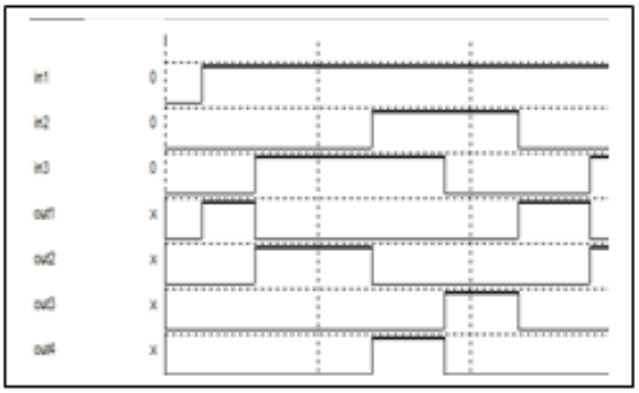


Fig 3. Timing diagram of 1x4 de-multiplexer

In this paper the de-multiplexer circuit design using transmission gate has been analyzed. The basic difference of pass-transistor logic compared to the
CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads [3]. The main advantage of using transmission gate logic is that it minimizes the number of transistors used for implementation of any logic circuit by eliminating redundant transistors. Transmission gate is an electronic element that selectively blocks or passes the signal level from input to output. The transmission gate comprises of NMOS and PMOS transistors. The control gates are biased in a complementary manner so that both transistors are either on or off. The schematic representation and circuit symbol of transmission gate are shown in Fig 4.

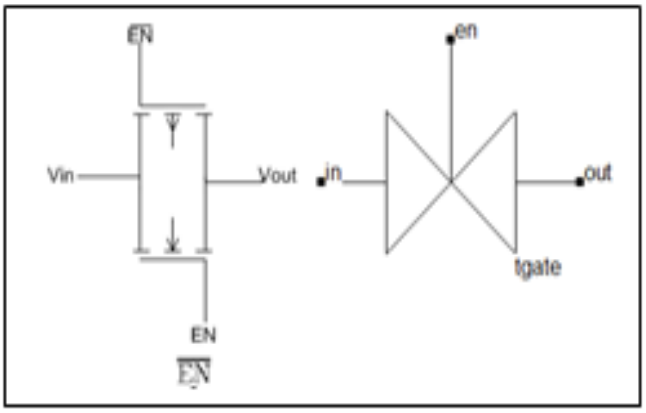


Fig 4 Schematic and circuit symbol of transmission gate

In the schematic diagram, the labels V_{in} and V_{out} are shown arbitrarily and can be reversed in order. In order to understand the operation of transmission gates, the entire input range of V_{in}needs to be investigated at both true and false values of the enable signal (EN). When the applied input EN is at logic level 1, its complementary input level 0 is applied at the active-low input EN. In this case the gate potential of the n type transistor is at V_{DD} and that of the p type is at ground potential. When the input (V_{in}) is below $|V_{Tp}|$, the p type transistor is closed as it needs to have a $V_{GSp} = V_{Gp} - V_{Sp} <= -V_{Tp}$ to conduct. The n type transistor on the other hand conducts as its gate-source voltage is large enough: $V_{GSn} = V_{Gn}-V_{Sn}$.

If the input voltage goes above $|V_{Tp}|$, the p type transistor starts to conduct. When the input voltage rises above $V_{DD} - V_{Tn}$ the gate-source voltage of the n type transistor becomes less than V_{Tn} so it cuts off. But by this time the p type transistor's channel is created and it connects the input and the output. In summary we can conclude that at least one of the transistors conducts during the entire input range when the enable input is true.

When the enable input is false (EN = 0) the gate of the n type transistor is at ground potential, that of the p type's is at V_{DD} voltage range of the input voltage the gate-source voltage of the n type transistor is less or equal to zero, so the transistor cuts off. The same is true for the p type as its source potential is less or equal than its gate potential in the entire range, thus its gate-source voltage is always non-negative. Thus when EN = 0 the transmission gate is equivalent to an open circuit between its input and output.

The new design consists of total six numbers of transmission gates with two inverters. The circuit arrangement of the new design is shown in Fig. 5.

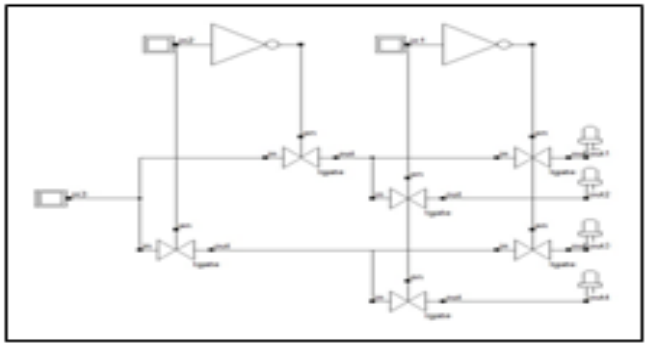


Fig 5. De-multiplexer using Transmission Gates

In this design of de-multiplexer the total number of transistors used has been reduced to 28 as compared to 36 in the conventional design. This reduction in the number of transistor helps in reduction of the power consumption of the circuit.

The new de-multiplexer circuit shown in Fig 5 works similar to the conventional de-multiplexer. Based on the select bits state i.e. 00, 01, 10 and 11, the input is directed to outputs OUT1, OUT2, OUT3 and OUT4 respectively.The timing diagram of the de-multiplexer is shown in Fig. 6.

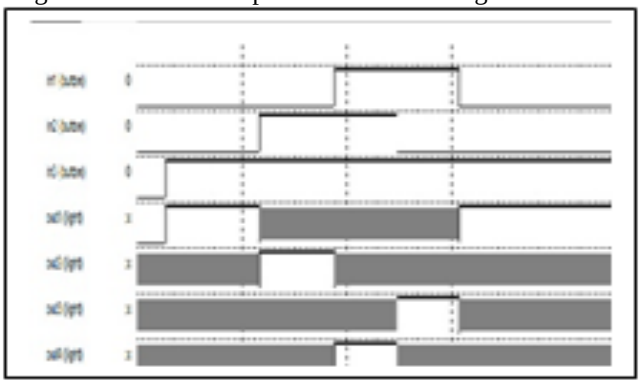


Fig 6. Timing diagram

IV. LAYOUT RESULT AND DISCUSSION

The main area of analysis in this paper is power consumption by the de-multiplexer circuit. In any digital CMOS circuit, the main reasons of power dissipation are gate leakage currents, short circuit currents while both transistors are partially on and dynamic power dissipation due to charging and discharging of the load capacitances.

The formula showing the power dissipation in circuit can be given as:

$$PD_{total} = P_{dyn} + P_{leak} + P_{sc} \quad (1)$$

In the above equation, the terms P_{leak} and P_{sc}denote leakage current and short circuit current respectively[4]. These powers dissipated in the circuit depend on the leakage current and short circuit current which are multiplied by supply voltage V_{DD} to calculate the dissipated power. These terms can be written as:

$$P_{leak} = I_{leak} * V_{DD} \quad (2)$$

$$P_{sc} = I_{sc} * V_{DD} \quad (3)$$

The dynamic power dissipation in the circuits can be given by formula:

$$P_{dyn} = CL * V_{DD} * f_{clk} * V \quad (4)$$

In the above equation, CL denoted the load capacitance, V_{DD} is the supply voltage, $f_{clk}$is the clock frequency which denotes the rate at which the transition from logic 0 to logic1 occurs in the circuit. V is the output voltage swing which is equal to the supply voltage in many circuits. In case of the transmission gates this value is slightly lower than the supply voltage [4].

The layout of the de-multiplexer circuit made using AND gates is shown in Fig. 7.

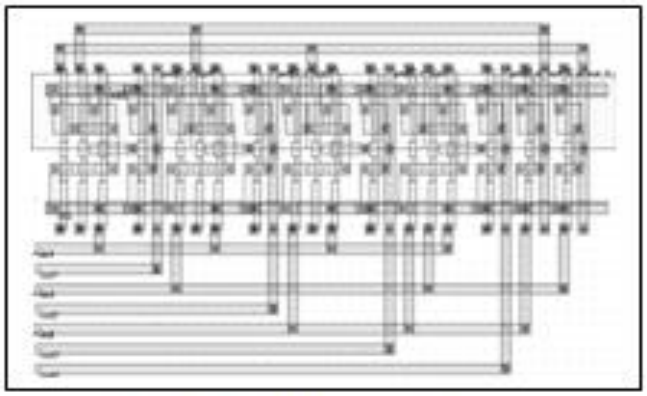


Fig 7. De-multiplexer layout

The analog simulation result of design shown in Fig. 7 is shown in Fig. 8.

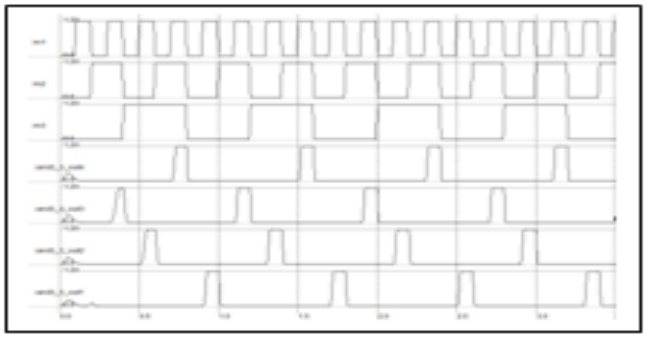


Fig 8. Analog simulation result

The layout of de-multiplexer circuit designed using transmission gates is shown in Fig. 9.

The analog simulation result of design shown in Fig. 9 is shown in Fig. 10.

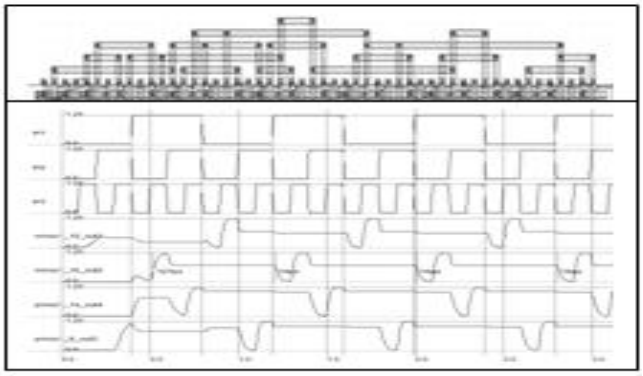


Fig 10. Analog simulation result

Different parameters of conventional de-multiplexer circuit and other made using transmission gate are compared in the table 1.

Table 1. Comparison of 1x4 De-multiplexer

Sr.No	Properties	1:4 DE-MUX using gate	1:4 MUX using transmission gate
1.	Rise delay	19pS	15pS
2	Fall delay	6pS	16pS
3	No of transistors	36	28
4	Power consumption	77.561µW	63.68µW

From the analysis of both the designs of the de-multiplexer circuits it is evident that the new designed de-multiplexer with transmission gates consumes less power than the conventional de-multiplexer.

V. CONCLUSION

The 1x4 de-multiplexer circuit has been designed using transmission gates. Power supply for the designed circuit is 1.2 volts. Circuit has been realized using 90nm technology. The power consumption of the designed circuit at 27^{o}C and 1.2 V supply is 63.68 µW which is lower than that consumed by conventional de-multiplexer designed with gates. The de-multiplexer can operate well up to 1.25 Gb/s. The number of transistors in the new circuit has reduced considerably. The total number of transistors used is 28 in new design as compared to 36 in conventional de-multiplexer design using AND gates. The new circuit provides an innovative method of designing de-multiplexer circuit using transmission gates which consumes lesser power than conventional design de-multiplexer. The future need of low powered devices is fulfilled by the new design which proves itself to be a proving model for new circuit.

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