Area & Power Efficient Design of XNOR-XOR Logic Using 65nm Technology

Swati Sharma, Rajesh Mehra

***Abstract*— XNOR-XOR gates are used in many arithmetic and logical circuits. This paper presents combination of XNOR-XOR circuit by using transmission gate and CMOS inverter to reduce area & power consumption. The developed logic has been design using 65nm technology on microwind3.1. The proposed design has consumed seven transistors as compared to 16 transistors in case of existing design. The performance of simulated circuit has been evaluated and compare in terms of power & area consumption. It can be observed from the result that purposed design can reduce 30 % area and 34% power as compared to CMOS based design**

***Index Terms*—** CMOS, Transmission gate, VLSI, XNOR-XOR

I. INTRODUCTION

In the growth of the integrated circuit towards large integration density with high operating frequency the concern issues are power, delay and smaller silicon area with higher speed. XNOR and XOR gate are used in various circuits like arithmetic circuit, code converter and error detection. The performance of the complex logic circuits is affected by the XNOR-XOR circuits [1]. In this paper we propose a new design of XNOR-XOR gate using transmission gate with CMOS inverter circuit. It covers less area compared to 16 transistors XNOR-XOR with CMOS circuit as well as less power with smaller delay. In VLSI technology, MOS circuits have been widely used in many fields. There are two types of MOS, i.e. the NMOS and the PMOS. Where NMOS transistor can gives the "LOW" signal completely, but it has poor performance at "HIGH' signal. Same as in PMOS transistor which gives the "LOW" signal completely but poor performance at "HIGH" signal. So the CMOS transistor is used. CMOS transistor is the combination of NMOS and PMOS transistor which gives full output voltage swing. The design analysis is required for XNOR- XOR circuit with less delay as well as low power consumption in a critical path.

In this paper, we propose a new circuit of XNOR-XOR gate using transmission gates with CMOS inverter. The advantage of transmission gate has to provide higher speed and lower delay. The paper is organized as follows: in Section II Transmission gate logic and CMOS inverter is explained, section III the proposed design of XNOR-XOR gate is presented and in section IV the simulation results and layout design analysis are given and discussed.

The comparison and evaluation for proposed and existing designs are carried out. Finally a conclusion is drawn in section V.

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II. TRANSMISSION GATE LOGIC

NMOS and PMOS device gives poor performances when transmitting particular logic signal. The NMOS degrades the logic level '1' while the PMOS degrades the logic level '0'. Thus, a perfect transmission gate can be constructed from the combination of NMOS and PMOS devices, leading to improved performances. This transmission gate has high speed due to low input capacitance but it has only limited capacity to drive a load. It has the advantage of being simple and fast. The static and transient performance depends upon the availability of high quality switches with low parasitic resistance and capacitance. Its static power dissipation is constant and dynamic power is very less. The drawback in a transmission gate is that it needs inverted signal values to control gates of PMOS and NMOS, respectively [2]. The problems with transmission gate are it degrades the output as it passes through various stages and no isolation between input and output terminal. Figure-1 shows the symbol of transmission gate where input is denoted by A and output is denoted by B, input E is used as an enable signal or control signal. The function of control signal is to decide the operation of transmission gate. When E=1 it passes the signal from A to B. When E=0 it works as an open circuit.

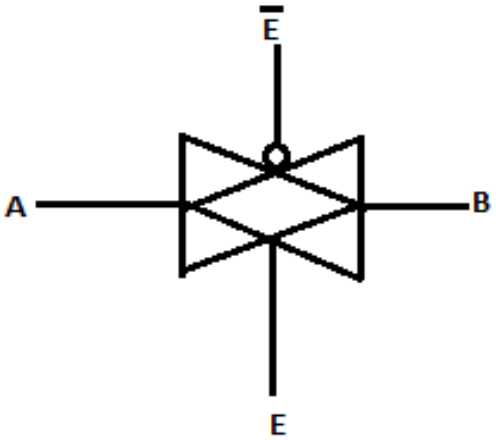

Figure-1 Transmission Gate

In this paper we design the XNOR-XOR circuit by using CMOS transistor and compare it with the proposed design of XNOR-XOR circuit using transmission gate with CMOS inverter circuit. Figure-2 shows the XNOR-XOR combine gate using CMOS transistor circuit. There are total sixteen transistors used in which 8 transistors are PMOS and rest are the NMOS transistors. The NMOS transistor can give the "LOW" signal completely, but it has very poor performance at "HIGH" signal. Similarly PMOS transistor can gives the

"HIGH" signal completely, but poor performance at "LOW" signal [3].

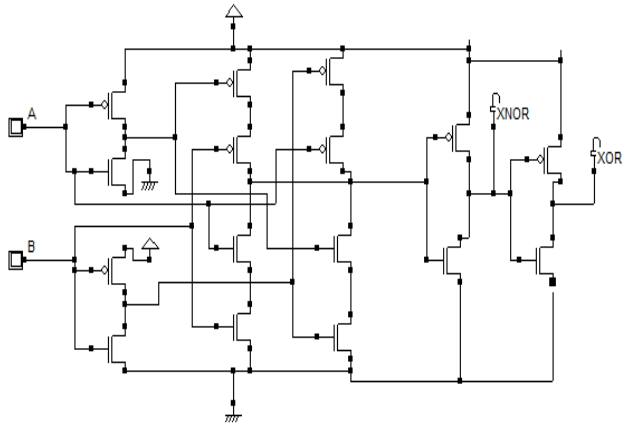

Figure-2 XNOR-XOR gate using CMOS

Figure-2 shows the XNOR-XOR gate using CMOS transistor circuit. The CMOS transistor is the combination of PMOS and NMOS so we get the full output voltage swing between HIGH and LOW voltage. When both inputs (A and B) are at zero signals then all PMOS transistors are in active high condition while all NMOS transistors are in cut off condition. So above circuit produce high signal at XNOR output and simultaneously produces low signal at XOR output.

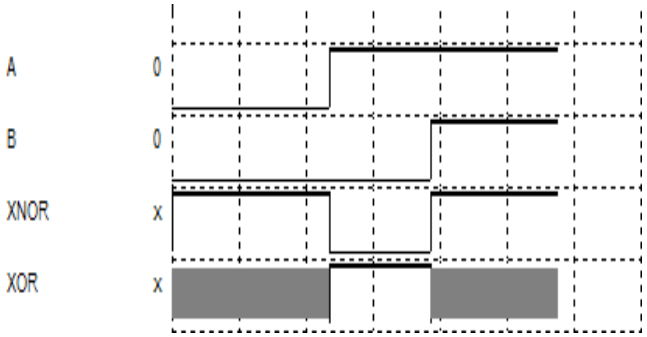

Figure-3 DSCH waveform of XNOR-XOR

Figure -3 shows the DSCH waveform of XNOR-XOR gate using CMOS transistor, it satisfy the function of XNOR-XOR gate. When both inputs are at LOW logic the XNOR gives HIGH logic at the output, whereas the XOR gate generates the LOW logic at the output.

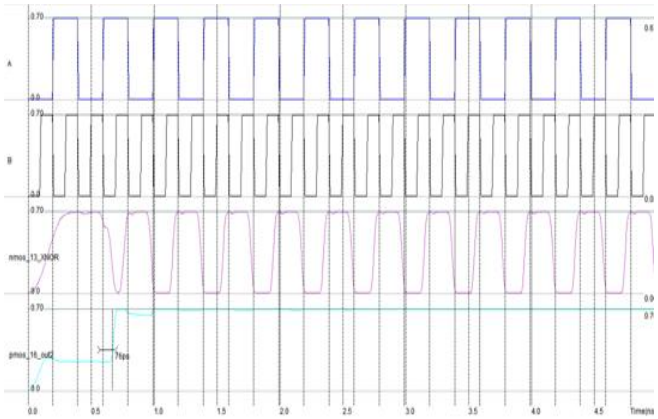

Figure 4 Output wave form of XNOR-XOR

Figure-4 shows the input and output waveform of the XNOR-XOR design using CMOS transistors. The output wave form is constant after some iteration.

III. XNOR-XOR SCHEMATIC

The XOR and XNOR gate functions are shown in Table 1 and denoted by $\oplus$ and $\odot$ respectively. The logic expression for XNOR and XOR are [4, 5].

$$P \oplus Q = \bar{P}Q + P\bar{Q} \quad (1)$$

$$P \odot Q = \bar{P}\bar{Q} + PQ \quad (2)$$

TABLE 1. XNOR AND XOR GATE FUNCTION

P	Q	XNOR	XOR
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

The proposed design of XNOR-XOR gate using transmission gates with CMOS inverter is shown in Figure 5. It uses a concept of transmission gates and CMOS inverter. The CMOS inverter is driving the transmission gate to achieve the perfect output voltage swing. P and Q are given as the input of transmission gates through CMOS inverter. Output of transmission gates gives the XNOR output and using an inverter we get the XOR output. The transmission gate allows to passes the signal through it, when the enable signal of transmission gate is high. The transmission gate has a n-channel device and a p-channel device, the n-channel MOS is situated on the bottom of the p-channel MOS. When zero signals apply to the enable (i.e. en) pin the transmission gate is off, and no signal is transferred through it. When enable signal is asserted high, the input signal appears to the output.

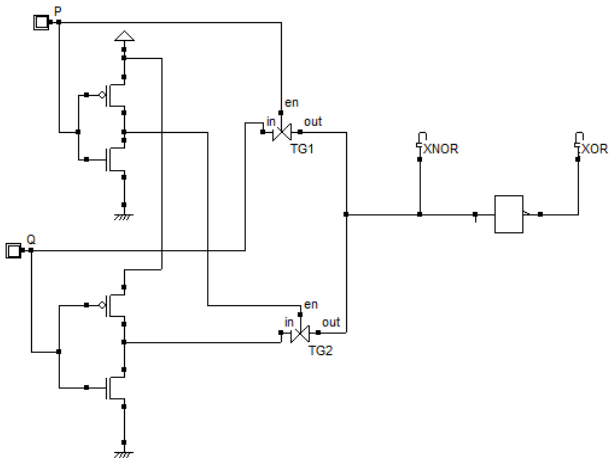

Figure-5 Proposed design of XNOR-XOR gate

The function of above circuit is summarized with the given Table 2. Here different values of P and Q apply to the proposed circuit and according to input values TG1 and TG2 change the state ON and OFF position.

Table 2 TG1 and TG2 function

P	Q	TG1	TG2
0	0	OFF	ON
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	OFF

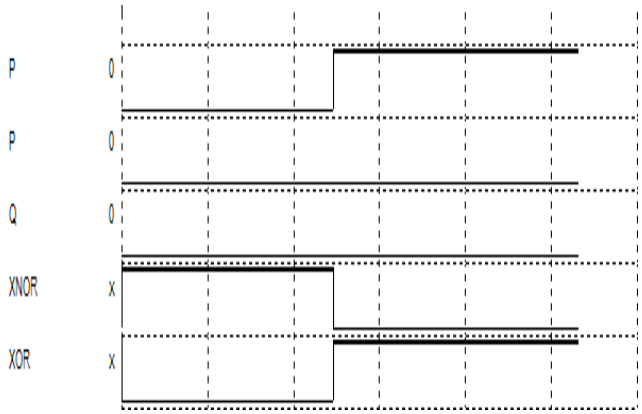

Figure-6 DSCH Waveform of XNOR-XOR

Transmission gate require lower switching energy and it reduces the count of the transistor used to make different logic gates [6, 7]. Figure 6 shows the DSCH wave form of proposed design of XNOR-XOR logic.

IV. Layout Design Analysis

Figure -7 shows the layout design of proposed design in which it shows that it require lesser number of transistors compared to the XNOR-XOR gate using CMOS. A total of seven PMOS and NMOS transistors are used.

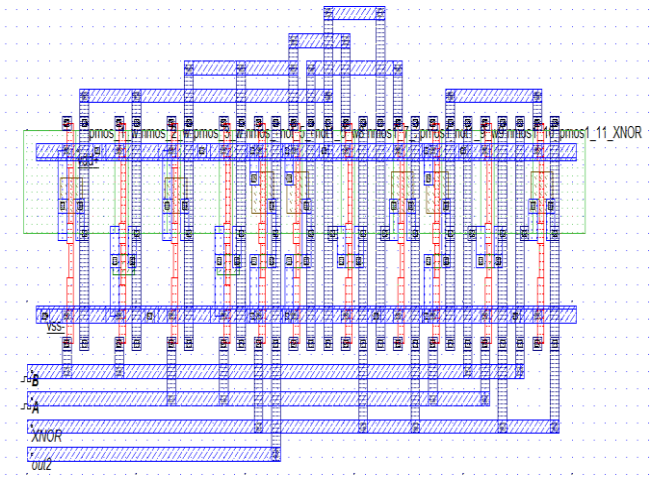

Figure-7 Layout design of XNOR-XOR logic

The XNOR-XOR gate is simulated by microwind 3.1 in the voltage range of 0.6V to 1.2V using 65nm CMOS technology. The power and delay measurement is 12.98µW and 130ps. Simulation is performed with different input conditions which show the transition of output signal with respect to input. The delay has been computed between the input signal P and XNOR output voltage level to the time it output reaches 50% of voltage level for both rising and fall transition.

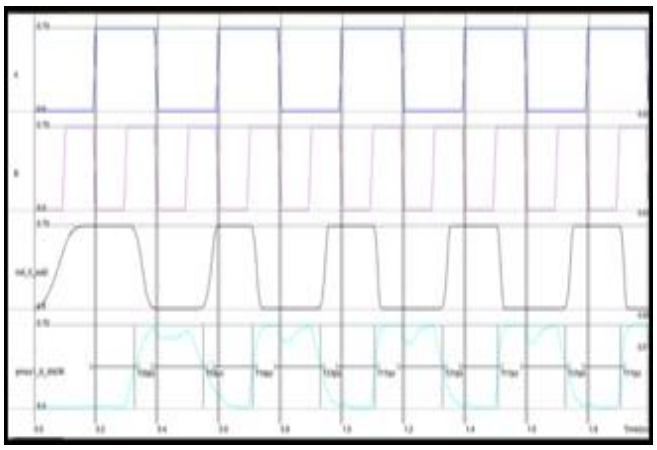

Figure -8 Output wave form of XNOR-XOR

Figure-8 shows the input signal P and Q, corresponding output signal also. We can see that XOR is a complement of XNOR gate. When P and Q are at LOW logic then XNOR output should be high but due to the some delay of gate the output gets changed after time.

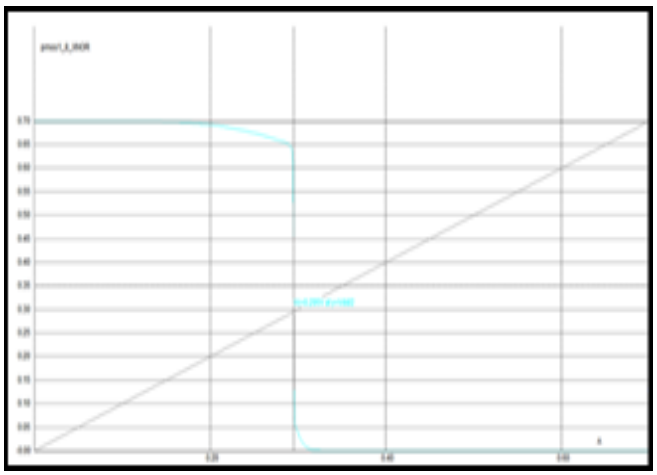

Figure-9 Transfer Characteristics.

Figure-9 Shows the transfer characteristics of XNOR-XOR gate in between input P and XNOR. So we can see that the XNOR output is complement of the input (P) signal.

Table-3 shows the comparisons between XNOR-XOR logic using CMOS and XNOR-XOR logic using transmission gate with CMOS inverter. It shows that the power required in XNOR-XOR gate using transmission gate is less compared to XNOR-XOR gate using CMOS circuit. Delay in proposed design is greater than the conventional design circuit because transmission gate has high switching speed and as we increases the number of transistors in a circuit the delay get introduces into the circuit [8, 9]. That is why it has high delay. The XNOR-XOR gate using transmission gate with CMOS inverter and XNOR-XOR gate using only CMOS are designed on 65nm transistor model in microwind3.1. The surface area of XNOR-XOR using CMOS transistor is 68.2µm^2 in which width of each transistor is 14.1µm and height of each transistor is 4.9µm. In the case of XNOR-XOR using transmission gate has low surface area i.e. 41.7µm^2 compared to conventional design.

Table-3 Comparison between XNOR-XOR using CMOS and transmission gate.

Parameters	XNOR-XOR using CMOS	XNOR-XOR using transmission gate
Power	18.416µW	12.198µW
Delay	76ps	130ps
Area	68.9µm^2	41.7µm^2
No Of transistors	16	7

Figure-10 Shows the compression between XNOR-XOR logic using CMOS transistors and XNOR-XOR logic using transmission gate. We can see that the conventional design has large power compare to proposed design. There is total 34% reduction in power consumption of proposed design.

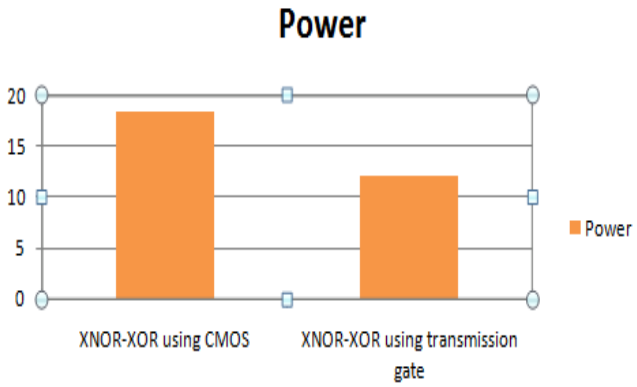

Figure-10 Power Graph

Similarly Figure-11 shows the area graph in which proposed design cover lesser area in compression to XNOR-XOR gate using CMOS. The XNOR-XOR gate using transmission gates require approximate 30% less area from XNOR-XOR gate using CMOS.

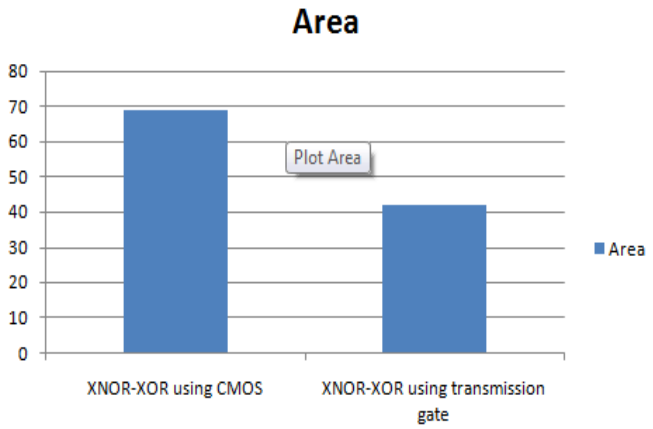

Figure-11 Area Graph

Figure-12 Shows the graph of XNOR-XOR logic using CMOS and XNOR-XOR logic using transmission gate. We can see that the conventional design require 16 transistor to design a XNOR-XOR circuit where as proposed circuit require less no of transistor.

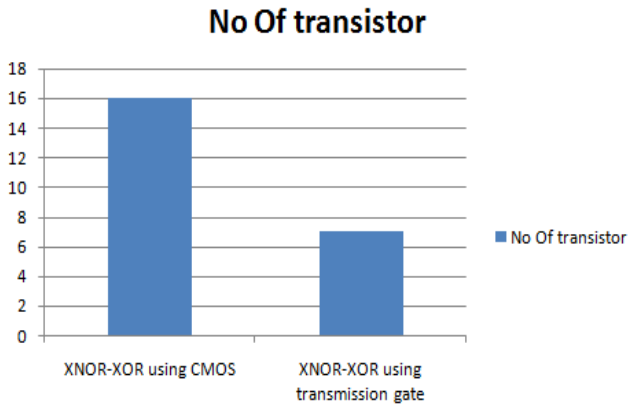

Figure-12 No of Transistor graph

V. CONCLUSIONS

In this paper, we proposed the new design of XNOR-XOR logic circuit configuration which is based on the transmission gate with CMOS inverter. The performances of this circuit have been compared to XNOR-XOR gate using CMOS in terms of power dissipation and area. According to the simulation results, the proposed design offers a better performance compared to CMOS based design. Proposed design reduces the power from the conventional circuit by 34% and area from the conventional circuit by 30%. It offers the lowest power dissipation at a low supply voltage. It has a good driving capability with good output signal in all input combinations and better performance. Thus, the proposed circuit is suitable for less area and low power application.

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