Modified Carrier Based PWM Technique for Multilevel inverter for High Power Applications with Reduced Number of Switches

M.Srilekha, P.Madhav

***Abstract*— In the present scenario, the event of multilevel inverter is becoming popular for industrial applications and better scale renewable green power technologies like cell , PV cell and turbine systems connected to the load. But the normal multilevel topologies have large components and sophisticated Pulse Width Modulation (PWM) controller resulting in reduced harmonics and voltage stress on the load. Therefore, a replacement topology of a cascaded multilevel inverter employing less number of switches with reduced gate driver circuits and straightforward control scheme is presented during this paper. A comprehensive MATLAB/ Simulink model of a seven-level inverter and therefore the generation of control pulses using multi-carrier-based PWM is evolved and discussed**

***Index Terms*— H-bride inverter; carrier disposition; PWM techniques; total harmonic distortion modulation index, multilevel inverter, pulse width-modulated (PWM).**

I. INTRODUCTION

In recent years, the research and development of multilevel converters/inverters are getting popular especially for high-power and high-voltage applications due to the generation of desired output voltage waveform from multiple DC voltage sources (Ebrahim, 2008). The fundamental concept of multilevel inverters is to trigger semiconductor switches arranged in a particular logic synthesising a staircase waveform. The more the number of steps in a waveform, the closer it is to a sinusoidal wave shape with reduced voltage (dv/dt) stress on load and harmonic distortion in output waveform, which results in improved power quality. This also provides good electromagnetic compatibility. However, a major drawback of multilevel inverter is that it requires a large number of power semiconductor switches compared to two-level conventional inverters. Every switch in the circuit demands a separate driver circuit to trigger the switches either on or off based on the firing gate signals. The requirement of multiple gate driver circuits makes the circuit expensive; consequently in practical applications, a reduction in the number of switches used is crucial. Therefore, a logical switching sequence needs to be developed to acquire the stepped wave shape with fewer switches and the control strategy will undoubtedly be less sophisticated. A decrease in the count would also minimize the burden when constructing a mechanical layout for the circuit. Besides, the incremental voltage steps traditionally produced with isolated DC sources or a bank of series capacitors are considered a serious drawback. Since the availability of DC sources may be limited from place to place, this could be a hindrance to the use of certain multilevel inverter topologies. Alternatively, voltage balancing is another problem with the use of series capacitor as a voltage divider. Conventional multilevel inverters include diode clamped converter (Nabae et al., 1981; Rodriguez et al., 2010), flying capacitors (Meynard and Foch, 1992) and cascaded H- bridge (Hammond, 1997; Malinowski et al., 2010). The cascaded H-bridge and the diode clamped are the most popular hardware-implemented topologies at present. Despite the fact that the latter topologies are commercially available in the markets, the number of voltage levels is limited due to complex control strategies and increased switches at higher levels. Declining availability and increasing costs of fossil fuels are compelling industries to look at renewable energy sources as alternative means of reliable energy source. Renewable energy sources such as photovoltaic cells and fuel cells can be interfaced with multilevel inverters for DC-AC power conversion. Other applications of multilevel inverters include FACTs, HVDC systems and Electric Vehicles. Recently new topologies or modifications of existing topologies have come into the scenario, all with the same intention of reducing output voltage distortion, reducing switching losses or even achieving a more compact design. Some new topologies are making use of a multi-winding transformer to get multiple outputs. This is applicable when there are few DC sources. The design and manufacturing of multi-winding transformers is complicated and costly. Also, the size of these transformers is relatively large and occupies huge space in the inverter. Other topologies utilise optimized algorithms for THD minimisation, at a low-frequency switching operation. Switching angles are specifically selected to reduce the harmonic content in the inverter's output voltage. Switching losses become negligible at low-switching frequencies; however, significant lower order harmonics will be dominant, which can lead to excessive heating in certain machines or utensils (McGrath and Holmes, 2002). In Electric Vehicle (EV) applications, cascaded H-bridge inverters are popularly used but with the major drawback of large number of isolated DC power supplies.

Only one power supply is desirable in an EV. The solution to the problem is presented in Yousefpoor et al. (2012) where an asymmetrical cascaded H-bridge is designed consisting of only one DC power supply to produce a very high level voltage output with the help of auxiliary small H-bridges acting as series active filter and using a small high frequency link. Asymmetrical cascaded H-bridge is also developed using non-equal DC input sources (Renuga and Prathiba, 2012). Similarly, a four-level DC-DC converter is developed using more switches and capacitors in Peng et al. (2010). It requires different ratings of semiconductor devices because the voltage stress of some switches may differ from that of the other

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switches, which proves to be a major downside of such topologies for high-power applications. Capacitor balancing is not an easy task and the size and cost of these capacitors may depend upon the load current. Najafi and Yatim (2011) developed a seven-level inverter using reduced number of MOSFET switches. This can be employed even for low-power applications, e.g. aircraft systems. The reduced component topology has greater efficiency, and inverter components are operated with line frequency without the need of additional switches for higher frequency operation. This leads to more reliable control of the inverter. Therefore, in this paper, a new topology of a cascaded multilevel inverter for high power and high-voltage applications is proposed in terms of design, control and good quality of power supply. A seven-level inverter is developed in MATLAB/Simulink environment with nine semiconductor switches. Phase Opposition Disposition (PD) multi-carrier Pulse Width Modulation (PWM) technique has been implemented in this topology.

II. CONVENTIONAL CASCADED MULTILEVEL INVERTER

A cascaded multilevel inverter uses a set of series connected full-bridge inverters with separate DC sources in a modular set-up to create the stepped waveform. A full bridge inverter in itself can generate a three-level output voltage and every module added in cascade to that extends the inverter with two more voltage levels, which then increases the number of steps in the waveform (Pereda and Dixon, 2012). Usually, in each bridge two switches conduct simultaneously, one switch in the first upper leg and the other in the second lower leg or vice versa. Two isolated DC sources are used, resulting in two voltage levels in both the positive half and the negative half of the waveform, making a total of five voltage levels including the zero level. One of the main advantages of cascaded multilevel inverters is their modular design and the manufacturing process becomes easier when compared with other complex topologies. The voltage stress on each switch is considered to be equal and all the switches will have identical power ratings. One can observe from here that it requires eight switches for a five-level inverter (Hammond, 1997; Malinowski et al., 2010). For a seven-level inverter model, 12 switches are needed, whereas the proposed model uses only nine switches. From the Table 1, it is observed that the diode clamped topology uses one switch more than the proposed topology. However, the control strategy for the former is much more complex than the latter. The multilevel inverter's greatest hurdle is the switch count. If fewer number of power semiconductor devices is employed, the complication of the control strategy will be lesser. Figure 1 shows the comparison of cascaded H-bridge and proposed topology to identify the requirement of switches for increased voltage levels. It is expected that the proposed topology would have an advantage over the conventional topologies for high-power and high-voltage applications in terms of simple design, control and cost of the set-up.

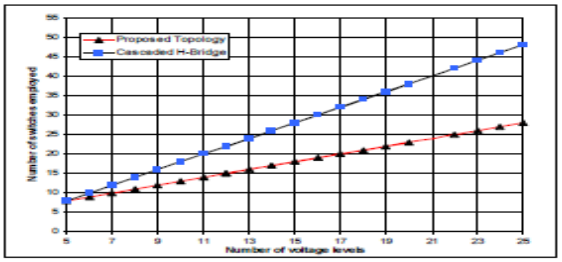

Fig.1 Voltage level vs. number of switches

Table 1. Comparison of component count with respect to a seven-level inverter

	Capacitor Clamped	Diode Clamped	Cascaded H-Bridge	Flying Capacitor	Proposed
No of Capacitors	14	6	-	15	-
No of Diodes	-	8	-	6	-
No of Switches	10	10	12	12	9
Total Devices	24	24	12	33	9

III. PROPOSED TOPOLOGY

The proposed topology has a set series connected to smaller multilevel inverter blocks (highlighted) as shown in Figure 2 (Nedumgatt et al., 2012). Each set will consist of two switches. Switch S8 and switch S9 should be conducting at different instances in order to prevent any short circuit across the voltage source. When switch S8 (S9 off) is turned on, the output will be equal to *Vdc* and when S9 is turned on (S8 off), output voltage will be zero.

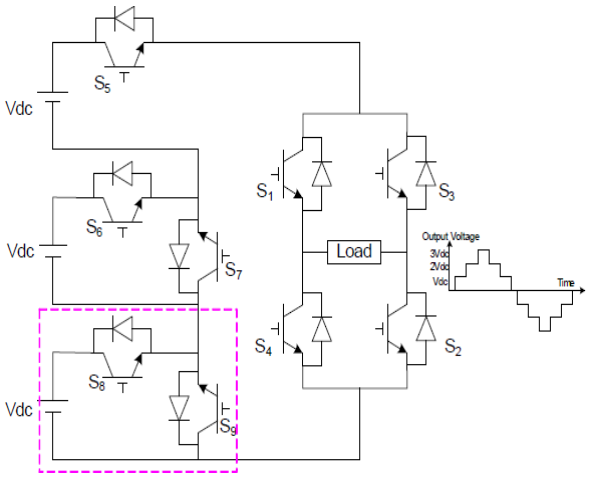

Fig.2 Modified H-Bridge Inverter

A set connected in a series of basic multilevel inverter blocks will achieve a stepped waveform. Isolated DC sources are necessary for this particular circuit's operation. Voltage balancing problems will not be encountered as in the case of other topologies due to stable and fixed DC levels. Each of the power DC sources used is equal to *Vdc*; hence, the circuit can also be described as a symmetrical multilevel inverter. Hence, the more the power sources, the more the steps in the waveform. From a mechanical design point of view, if a higher level inverter is needed, it easy to give provisions for the addition of basic multilevel block sets at the bottom (after switch S9) depending on the number of levels in question. A wave shape closer to a sinusoidal wave shape will power devices and loads with more accuracy, leading to less power losses, and consequently less heat generation (Nordvall, 2011). A typical seven-level output waveform that can be generated with the proposed topology is shown in Figure 2

The expected output voltage level (*n*) and their corresponding switches (*S*) can be calculated by

$S_{total} = (n-2) + K$, Where k = 4 (H-Bridge)

Each smaller multilevel unit will produce a voltage of *Vdc*. Maximum output voltage is equal to

$$V_{total} = V_1 + V_2 + \ldots\ldots\ldots\ldots\ldots\ldots V_N = NV_{dc}$$

where '*N*' is the number of DC sources.

To create both positive and negative voltage levels, an H-bridge is added to the circuit. Three levels will appear in the positive half and three levels in the negative half, and including the zero level, a total of seven levels can be generated. In Figure 2, the total switch count is nine for a seven-level inverter, whereas for a conventional cascaded multilevel inverter, it would be 12. With three switches being omitted in this topology, the gate driver circuit count also drops down by three, reducing the complexity of the overall circuit. In the H-bridge, switches in the same leg should not conduct simultaneously; appropriate gate pulses should be given in order to prevent any chances of short circuit conditions. Summarizing the operation of the topology, switches S5–S9 have the objective of producing the incremental voltage levels. Based on a specific sequence, the levels are added one above the other. Switches S1–S4 (H-bridge) have the purpose of providing a polarity to the waveform. Without the H-bridge, only four levels will be

developed in the positive side; thus, three more levels are generated in the negative half with the help of the latter switches. The primary objective of this paper is to minimize the number of power semiconductor devices of the conventional cascaded multilevel inverter. Again, each switch demands an individual gate driver circuit. However, the number of switches utilized is fewer than the conventional cascaded multilevel inverter. It reduces the installation area, gate drivers needed and consequently the cost of the whole set-up. At any given period of time, only five switches will be conducting, inclusive of two switches conducting in the H-bridge. Table 2 indicates which power semiconductor switches are turned on for the specific output voltage level. The sequence is repeated to create the staircase waveform.

State	Switchs					Output voltage
	S5	S6	S7	S8	S9	
0	Off	Of	On	Off	On	0
1	On	Of	On	Off	On	Vdc
2	On	On	Off	Off	On	2Vdc
3	On	On	Off	On	Off	3Vdc

Table 2. Switching States

IV. MULTI-CARRIER-BASED PWM TECHNIQUES

Carrier-based PWM techniques have been extensively put to use in multilevel inverters. Multi-carrier PWM techniques are categorised in two groups, namely Carrier Disposition (CD) methods and Phase-Shifted (PS) PWM methods. In the CD-PWM method, the reference waveform is sampled through a number of triangular carrier waveforms displaced by contiguous increments of the reference waveform amplitude. In the PSPWM methods, multiple carriers are phase shifted accordingly and compared with a reference sine wave (Crowley and Leung, 2011). The detailed comparison of multicarrier PWM technique is given in Wang and Zhu (2010). The Phase Disposition (PD) multi-carrier method is selected for this work because of the better utilization of DC sources.

Usually with three DC power sources for a seven-level inverter, six triangular carrier waveforms of the same frequency, phase and amplitude will be needed but with different DC offsets. Three of these are compared with the positive half of the reference sine wave and the remaining three are compared with the negative half of the sine wave (Malinowski et al., 2010). But this particular topology only requires three triangular carrier waveforms as seen in Figure 3, which makes the control circuit become easier.

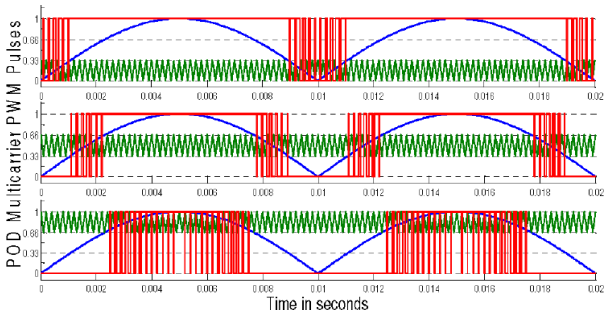

Fig 3. Multi Carrier PWM Pulses

These carriers are responsible for the generation of three voltage levels (excluding the H-bridge) to produce the positive and negative halves of the staircase wave shape (Calais et al., 2001). A carrier frequency of 5 kHz is generated and compared with a reference sine wave of 50 Hz. Unity amplitude modulation index has been selected. Which can Show in Fig.3.

The first set of pulses in Figure 3 is used to generate the first voltage level Vdc. This is followed by the second and third set of pulses to create the next two levels, *2Vdc* and *3Vdc*, respectively. These pulses are exclusively for switches S5–S9. These pulses are repeated for every half cycle. Suppose a source is not able to supply the required voltage level or is faulty; it can then be operated with the output level of 5 V from 7 V

V. SIMULATION RESULTS

Figure 4 shows the MATLAB/Simulink model of the proposed seven-level inverter consisting of three DC sources, nine IGBT switches and an LC filter. DC power source of 9 V batteries and a load of 25 W which is available in the laboratory are taken for the study Show in fig.4. The simulation work is divided into two parts. Firstly, a PWM technique using a low-frequency triangular wave (100 Hz) is compared with a fixed constant value. A multi-step wave shape is obtained after implementing this technique. In the second part, the PD-PWM methods are implemented. The main reason behind incorporating the different PWM methods is to analyse the harmonic spectrum of the inverter's output voltage. The modulation method that produced the best harmonic profile was implemented in the hardware model. The harmonic spectrum was analyzed using the FFT Window in MATLAB/Simulink.

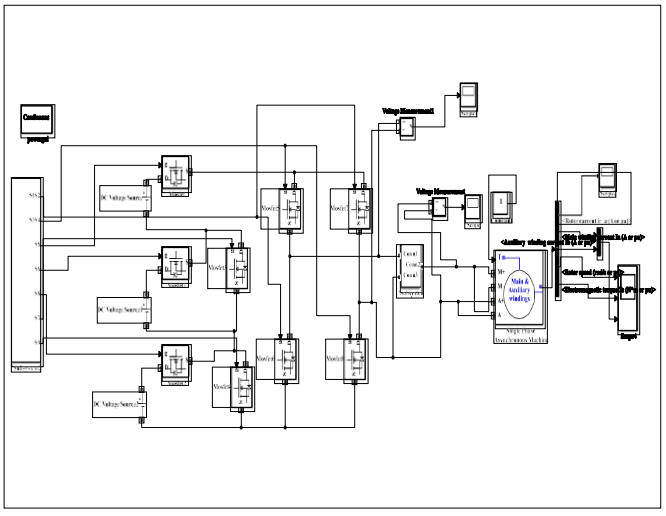

Fig.4 Simlink Model for Seven Level Inverter

Figures 5.1 and 5.2 show the inverter output voltage waveform and their frequency spectrums for equal pulse width and PD-PWM switching operations. The stepped pulse width could be varied for different output voltage levels of multilevel operation to minimize the harmonic content and without the need of additional filter components. These switches are closed only once in a cycle to reduce the switching losses and EMI problems. However, in Figure 5.1 the lower order 9th and the 13th harmonics are quite dominant, which reduce the desired magnitude of output voltage waveform as compared to the PWM method. The desired terminal voltage can also be maintained equally without compromising the harmonics by varying the step size. It would not be suitable for a hardware implementation because the size of the LC filter will then be large and bulky due the presence of lower order harmonics

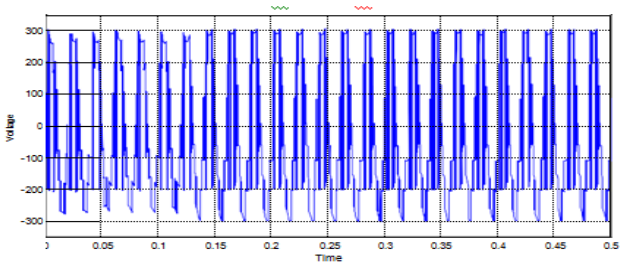

Fig.5.1 Output Voltage

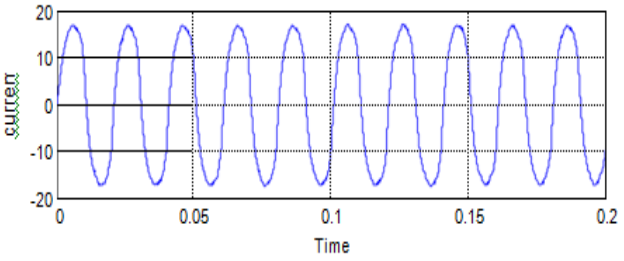

Fig.5.2 Output current

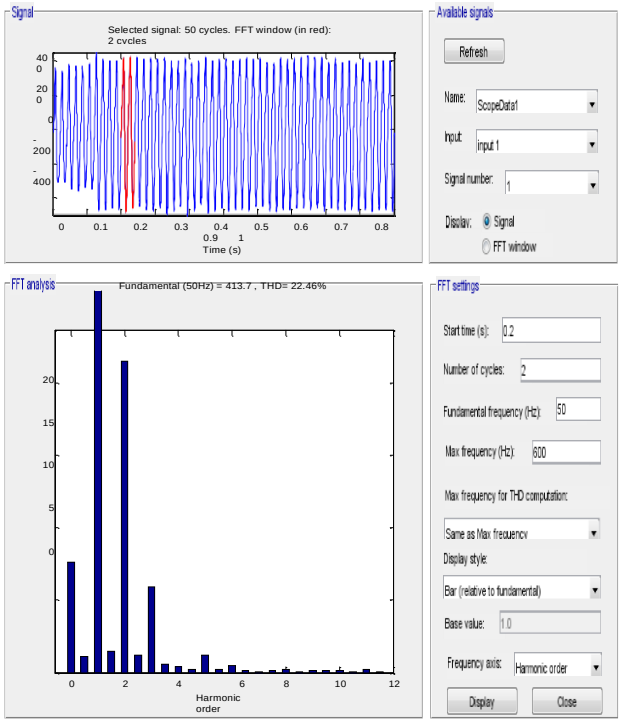

Fig.5.3.FFT Analysis Of Output Voltage

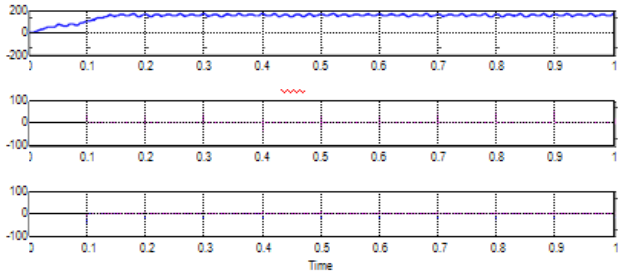

Fig.6 Motor speed , torque, Rotor Current

In Figure 5.2, one can observe that the low- order harmonics are considerably reduced as compared to Figure 5.3. The significant harmonic energy appears at the side band frequencies of the carrier frequency; in this case, the frequency is 5 kHz. Designing a practical filter would be easier in this case, due to the fact that only high-order harmonics need to be eliminated By using an amplitude modulation index much less than one for the PWM technique, the results in Figure 5.2 were obtained. The PWM technique applied in Figure 5.2 was used along with the filter and obtaining an output as shown in Figure 5.3, a THD of 3.7% which is within the limits of IEEE 519 harmonic standards. Figure 6 Can be show Motor Out put data ie rotorspeed in rad/sec, Torque in N-M and Rotor Current in Amp.

VI. CONCLUSION

A new topology of the cascaded multilevel inverter was successfully demonstrated to produce an increased stepped output with less number of semiconductor switches. The proposed topology operated with a minimum of nine switches compared with conventional H-bridge inverter using 12 switches to generate the same number of discrete voltage levels. Fewer switches present in the power circuit reduce the investment, and controlling. the overall circuit becomes less complex. Performance of the topology is compared with stepped pulse signal and PWM signal. Phase disposition multi-carrier-based PWM method is implemented in Matlab/Simlin The inverter output voltage waveform and its frequency simulation results will compare to conventional H-bridge inverers. Therefore, the proposed topology can be exploited for various applications like single phase induction motor, with cheap cost, compact size and less control where multilevel inverters are employed.

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