International Journal of Engineering and Technical Research (IJETR)
ISSN: 2321-0869 (O) 2454-4698 (P) Volume-9, Issue-3, March 2019

Efficient Layout Design using Transmission Gate in 45nm Technology

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***Abstract*— XNOR-XOR gates are generally used in arithmetic and logic circuits. This paper presents the performance comparison analysis for the combination of XNOR-XOR circuit by using transmission gate. The transmission gate has consumed only 10 transistors as compared to 16 transistors in case of conventional design. The performance of the simulated circuit has been evaluated and compared in terms of propagation delay, power & area consumption using 45nm technology. It can be observed from the simulated results that proposed circuit consume 63.97% less area and 90.66% less power as compared to existing design. The speed performance of proposed design is also improved by 85.38% to provide high performance solution for VLSI applications.**

***Index Terms*— CMOS, Transmission gate, VLSI, CMOS Technology.**

I. INTRODUCTION

In the evolution of the integrated circuit towards high frequency with integration density, the concern issues are power, less area and minimum delay with high speed. XNOR and XOR gate is used in several different circuits like an arithmetic circuit, error detection, and code converter. The working of complex logic circuits is depending on the XOR-XNOR circuits [1]. Speed of operations depends on the largest critical paths and number of transistors are used in circuits. [2] In this research paper, we design XOR-XNOR gate using the transmission gate with CMOS inverter circuit 45nm technology. Using transmission gate, it covers less area compared to 16 transistors XNOR-XOR with CMOS circuit as well as less power with a smaller delay. There are 2 types of MOS the NMOS and PMOS. Where NMOS transistor provides the "LOW" signal good, but poor for "HIGH" signal. Similar as in PMOS transistor which provides the "LOW" signal completely but poor for "HIGH" signal. So, the CMOS transistor is used. CMOS transistor is combination of PMOS and NMOS transistor which gives good output voltage swing. The design analysis is required for XNOR-XOR circuit with less delay as well as less power consumption in a critical path [3]-[7]. To reduce power consumption, implementations of a circuit have been considered as a good solution for many applications. [8]

In this research paper, we use circuit of XOR-XNOR gate using transmission gates with CMOS inverter. The advantage of the transmission gate has to provide higher speed and lower power consumption. This paper is organized in V sections as follows: in Section I introduction, Section II Transmission gate with CMOS inverter is explained, the designing of XNOR-XOR gate using transmission gate and with CMOS explained in section III, in section IV the simulation results and layout design analysis are given and discussed for both 65nm and 45nm technologies. The evaluation and comparison for transmission gate and existing designs with proposed design are carried out. Finally, conclusions are drawn in section V.

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II. TRANSMISSION GATE LOGIC

A transmission gate (TG) is which conduct in both directions by a control signal with almost any voltage potential, it is similar to a relay. It is a CMOS-based switch, in which NMOS passes a strong zero and PMOS passes strong one. Both NMOS and PMOS work simultaneously. NMOS and PMOS device gives mediocre performance when transmitting a logic signal. The NMOS deprave the logic level "1" while the PMOS deprave the logic level "0". Thus, an ideal transmission gate can be built from the merging of NMOS and PMOS, leading to better performances [9]. This transmission gate has high speed due to low input capacitance but it has only limited capacity to drive a load. the advantage of the transmission gate is simple and fast.

The static and transient performance depends upon the availability of high-quality switches with low parasitic resistance and capacitance [10]-[11]. Its static power dissipation is constant and dynamic power is very less. The drawback of transmission gate is that it requires inverted logic to control gates of NMOS and PMOS, respectively. The problems of transmission gates are they diminishes the output as input passes through multiple stages and no isolation is provided between output and input terminal. Figure-1 shows the symbol of the transmission gate and Figure-2 shows Schematic. When node A has high Logic 1, then complementary $\bar{A}$ has Logic zero is applied on A node, allowing both transistors to conduct and pass the signal between IN to OUT.

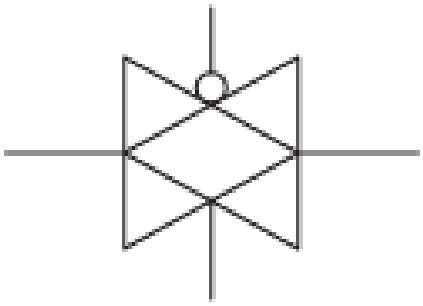

Figure-1 Transmission Gate Symbol

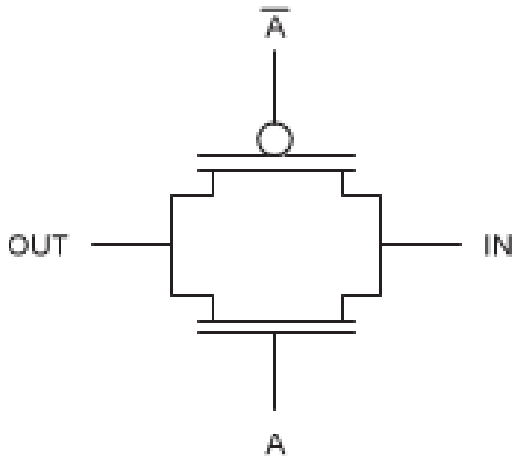

Figure-2 Transmission Gate Schematic

III. PROPOSED SCHEMATIC DESIGN

In this paper, designing of XOR-XNOR circuit by using a transmission gate inverter circuit in 45nm and compare its results with 65nm technology. Figure-3 Schematic of XNOR-XOR gate transmission gates. The CMOS inverter is required for the transmission gate to attain the good output voltage swing. A and $\bar{A}$ are provided as the input to transmission gates through CMOS inverter. The output of transmission gates provides the XNOR output and using an inverter we got the XOR output.

The transmission gate allows to passes the signal through it when the enable signal of transmission gate is at logic "1". The transmission gate has a p-channel device and n-channel device, n-channel MOS is located on the bottom of the p-channel MOS. When "0" signals logic applies to enable pin the transmission gate is turned off, and no signal is passes from it. When the enable is asserted high, the input signal passes to the output.

Table 1. Shows the truth table for XNOR-XOR gates. Figure-4 Timing Diagrams out1 is out-put of XNOR gate and out2 is for XOR.

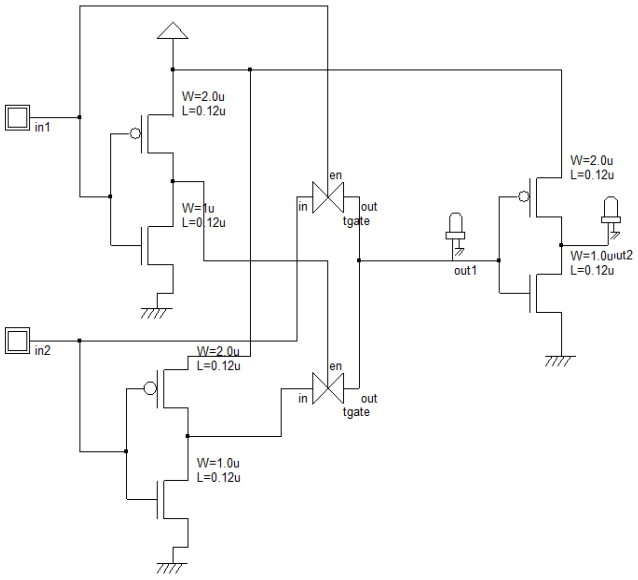

Figure-3 Transmission Gate based Schematic of XNOR-XOR

Table 1 XNOR-XOR Truth Table

in1	in2	XNOR	XOR
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

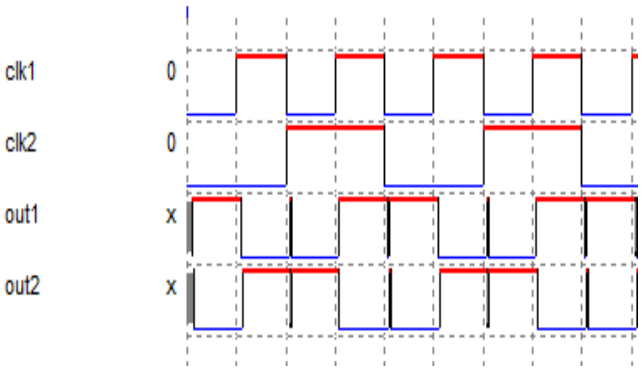

Figure-4 Schematic Simulation

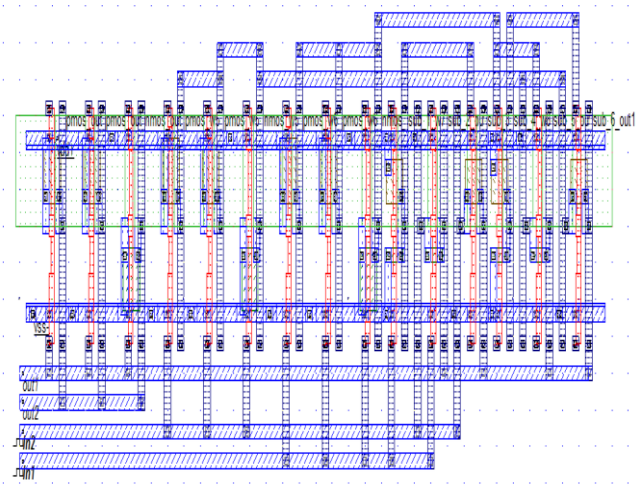

Figure-5 Layout Design- XNOR-XOR with Transmission

IV. LAYOUT DESIGN ANALYSIS

Once the circuit designing is completed in Dsch2 tool then Verilog file is created for circuit. Files is compiled in Microwind3.1 for layout design and simulation. Figure-5 shows layout design for XNOR-XOR circuit using transmission gate.

The XNOR-XOR gate circuit is simulated in Microwing3.1 with 45nm technology. Verilog files of designed circuit is compiled in Microwind3.1 with foundry setting in 45nm. XNOR-XOR using transmission gate (TG) are and simulation results is shown in Figure-6 and Figure-7 respectively for 45nm technology. The analog simulation has been performed and its

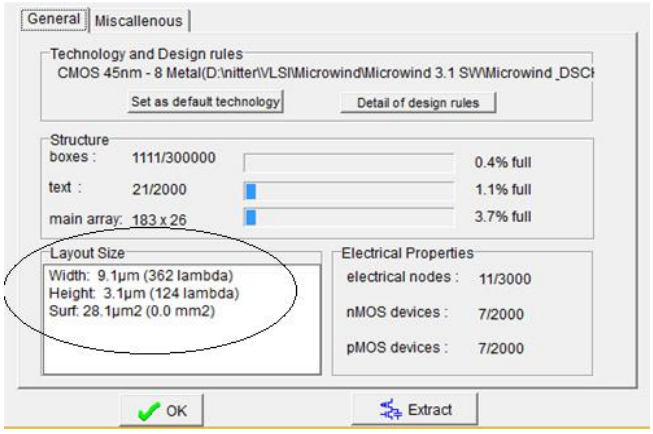

Figure-6 Total Area - XNOR-XOR using TG (45nm)

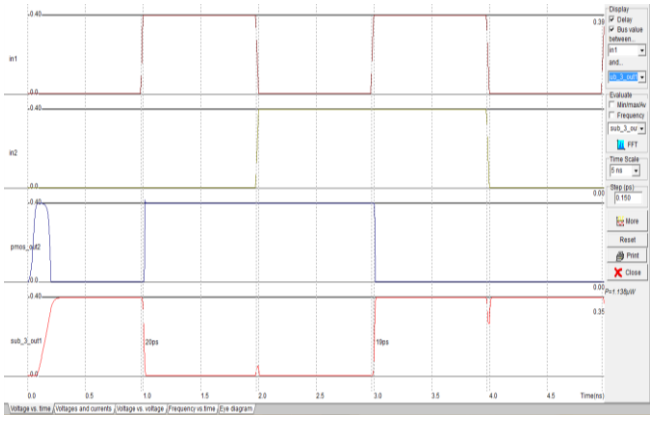

Figure-7 Layout Simulation

Table-2 Results Analysis

Parameters	**Proposed Design**
Power Consumption (uW)	1.139
Area (um2)	28.1
Delay (Ps)	19

results in term of power, area and speed are shown in Table-2. It shows that XNOR-XOR implementation using transmission gate technology is much better than XNOR-XOR implementation using CMOS. The performance of proposed design is Compared with Existing design[1] and Proposed design are shown in Table-3.

Table-3 Results Comparison

Parameter	**Existing Design** [1]	**Proposed Design**	**Improvement (%)**
Power Consumption (uW)	12.198	1.139	90.66
Area (um2)	41.7	28.1	63.97
Propagation Delay (Ps)	130	19	85.38

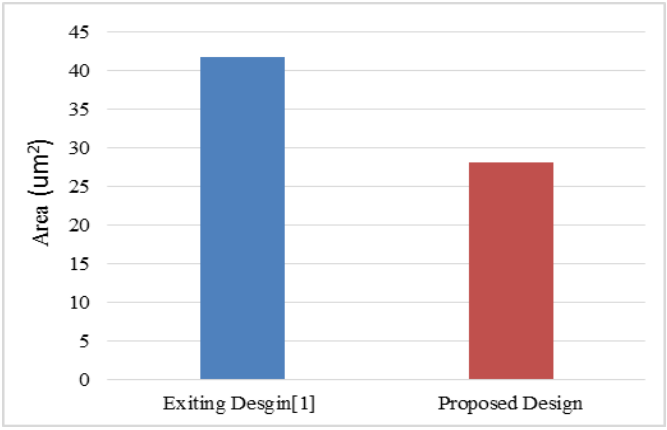

Figure-8 Area Required

Figure-8 shows the area graph in both designs technologies. It shows that for implementation of XNOR-XOR using transmission gate required 28.1um^2 area and exiting design required 41.7um^2 area.

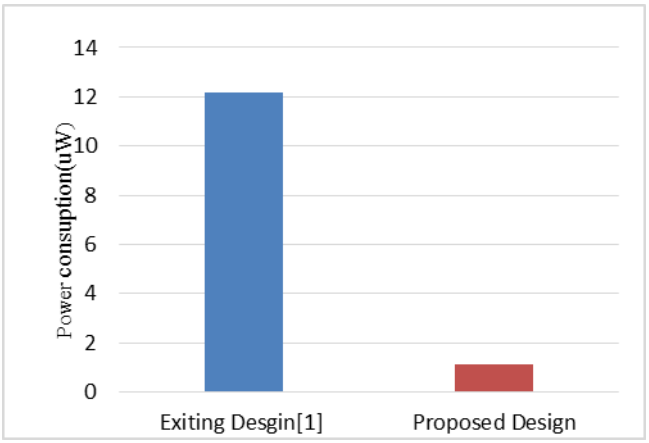

Figure-9 Power Consumption(uW)

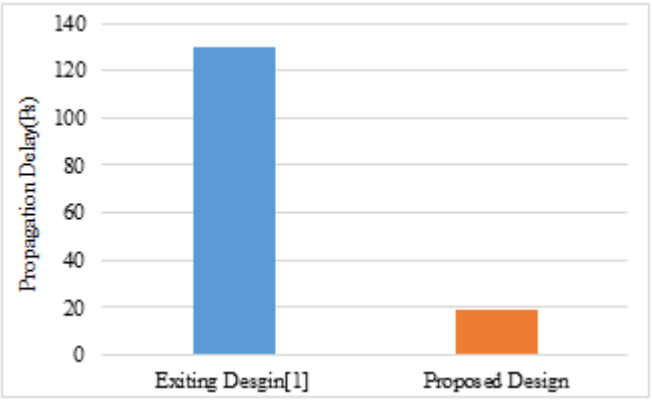

Figure-10 Propagation delay(Ps)

Figure-9 shows power consumption plots in uW for XNOR-XOR using transmission gate. Power consumption in XNOR-XOR using CMOS transmission gate consume 1.139uW, 12.198uW in proposed design and exiting design respectively. Figure-10 shows propagation delay in (Ps) for XNOR-XOR using transmission gate for proposed design and existing design. Which is 130ps for existing design and 19ps for proposed design.

V. CONCLUSION

Proposed XNOR-XOR using CMOS transmission gate is designed and simulated successfully in 45nm technology. The performance parameters are compared with existing design. From the result it is found that proposed design requires 63.97% less than existing design. Power consumption in XNOR-XOR using transmission gate consume 90.66% less in proposed design. Speed of proposed design is 85.38% fester then exiting design. The importance of the work or suggest applications and extensions.

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