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Implementation of Full Adder at One Terabyteper Second Speed Using Cadence

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***Abstract*— In digital circuits design high speed, high throughput and small silicon area and at the same time low power consumption of digital circuit is most important parameter for digital circuit designers. Most of the VLSI applications, such as image and video processing, digital signal processing and microprocessors extensively use arithmetic operations. Addition, subtraction, multiplication and accumulate are most commonly used operations. Adders are some of the most critical data path circuits requiring considerable design effort in order to squeeze out as much performance gain as possible. Various adder structures can be used to execute addition such as serial and parallel structures and most of researches have done research on the design of high-speed, low-area, or low-power adders. Adders like carry select adder, carry look ahead adder, carry skip adder, carry save adder etc exist numerous adder implementations each with good attributes.**

The main objective of this thesis is implementation of full adder at

one Terabyte per second speed. The simulation is done using Cadence and we have recorded the performance in propagating implementation of full adder at one terabyte per second. This thesis focuses on the implementation and simulation of 4 bit carry look-ahead adder, carry skip adder and carry select adder based on synthesis analysis and compared for their performance. Especially, this work focuses on the reduction of the power dissipation and implements high performance.

***Index Terms*— Carry look ahead adder (CLA), Carry skip adder (CSkA), Carry select adder (CSLA), Cadence.**

I. INTRODUCTION

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. We have come a long way from the single transistor era in 1958 to the present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip [1]. In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. We have come a long way from the single transistor era in 1958 to the present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip. For example, high-end microprocessors in 2010 are predicted to employ billions of transistors at clock rates over 30GHz to achieve TIPS (Tera Instructions per seconds) performance. With this rate, high-end microprocessor's power dissipation is projected to reach thousands of Watts. This thesis investigates one of the major sources of the power dissipation and proposes and evaluates the techniques to reduce the dissipation.

Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology.

Arithmetic circuits, like adders and multipliers, are one of the basic components in the design of communication circuits. Recently, an over whelming interest has been seen in the problems of designing digital systems for communication systems and digital signal processing with low power at no performance penalty. Designing low power high-speed arithmetic circuits requires a combination of techniques at four levels; algorithm, architecture, circuit and system levels. This thesis presents layout and simulations of a multiplication algorithm, which is suitable for high-performance and low–power applications.

II. THE SYNTHESIS OF A LOGIC CIRCUIT SHOULD HAVE FOLLOWING OPTIMIZATION PARAMETERS.

1. Minimum number of gates
2. Minimum number of garbage outputs
3. Minimum number of constant inputs
4. Minimum number of quantum costs

2.1 Adder Architecture And Power Analysis

Addition is a fundamental operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Adders are also very important component in digital system because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operation inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed.

2.2 Ripple Carry Adder (RCA)

These adders are simple in design and also they occupy less area. But they are constrained in their performance capabilities. For the modern day designs where high speed of operation is required, these adders fall short by a large extent as the delay through the adder chain to produce the output is very large. Hence, these adders are not very popular to be

implemented in the modern day designs. Because of their simplicity in design there are certain circuit implications which can be efficiently implemented using ripple carry adders.

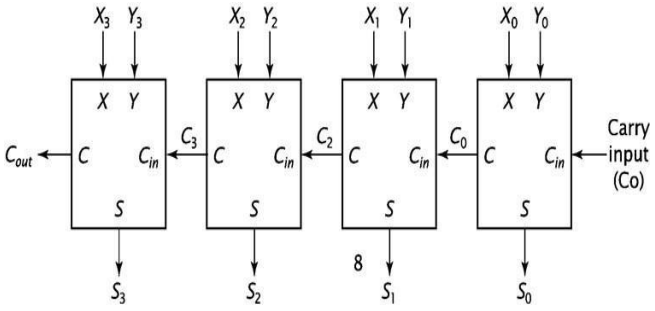


Figure2.1 Ripple Carry Adder

2.2 Carry look-ahead adders(CLA)

Carry look ahead logic uses the concepts of *generating* and *propagating* carries. Although in the context of a carry look ahead adder, it is most natural to think of generating and propagating in the context of binary addition, the concepts can be used more generally than this. In the descriptions below, the word *digit* can be replaced by *bit* when referring to binary addition.

Carry look ahead depends on two things:

1. Calculating, for each digit position, whether that position is going to propagate a carry if one comes in from the right.

2. Combining these calculated values to be able to deduce quickly whether, for each group of digits, that group is going to propagate a carry that comes in from the right

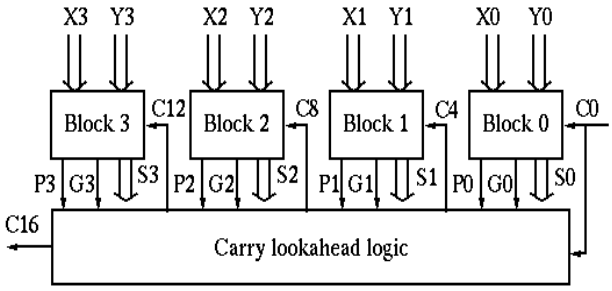


Figure2.2 Carry Look Ahead Adder

2.3 Carry Skip Adders (CSkA)

A carry-Skip consists of a simple ripple carry-adder with a special up carry chain called a skip chain. Carry skip adder is a fast adder compared to ripple carry adder. A carry-skip adder is designed to speed up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder.

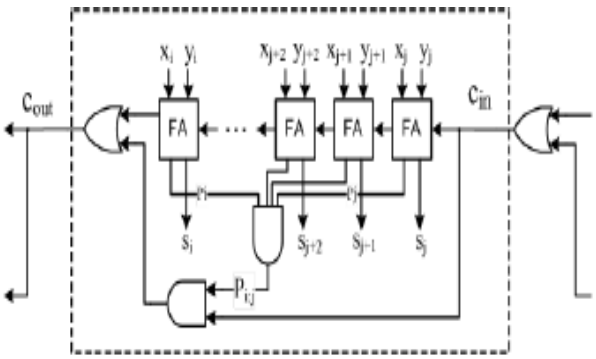


Figure2.3 Carry Skip Adder(CskA)

Carry Skip Mechanics

Boolean Equations

Carry Propagate: $P_i = A_i \oplus B_i$

Sum: $S_i = P_i \oplus C_i$

Carry out: $C_{i+1} = A_i B_i \oplus P_i C_i$

If $A_i = B_i$ then $P_i = 0$, making the carry out C_{i+1}, depends only on $A_i and\ B_i$

Then $C_{i+1} = A_i B_i$

$C_{i+1} = 0$, if $A_i = B_i = 0$ and $C_{i+1} = 1$,

if $A_i = B_i = 1$.

2.4 Carry Select Adders (CLSA)

Carry select adders are one of the other popular architectures which show improved performance over ripple carry adders. As in ripple carry adders they are popular for their regular layout structure. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The conventional carry select adder consists of k/2bit adder for the lower half of the bits i.e. least significant bitsand for the upper half i.e. most significant bits (MSB's) two k/bit adders. In MSB adders one adder assumes carry input as one for performing addition and another assumes carry input as zero. The carry out calculated from the last stage i.e. least significantbit stage is used to select the actual calculated values of outputcarry and sum. The selection is done by using a multiplexer.

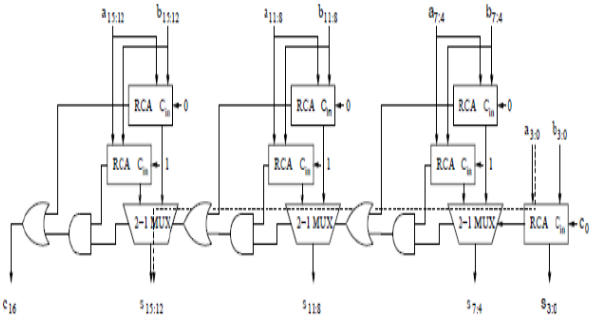


Figure2.4 Carry Select Adder Implementation with 4 blocks

2.5 Power Dissipation

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its input. The D.C or average power dissipation is the product of D.C supply voltage and the mean current taken from the supply. Ideally, CMOS circuits dissipate no static (DC) power, since in the steady state there is no direct path from VDD to ground. There are always leakage currents and substrate injection currents which leads to static power dissipation in CMOS circuits .One of the dynamic components of power dissipation arises from the transient switching behavior of the CMOS devices. At some point during the switching transient, both the NMOS and PMOS devices are on and a short circuit current exists between VDD and ground. Another component

of dynamic power dissipation is charging and discharging of parasitic capacitances which consume most of the power used in CMOS circuits. This leads to the conclusion that CMOS power consumption depends on the switching activity of the signals involved. If we show the switching activity by a parameter α, then we can compute the whole power dissipation through the following equation-

$$P = \alpha C_L V_{DD}^2 f_{clk} + (I_{SC} + I_{leakage}) V_{DD}$$

2.6 Propagation Delay and Power Delay

The propagation delay, can be defined as time required to reach 0.5VDD of output from the 0.5VDD of input. The propagation delays of CLA are measured in the order of nanosecond.

Power Delay Product is the product of average power dissipation to the propagation delay ((PDP=average power consumed * propagation delay), in fJ ($10^{\wedge -15}$)).

III. Implementation of Carry Look Ahead Adder

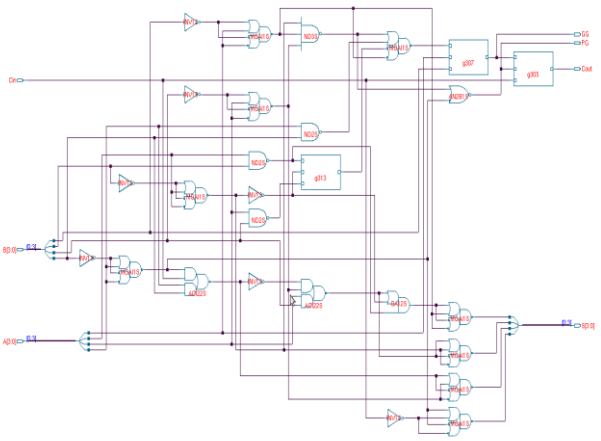
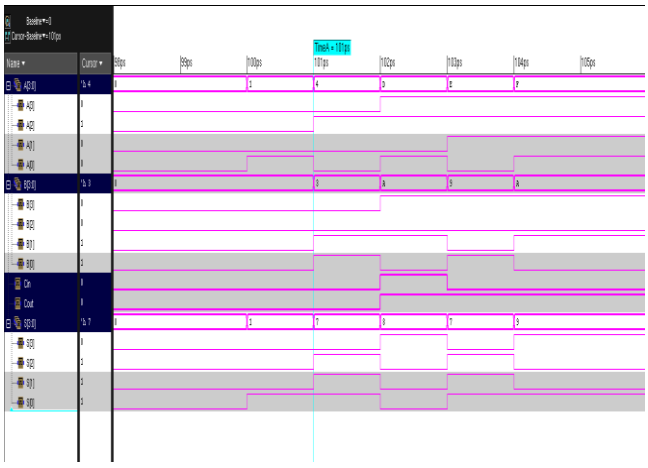


Figure 3 RTL diagram of carry look ahead.

Observation Result

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
CLA_4bit	27	31.253	30199.803	30231.056



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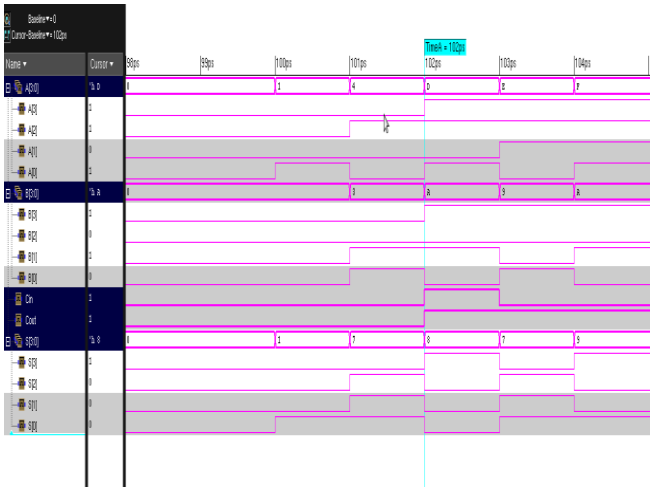

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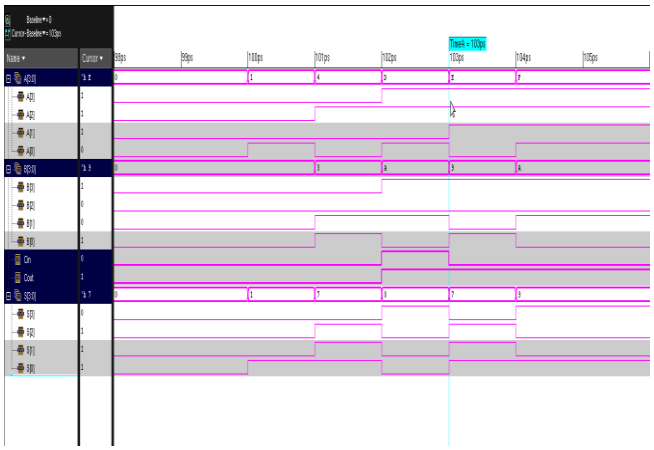


(c)

IV. Implementation of Carry Skip Adder

- RTL Diagram

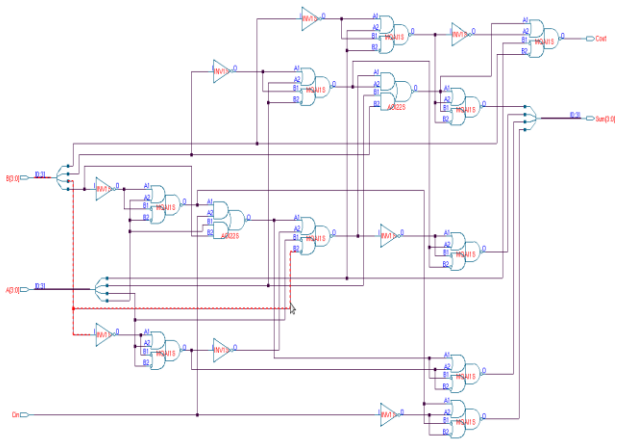
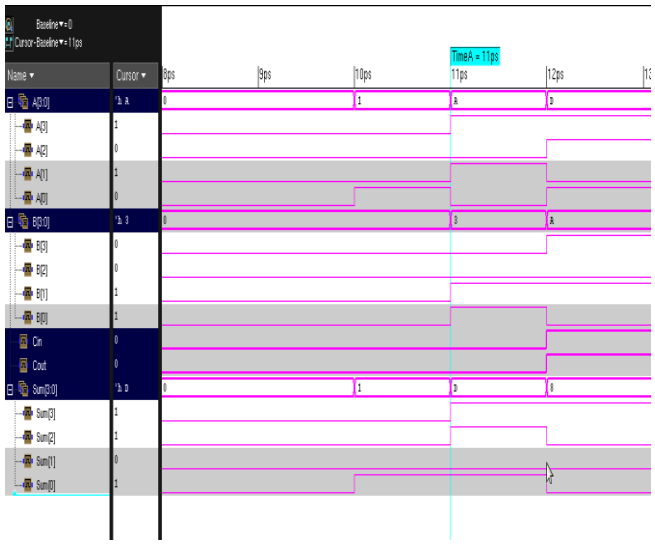


Figure 4 RTL diagram of carry skip adder

Instance	Cells	Leakage Power (nW)	Dynamic Power(nW)	Total Power(nW)
ripple_adder_4bit	20	23.707	22702.732	22726.439

- Simulation observation



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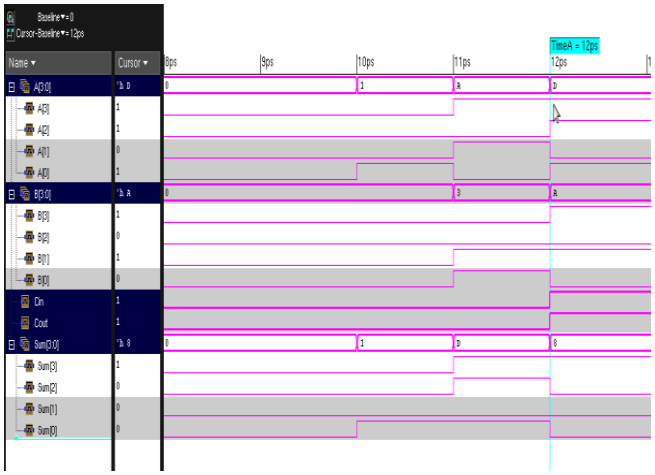

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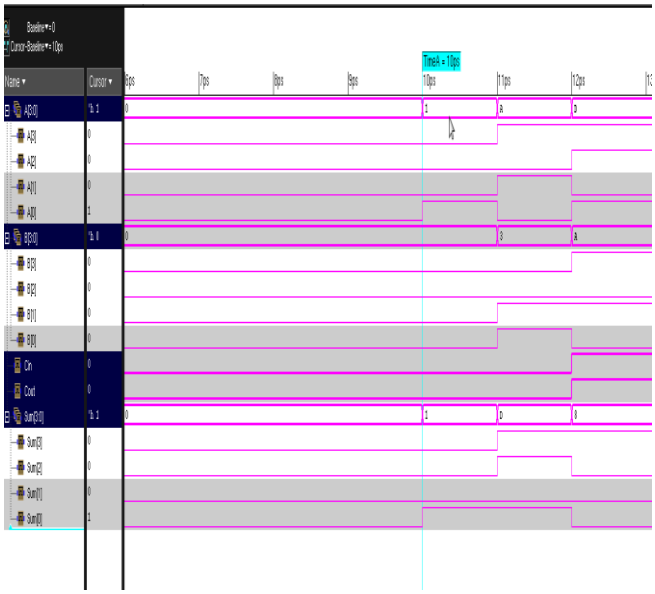


(c)

Figure 5.4 Simulation diagram of carry skip adder implemented with 1 terabyte

V. IMPLEMENTATION OF CARRY SELECT ADDER

- RTL Diagram

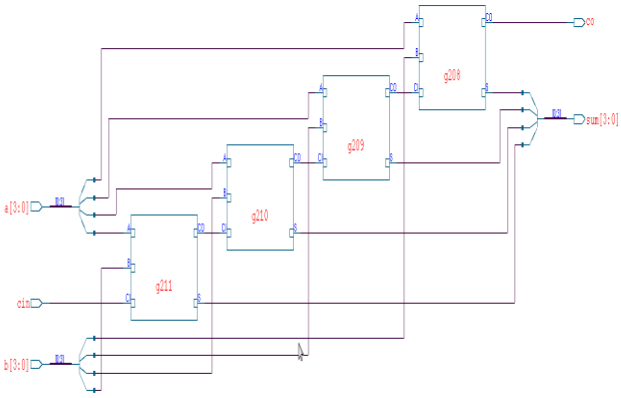
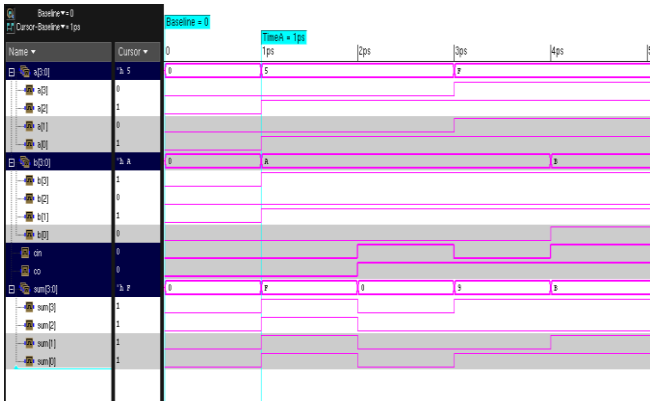


Figure 5 RTL diagram of carry select adder

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
Carry select	4	13.740	12072.916	12086.655

- Simulation observation



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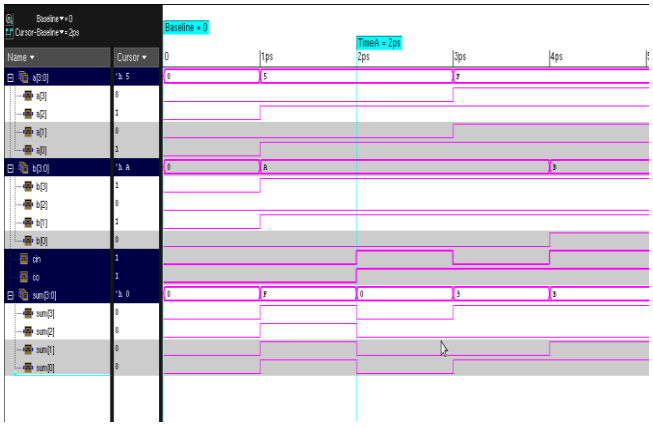

(b)

VI. CONCLUSION

The Full Adder was successfully demonstrated by cadence. Performance of all architecture of full adder is verified through simulation. The proposed full adder design has a simpler structure which can be used for cadence. The simulated system has the prospective to operate at 1 Tb/s and can be used for high speed optical networks, opamp circuits, and adaptive filter implementation and in all-optical computing as well in future.

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