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Analytical Model for Surface Potential and Inversion Charge of Dual Material Double Gate Son MOSFET

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Abstract— **A simple analytical model of a nanoscale fully depleted dual- material gate (DMG) SOI and SON MOSFETs has been developed and their performance comparison analysis is presented in this paper. An analytical model for the surface potential and threshold voltage has been developed both for these structures using a generalized 2D Poisson's equation solution. The DMG SON MOSFET technology is found to have more potential against various short channel effects (SCEs) thereby offering further device scalability with improved immunity.**

Double-gate MOSFETs seem to be a very promising option for ultimate scaling of CMOS technology. Excellent short-channel effect (SCE) immunity, high transconductance, and ideal sub threshold performance • have been reported from theoretical and experimental work on this device. In particular, asymmetrical DG SOI MOSFETs are becoming popular since these structures provide a desirable threshold voltage unlike symmetrical DG SOI MOSFETs. To enhance the immunity against SCEs, a new structure called a dual-material (DMG) gate MOSFET has been proposed. A dual-material gate structure induces the peak of the electric field at the interface between the different materials, which enhances the carrier's speed and improves the device's performance. In the era of VLSI/ ULSI, with the aim of fabricating low power, high speed and energy efficient devices, silicon on insulator (SOI) technology has been recognized as a favorable solution for enhancing the performance of CMOS because of their several advantages over traditional bulk CMOS technology in terms of higher speed, lower power dissipation, high radiation tolerance, lower parasitic capacitance and lower short channel effects. But, this technology has been cursed by two most crucial disadvantages like threshold voltage roll-off and DIBL which have been moderated with the introduction of a modified SOI structure, i.e., Silicon on Nothing (SON) where the thick buried oxide layer is replaced with "nothing" layer. Due to the lower dielectric permittivity of "nothing" or air layer and diminished electrostatic coupling between channel and source/ drain, the SON structure becomes a promising candidate for high speed and low power circuits.

Index Terms— **SOI/SON MOSFET, Threshold Voltage, Short Channel Effect, DIBL.**

I. INTRODUCTION

Nowadays, it is becoming painful for the device engineers to further improve device performance and reliability only through traditional scaling and it is now obvious that conventional scaling trend cannot continue indefinitely. To resolve this crucial issue, the engineers had to switch to new innovative device structures for low power, high speed applications to maintain the increased rate of performance. The continuous scaling of gate length in MOSFETs throws a bunch of tough challenges in front of the researchers as leakage current and SCEs increase due to decreasing gate control over the channel. The major problems associated with this continuous device miniaturization in sub-micron and nanometre regime are reliability issues, direct tunnelling, gate depletion, boron penetration and most importantly the short-channel effects (SCEs) such as Drain-Induced Barrier Lowering (DIBL), Hot carrier effect (HCE), Sub threshold conduction, junction leakages etc. The Drain-Induced-Barrier-Lowering (DIBL), threshold voltage roll-off, poor sub threshold swing are examples of the short channel effects. Degraded threshold voltage (V_{TH}) from scaling causes early channel conduction and leads to a lower noise margin and off-state leakage.

To solve these problems, a number of attractive device structures such as full depleted silicon on insulator (FD-SOI) MOSFETs, double gate (DG) MOSFETs, multigate SOI MOSFETs (MuGFETs), and junction less double (JLDG) SOI MOSFETs have been already reported in the existing literature. Among those, a junction less double gate (JLDG) SOI MOSFETs has been considered as a more promising candidate in the aspect of future technology. Multiple gate transistors are powerful candidates for ultimate scaled devices due to their robustness against SCEs and higher current driving capability. But, these devices face critical issues during fabrication like abrupt doping concentration gradients and low thermal budgets. To alleviate these process challenges, junction less transistors have been proposed as an alternative device structure which is composed of homogeneously doped source, drain and channel regions with uniform doping concentration.

II. MOSFET DEVICE STRUCTURE

A metal-oxide semiconductor field effect transistor (MOSFET) is a semiconductor device based on a silicon substrate that is used in almost every electronic device today to amplify and switch electrical signals. Because of the high scalability of the MOSFET it is the basic element in Very Large Scale Integrated (VLSI) circuits. These circuits are also known as Integrated Circuits or microprocessors and they are what make things like cell phones and personal computers possible today. Compared to the bipolar junction transistor, the MOS transistor occupies a relatively smaller silicon area, and its fabrication used to involve fewer processing steps. These technological advantages, together with the relative simplicity of MOSFET operation, have helped make the

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MOS transistor the most widely used switching device in LSI and VLSI circuits.

The MOSFET device is constructed like a sandwich containing layers of materials with different electrical properties. The bulk of the MOSFET is called the substrate and can be a number of different materials, but the important thing is that it can be ―doped‖. The doping procedure involves adding other elements like arsenic or gallium to change the availability of electrons or holes. The structure consists of three layers: the metal gate electrode, the insulating oxide (SiO_2) layer, and the p-type bulk semiconductor (Si), called the substrate. As such, the MOS structure forms a capacitor, with the gate and the substrate acting as the two terminals (plates) and the oxide layer as the dielectric. Figure 1 shows cut away of the basic MOSFET showing the three terminals and the substrate. The channel is where the actual manipulation of electrical signals is accomplished and is where the ―field effect‖ part of the name comes from.

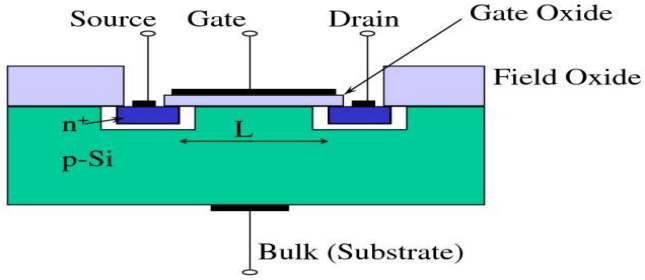


Figure 1 Basic structure of a N channel MOSFET

III. JLDG SON MOSFET MODEL

Junctionless (JL) double gate (DG) MOSFET is recently emerging as more promising and superior option to conventional junction based MOSFET structure. It has the same structure as a conventional DG-MOSFET except for the homogeneously doped body from a source via a channel to the drain. Such a junctionless structure exhibits simple fabrication process because of the absence of junction engineering, smaller Drain Induced Barrier Lowering (DIBL) effect, nearly ideal subthreshold slope (SS) and high on-off current ratio.

In a short channel device, potential distribution in the channel region is purely two-dimensional in nature [3.12]. The channel region is assumed to be perfectly depleted in the subthreshold operation regime. The potential profile and hence short channel threshold voltage of the proposed device can be calculated by solving 2-D Poisson‘s equation in the channel region [3.13].The 2D Poisson‘s equation for N-channel junctionless double gate (JLDG) SON MOSFET can be expressed as,

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = \frac{-qN_d}{\varepsilon_{si}}$$

where Φ(x, y) is the two dimensional potential profile in the channel, N_d is the uniform doping concentration of the channel and ε_{si} is the dielectric constant of silicon. Considering Young‘s parabolic potential profile [3.14] in the channel, can be written as,

$$\phi(x,y) = C_1(x) + C_2(x)\,y + C_3(x)\,y^2$$

Depending on the continuity of electrostatic potential, the boundary conditions used here are described below:

The central potential, $\Phi_c(x)$ is a function of x only.

$$\phi(x,0) = C_1(x) = \phi_C(x)$$

The electric field at $y = \frac{t_{si}}{2}$ is determined by the gate and the oxide thickness.

$$\left.\frac{\partial \phi(x,y)}{\partial y}\right|_{y=\frac{t_s}{2}} = -i = -\frac{\varepsilon_{ox}}{t_{ox}}\left(\phi_f(x) - V_{gs} + V_{fb}\right)$$

The electric field at $y = \frac{t_{si}}{2}$ is determined by the gate and the air thickness.

$$\left.\frac{\partial \phi(x,y)}{\partial y}\right|_{y=-\frac{t_{si}}{2}} = \frac{\varepsilon_{air}}{\varepsilon_{si}}\frac{\phi_b(x) - V_{gs} + V_{fb}}{t_{air}}$$

where $\Phi_f(x)$ and $\Phi_b(x)$ are the front surface and the back surface potential respectively. V_{gs} represents gate to source voltage while V_{fb} denotes flat band voltage at the interface of the silicon film and gate electrode.

$$\phi_f(x) = \phi_c(x) + C_2(x)\frac{t_{si}}{2} + C_3(x)\frac{t_{si}^2}{4}$$

$$\phi_b(x) = \phi_c(x) - C_2(x)\frac{t_{si}}{2} + C_3(x)\frac{t_{si}^2}{4}$$

We get $C_2(x)$ and $C_3(x)$. The front surface potential is obtained by substituting the expressions of $C_2(x)$ and $C_3(x)$.

$$\phi_f(x) = \frac{\phi_c(x) + (V_{gs} - V_{fb})\dfrac{3C_{ox}C_{si} + C_{ox}C_{air} - C_{air}C_{si}}{8C_{si}^2 + 4C_{air}C_{si}}}{\dfrac{8C_{si}^2 + 3C_{ox}C_{si} + 3C_{si}C_{ox} + C_{ox}C_{air}}{8C_{si}^2 + 4C_{air}C_{si}}}$$

Similarly, by substituting $C_2(x)$ and $C_3(x)$, the back surface potential can be expressed as,

$$\phi_b(x) = \frac{\phi_c(x) + (V_{gs} - V_{fb})\dfrac{3C_{air}C_{si} - C_{ox}C_{si} + C_{air}C_{ox}}{8C_{si}^2 + 4C_{ox}C_{si}}}{\dfrac{8C_{si}^2 + 3C_{air}C_{si} + 3C_{ox}C_{si} + C_{ox}C_{air}}{8C_{si}^2 + 4C_{ox}C_{si}}}$$

Now, twice with respect to x and y and putting the values of $C_1(x)$, $C_2(x)$ and $C_3(x)$ obtained previously, Substituting surface potential in terms of central potential, we get the simplified scaling equation as reported in:

$$\frac{\partial^2 \phi_c(x)}{\partial x^2} - \frac{1}{\lambda_c^2}\left(\phi_c(x) - \Phi_C\right) = 0$$

$$\frac{1}{\lambda_c^2} = \frac{8C_{si}^2(C_{air} + C_{ox}) + 8C_{air}C_{ox}C_{si}}{t_{si}\varepsilon_{si}\left(8C_{si}^2 + C_{air}C_{ox} + 3C_{ox}C_{si} + 3C_{air}C_{si}\right)}$$

$$\Phi_C = V_{gs} - \omega_1$$

With

$$\omega_1 = V_{fb} - \frac{qNt_{si}(8C_{si}^2 + C_{air}C_{ox} + 3C_{ox}C_{si} + 3C_{air}C_{si})}{8C_{si}^2(C_{air} + C_{ox}) + 8C_{air}C_{ox}C_{si}}$$

$$\frac{\partial^2 \phi_f(x)}{\partial x^2} - \frac{1}{\lambda_f^2}(\phi_f(x) - \Phi_f) = 0$$

where λ_f and Φ_f , both stand for surface potential, defined as,

$$\frac{1}{\lambda_f^2} = \frac{2(C_{air}C_{ox} + C_{ox}C_{si} + C_{air}C_{si})}{t_{si}\varepsilon_{si}(2C_{ox} + C_{air})}$$

By setting minimum central potential ($\square_{C,min}$) to zero and solving for gate to source voltage, V_{gs}, the threshold voltage for JLDG SON MOSFETs is as follows:

$$V_{th} = \frac{(\omega_1 + 2PS + 2QR) \pm \sqrt{(\omega_1 + 2PS + 2QR)^2 - (1-4PR)(\omega_1^2 - 4QS)}}{(1-4PR)}$$

IV. ANALYTICAL MODELING

The conventional Bulk CMOS technology belonging to sub-micron regime could not overcome this fundamental physical limitation [1] which leads to a several non-conventional geometry MOS technology, among which fully depleted silicon-on-insulator (FDSOI) MOSFET has got more attention to the researchers. The reduced coupling effect of channel with source/drain and substrate in FD SOI structure initiates less SCEs thereby allowing the further device miniaturization [2]. Though FD SOI is better candidate for future MOSFET technology, there are some serious issues like growth technique of buried oxide, control of buried layer thickness etc.

Various SCEs can be reduced by introducing a new structure called a dual-material gate (DMG) MOSFET [5]. The DMG MOSFET structure has two metals M1 and M2 of different work functions ΦM1 and ΦM2 respectively. These two metals are placed together side by side forming a single gate electrode and provide a step in the surface potential profile, which thereby increases the drain current characteristics and suppresses various SCEs.

A schematic cross-sectional view of a generalized layered structure of fully depleted SOI/SON MOSFET is shown in Figure 2 with gate metals M1 and M2 of lengths L1 and L2, respectively.

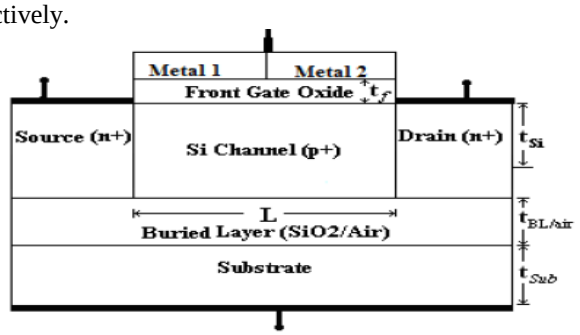


Figure 2 Structure of DMG SOI/SON-MOSFET with metal 1 and metal2

V. RESULTS

The theoretical calculation for threshold voltage (V_{th}) model of a junctionless double gate (JLDG) SON MOSFETs. The long-channel behavior of the structure shown in figure 3 clearly shows that the potential is flat and independent of the variation of V_{ds}, but as the device is shortened into the submicron regime the nature of the potential is highly dependent on V_{ds} which exhibits the short-channel behavior.

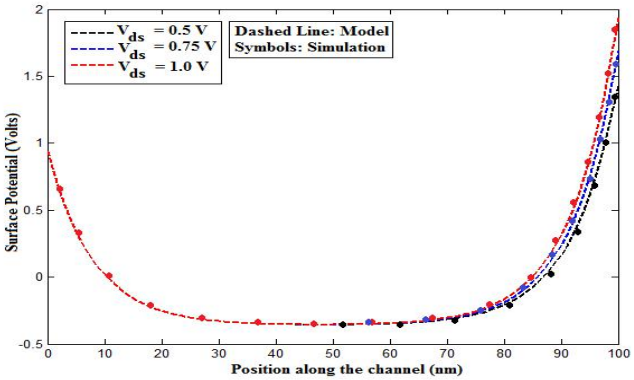


Figure 3 Long-channel surface potential distribution with respect to the position in the channel. The parameter V_{gs} is kept constant to 0.1V and V_{ds} is varied.

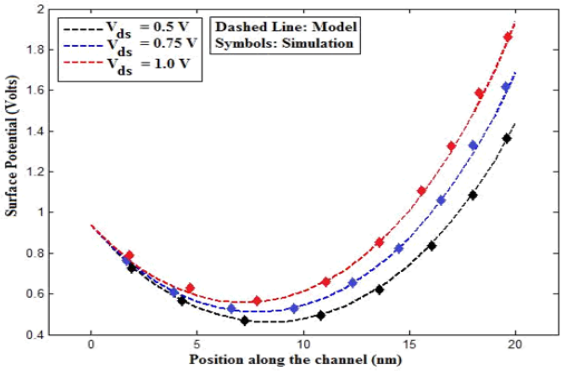


Figure 4 Short-channel surface potential distributions with respect to the position in the channel. The parameter V_{gs} is kept constant to 0.1V and V_{ds} is varied

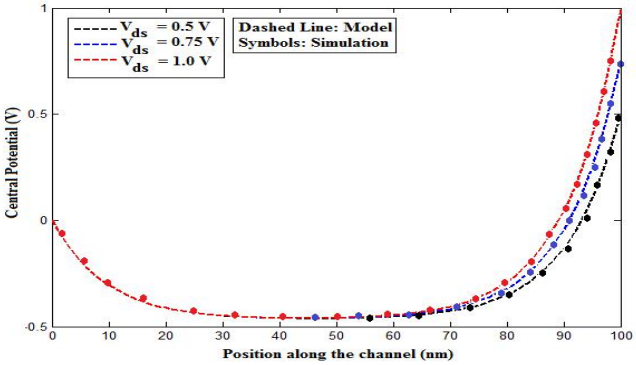


Figure 5 Long-channel central potential distribution along the channel length direction at various drain voltages and V_{gs} is kept constant at 0.1 V

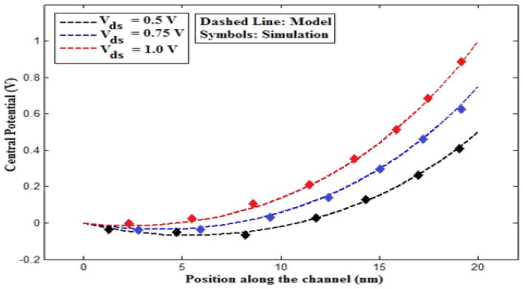


Figure 6 Short-channel central potential distribution along the channel length direction at various drain voltages and V_{gs} is kept constant at 0.1 V

It is observed that the minimum potential point gives an upward movement with increasing of drain voltage. This shift in the value of the central potential minimum with varying drain voltage proves the presence of DIBL effect. Figure 7 illustrates the dependency of the threshold voltage on the channel length at V_{ds} = 0.1 V with identical parameters as described below.

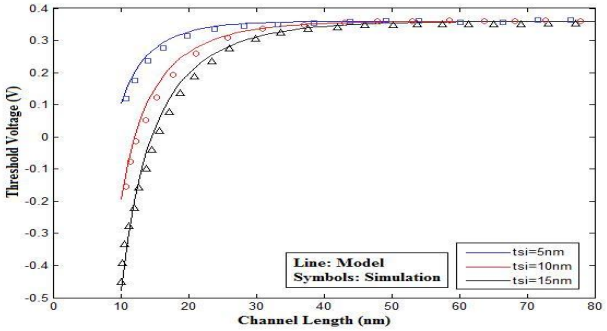


Figure 7 Threshold voltage vs. channel length at V_{ds} = 0.1 V for different silicon body thicknesses

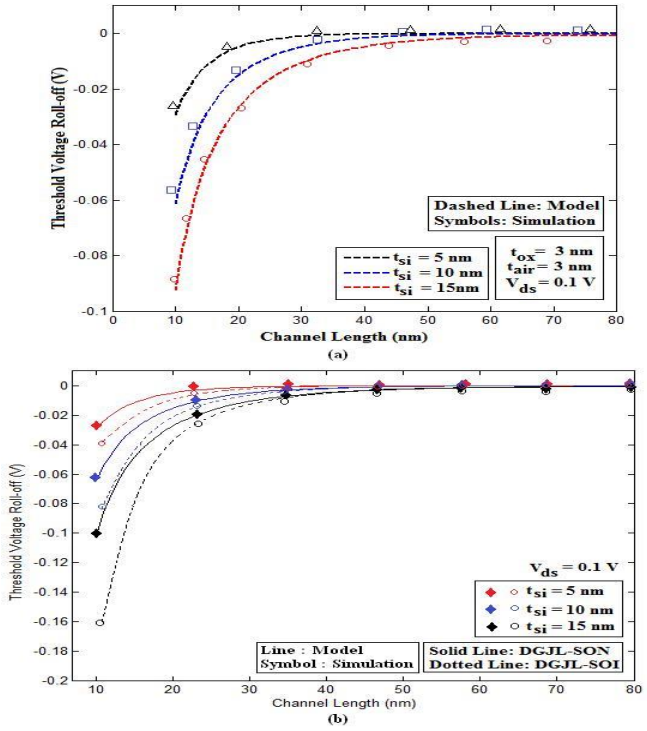
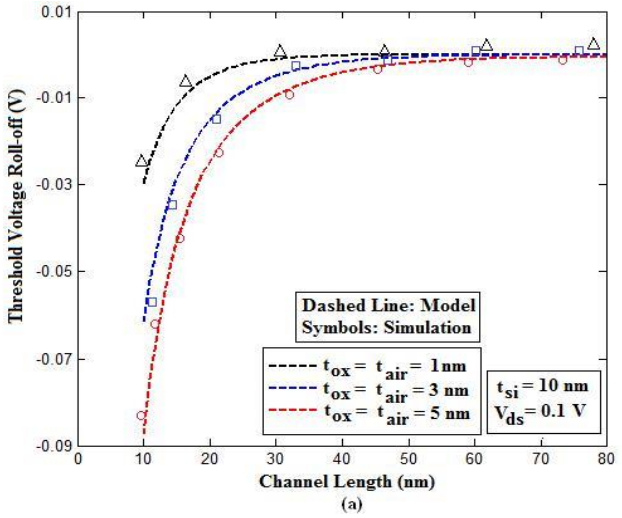


Figure 8 Variation of the V_{th} roll-off along the channel length for different silicon film thicknesses



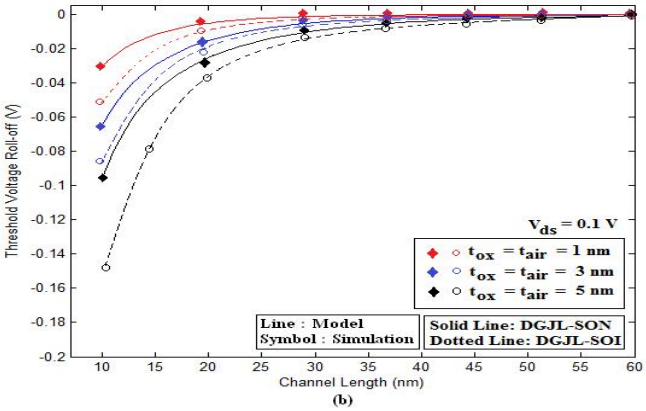


Figure 9 Variation of the V_{th} roll-off along the channel length for different gate oxide (air) thicknesses

As the channel length (L) is diminished below 30nm, the DIBL issue will become more prominent for each case. The figure 10 indicates that low drain bias can effectively suppress DIBL.

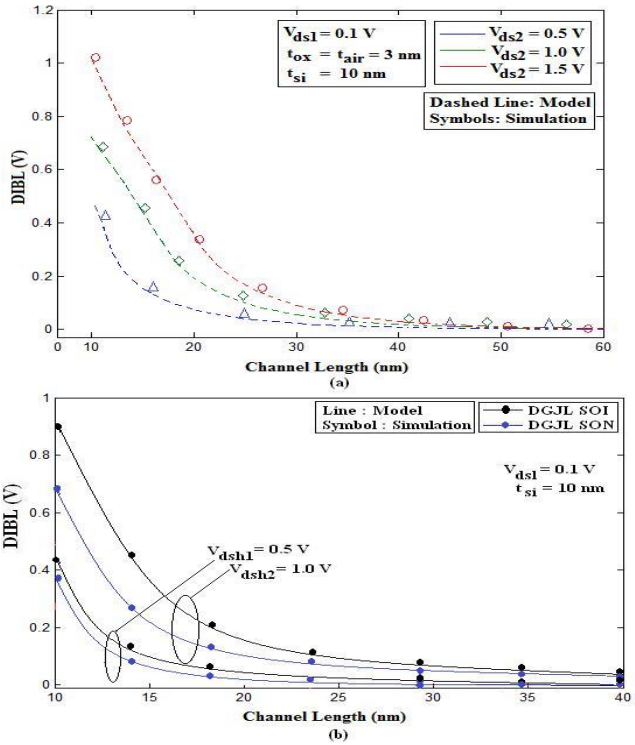


Figure 10 DIBL change with channel length for different drain biases

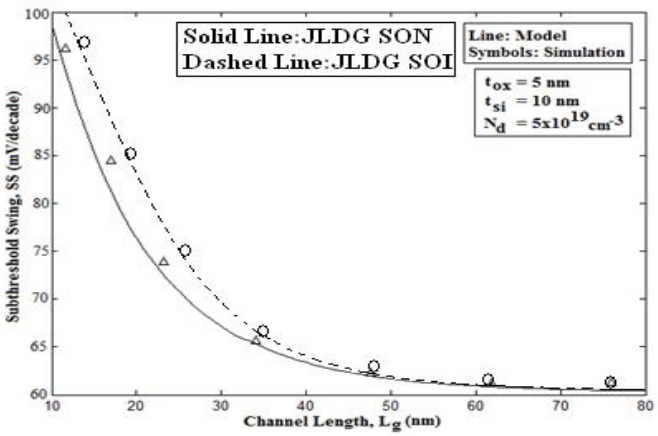


Figure 11 Subthreshold swing deviation with the channel length

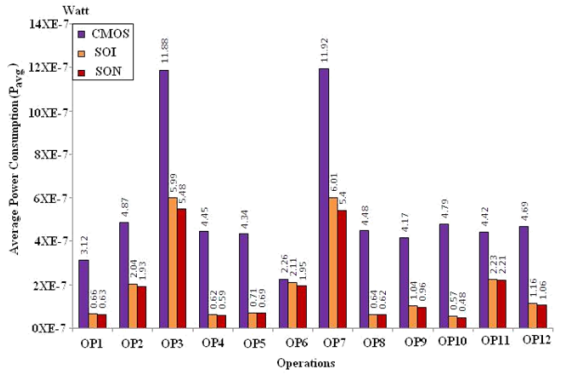


Figure 12 Details of Average Power Consumption

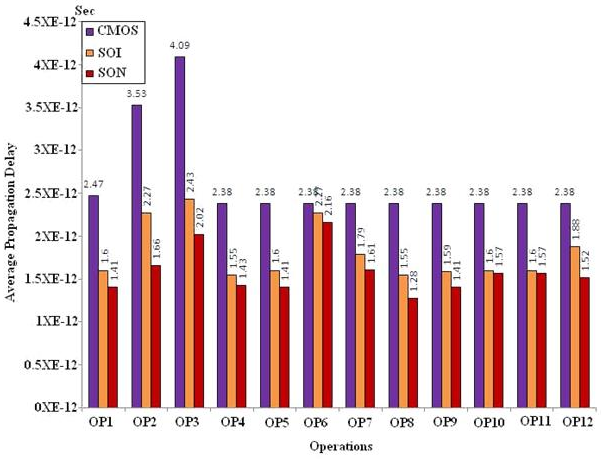


Figure 13 Details of Average Propagation Delay

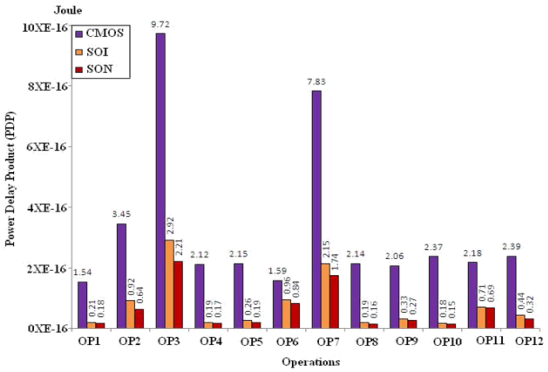


Figure 14 Details of Power Delay Product (PDP)

VI. CONCLUSION

In this paper, we have developed an expression for surface potential of short channel junction-less double gate (JLDG). MOSFET by solving 2-D Poisson's equation. A comparison of analytical solution with numerical solution using ATLAS device simulator provided good approximation of the model. It can be observed through results that the JLDG MOSFET provides higher immunity to SCEs as compared to junction based DG MOSFET. The results clarified that in a JLDG MOSFET, the doping concentration affects the DIBL, sub-threshold swing and ION/IOFF ratio. Further, in this paper we have investigated the various analog/RF Figure of merits such as gm, gd, VEA, AV, TGF, fT, GFP, TFP and GTFP. The peak values of these analog/RF FOMs conclude that the JLDG device have bright future for ultra low power and high frequency analog/ RF applications.

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