

Analytical Model for Surface Potential and Inversion Charge of Dual Material Double Gate Son MOSFET: A Survey

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Abstract— Double-gate MOSFETs seem to be a very promising option for ultimate scaling of CMOS technology. Excellent short-channel effect (SCE) immunity, high transconductance, and ideal subthreshold performance have been reported from theoretical and experimental work on this device. Silicon-on-Insulator (SOI) technology can be considered as an alternative to conventional bulk MOSFET which can perform in a better way as expected from next generation Si technology. The continuous shrinking of Metal Oxide Semiconductor (MOS) device technology is facing countless challenges which have inspired the Engineers to focus on other promising devices. With the objective of diminishing different short channel effects (SCEs), various multigate devices have been proposed and are accounted to play a very vital role in deep submicron era due to better electrostatic control. Moreover, for transistor with reduced dimensions, it is very much troublesome to create ultra-sharp junctions in source/ drain, avoiding diffusion of impurities into the channel. This will enhance the complexity of fabrication process and hence further miniaturization is becoming a decisive challenge for device Engineers. Junctionless transistors with their pronounced electrostatic properties are flourished with the purpose to provide a partial solution for the above said challenging issue. Presently, double gate (DG) MOSFETs appear to be very convincing candidate for intense scaling of CMOS technology due to their excellent SCEs immunity, high transconductance and ideal subthreshold swing.

Index Terms— SOI/SON MOSFET, Threshold Voltage, Short Channel Effect, DIBL, dual material gate, double-gate MOSFET, strained-Si, short-channel effect;

I. INTRODUCTION

The Semiconductor Industry was born in the 70s as a component industry with two main business drivers. The first consisted in providing more cost effective memory devices to the computer industry. The second consisted in timely production of application specific integrated circuits (ASIC) to any company that required very specific functionalities to realize novel products. Customers demanded pin-out and functionality standardization for memory devices while ASIC products were typically customer specific. Logic devices reprogrammable by software (e.g., microprocessors) were developed to minimize cycle time of ASIC devices. With all this talk of transistors the average technician or computer user may not understand what the figures mean; a simpler way to explain is that the earlier CPUs on the market had a single speed or frequency rating while the newer models have a

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rating which refers to more than one CPU. If we have purchased a computer recently you might have an idea of what this means as salespersons may have sold you on the wonders of multi-core CPUs. To solve these problems, a number of attractive device structures such as full depleted silicon on insulator (FD-SOI) MOSFETs, double gate (DG) MOSFETs, multigate SOI MOSFETs (MuGFETs), and junction less double (JLDG) SOI MOSFETs have been already reported in the existing literature. Among those, a junction less double gate (JLDG) SOI MOSFETs has been considered as a more promising candidate in the aspect of future technology. Multiple gate transistors are powerful candidates for ultimate scaled devices due to their robustness against SCEs and higher current driving capability. But, these devices face critical issues during fabrication like abrupt doping concentration gradients and low thermal budgets. To alleviate these process challenges, junction less transistors have been proposed as an alternative device structure which is composed of homogeneously doped source, drain and channel regions with uniform doping concentration

II. LITERATURE REVIEW

Downscaling of MOSFET dimensions has been very aggressive over recent few years. A number of studies have been devoted to the nonconventional silicon devices due to their compatibility with standard silicon processing and their potential to achieve much better performance because of the highly improved electrical properties.

In the early 1990s, SOI development began in the Advanced Silicon Technology Centre (ASTC) of the IBM Microelectronics Division, with the aim of assessment and development of SOI CMOS. In 1993, the value of the surface potential at threshold in fully depleted transistors is obtained analytically in terms of device dimensions, film doping level, and applied voltages by Mazharietal. On the other hand, in 1997, based on the studies of Shuretal, Long et. al. proposed a new structure called Dual material gate field effect transistor (DMGFET) where the gate was constituted two materials having different work functions placed side by side touching each other In 2000, Jurczaket al proposed a novel CMOS device architecture called silicon on nothing (SON), which allows extremely thin (in the order of a few nanometres) buried dielectrics and silicon films to be fabricated with high resolution and uniformity guaranteed by epitaxial process. In the next year, W. Wu et al have developed a model for partially depleted (PD) SOI MOSFET using a surface potential based approach. This model has been formulated within the framework of the latest industry standard bulk type MOSFET model. Again the researchers presented a simulation study of analog circuit performance parameters for a symmetric

double-gate junction less transistor (DGJLT) using dual-material gate along with high- k spacer dielectric (DMG-SP) on both sides of the gate oxides of the device.

In 1988, the reduction of kink effect in thin-film SOI MOSFETs has been suggested by J. Colinge [1]. In 1989, a true two-dimensional short-channel analytical threshold voltage model for fully depleted SOI MOSFET, based on the solution of 2D Poisson's equation was proposed by K K Young [2]. In 1989, short-channel effects in thin-film silicon-on-insulator (SOI) MOSFETs has been shown to be unique because of dependences on film thickness and body and back-gate (substrate) biases in [3]. Analytical models of subthreshold swing and threshold voltage for thin- and ultra-thin-film SOI MOSFETs has been thoroughly discussed in the next year [4]. In 1990, J. Colinge et al. described the process fabrication and the electrical characteristics of an SOI (silicon-on-insulator) MOSFET with gate oxide and a gate electrode not only on top of the active silicon film but also underneath it [5]. A threshold voltage instability phenomenon at low temperatures in partially depleted thin-film silicon-on-insulator (SOI) SIMOX (separation by implantation of oxygen) MOSFETs was reported in 1991 [6]. In the same year, an analytical model including the semiconducting substrate effect for silicon-on-insulator (SOI) MOSFET threshold and subthreshold operation was presented [7]. This year, floating-body effects triggered by impact ionization in fully depleted submicrometer silicon-on-insulator (SOI) MOSFETs were analyzed based on two-dimensional device simulations by J. Y. Choi et al. [8]. Yan et al. [9], in the year 1992, suggested some guidelines for designing SOI MOSFETs. In the next year, Suzuki et al. [10] proposed another scaling theory for double gate SOI MOSFET.

In 1995, Suzuki et al. aimed analytical models for n+-p+ double-gate SOI MOSFET's [11]. In this year, threshold voltage model for deep-submicrometer fully depleted SOI MOSFET's [12] was offered by Banna et al. The behavior of transients in the drain current of partially-depleted (PD) SOI MOSFET's down was examined as a function of drain bias [13] in 1995. Fossum et al. [14] measured current-voltage characteristics of scaled, floating-body, fully depleted (FD) SOI MOSFET's that show subthreshold kinks controlled by the back-gate (substrate) bias. A new model for the non-fully depleted (NFD) SOI MOSFET was developed and used to study floating-body effects in SOI CMOS circuits [15]. In 1997, Pong-Fei Lu et al. [16] presented a detailed study on the impact of a floating body in partially depleted (PD) silicon-on-insulator (SOI) MOSFET's on various CMOS circuits.

On the other hand, in 1997, based on the studies of Shuret. al., Long et. al. [17] proposed a new structure called Dual material gate field effect transistor (DMGFET) where the gate was constituted two materials having different work functions placed side by side touching each other. In this novel structure, the threshold voltage near drain end is found to be more negative than that in the source end, thereby brings in a shielding effect which reduces the SCEs. The use of two different materials as a single gate introduces a discontinuity in the field distribution in the channel which subsequently enhances the carrier transport and suppresses the SCEs. Jeffrey W. Sleight et. al., in 1998, presented a fully continuous compact model for circuit simulations which

automatically accounts for the correct body depletion condition. Unlike previously reported models which have been derived for either fully-depleted (FD) or partially-depleted (PD) devices, their model has the flexibility as it accounts the transitions between FD and PD behavior during the device operation.

III. SOI MOSFET

The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling. It is expected that the operational characteristics of the MOS transistor will change with the reduction of its dimensions. The term SOI means Silicon on Insulator structure, which consists of devices on silicon thin film (SOI layers) that exists on insulating film. In the case of bulk CMOS devices, P/N type MOS transistors are isolated from the well layer. In Silicon on Insulator (SOI) Fabrication technology Transistors are built on a silicon layer resting on an Insulating Layer of Silicon dioxide (SiO₂). The insulating layer is created by flowing oxygen onto a plain silicon wafer and then heating the wafer to oxidize the silicon, thereby creating a uniform buried layer of silicon dioxide. Transistors are encapsulated in SiO₂ on all sides.

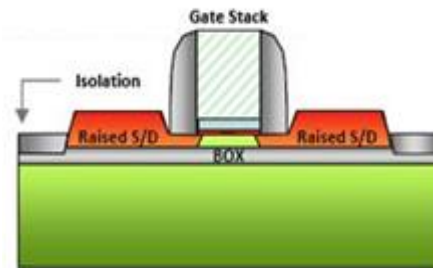


Figure 1 A silicon-on-insulator (SOI) MOSFET

FDSOI

In an NMOS transistor, applying a positive voltage to the gate depletes the body of P-type carriers and induces an N-type inversion channel on the surface of the body. If the insulated layer of silicon is made very thin, the layer fills the full depth of the body. A technology designed to operate this way is called a —fully depleted SOI technology.

PDSOI

On the other hand, if the insulated layer of silicon is made thicker, the inversion region does not extend the full depth of the body. A technology designed to operate this way is called a —partially depleted SOI technology.

Advantages of SOI

- The latch-up effect observed in bulk devices can be completely prevented due to the dielectric isolation. In addition, several processing steps are saved, since the deep wells are not required. As a result of this, the minimum distance between devices is determined only by the technology constraints on the minimum width of the oxide filled trenches, required for the lateral isolation of devices. This and the fact that body contacts are not needed for fully depleted devices, result in a higher device density when using a SOI process compared with a bulk process.
- Further, when scaling down the device dimensions the doping densities must be increased to maintain proper device behavior, which is hard to manage when the device

dimensions reach 50 nm and below. However, for thin film devices, such as fully depleted SOI, the doping densities required are lower [18]. This is one reason for why SOI may be more suitable for the future processes.

Disadvantages of SOI

- The thermal conductivity is about 100 times lower for SOI devices than for bulk devices, due to the buried oxide layer and the thin active silicon layer. Hence, the self-heating effect is an important issue to take into concern when designing in SOI technology. New models and simulators that not only consider the electrical behavior, but also the temperature properties of the circuits, are required [19].

IV. JLDG SON MOSFET

The JL transistor is a resistor with uniform doping. The doping concentration is constant through the source, channel, and drain. The absence of doping concentration gradient eliminates diffusion of impurities and the problem of sharp doping profile formation altogether. Any increase of temperature induces variations of the electrical parameters of MOS devices (e.g., threshold voltage shift, increase of leakage current, and reduction of mobility. Recently, a junction less (JL) double-gate (DG) field effect transistor (DGFET) (JL DGFET) has been reported as a promising candidate for future technology nodes. Technically, all undoped or lightly counter-doped DG MOSFETs are junction less if the doping in the channel is of the same type as the source and the drain. What distinguishes the recently proposed junction less MOSFET is that the channel is heavily doped of the same type and to a similar magnitude of concentration as the source and the drain. The fabricated junction less device with a high content of impurity concentration within the channel and source/drain (S/D) regions requires no junctions and exhibits many advantages such as the **simplified flexible fabrication process, nearly ideal sub threshold slope ($SS \approx 60$ mV/dec), high ON-OFF-current ratio ($I_{ON}/I_{OFF} > 10^7$), low S/D series resistance, and small drain-induced barrier lowering.** Moreover, the JL transistor shows many interesting characteristics, like conductance oscillations at low temperature and high temperature behaviour.

Increased demand for High Performance, Low Power and Low Area among microelectronic devices is continuously pushing the fabrication process to go beyond ultra deep sub-micron (UDSM) technologies such as 45nm, 32nm and so on. Currently, chips are being designed in 55nm, 45nm and 32nm process nodes. The magic term of SOI is attracting a lot of attention in the design of high-performance circuits. SOI offers speed, reliability and hardness beyond traditional technologies. SOI's performance parameters can be attributed largely to overall capacitance reduction as well as lower SOI device leakage. This creates the ideal opportunity for implementing SOI in sophisticated IC designs operating under LP-LV conditions.

The term SOI means Silicon on Insulator structure, which consists of devices on silicon thin film (SOI layers) that exists on insulating film. In the case of bulk CMOS devices, P/Ntype MOS transistors are isolated from the well layer. In contrast, SOI-CMOS devices are separated into Si supporting substrate and buried oxide film (BOX). Also, these devices are structured so each element is completely

isolated by LOCOS (Local Oxidation of Silicon) oxide film and the operating elements area (called the SOI layer) is completely isolated by insulators. Also, elements that have a thin SOI layer (normally <50 nm) and have all body areas under the channel depleted, are called complete depletion type SOI. Conversely, elements that have a thick SOI layer (normally >100 nm) and have some areas at the bottom of the body area that are not depleted, are called partial depletion type SOI.

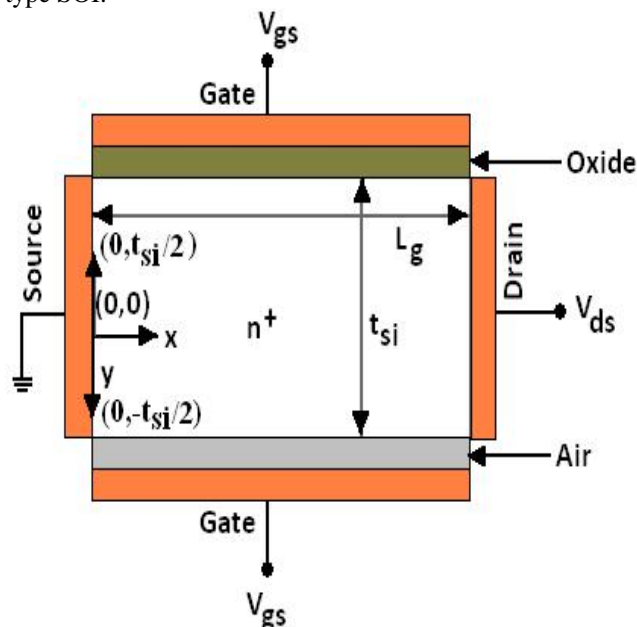


Figure 2 JLDG FD SON MOSFET

V. DOUBLE GATE (JLDG) MOSFET

The downscaling of the channel length in MOSFETs poses increasingly difficult challenges as leakage current and short-channel effects increase due to the decreasing control efficiency of the gate on the channel. In a MuGFET, the gate electrode is wrapped around a silicon nanowire, forming a multigate structure with excellent control of the channel potential, which allows one to fully deplete the channel region. In very-short-channel devices, the formation of ultra sharp source and drain junctions is quite a challenge and imposes drastic conditions on doping techniques and thermal budget. The JL transistor is a resistor with uniform doping. The doping concentration is constant through the source, channel, and drain [20]. The absence of doping concentration gradient eliminates diffusion of impurities and the problem of sharp doping profile formation altogether. Any increase of temperature induces variations of the electrical parameters of MOS devices (e.g., threshold voltage shift, increase of leakage current, and reduction of mobility).

VI. CONCLUSION AND FUTURE SCOPE

In this paper, we have developed an expression for surface Potential of short channel junction-less double gate (JLDG). MOSFET by solving 2-D Poisson's equation. A comparison of analytical solution with numerical solution using ATLAS device simulator provided good approximation of the model. It can be observed through results that the JLDG MOSFET provides higher immunity to SCEs as compared to junction based DG MOSFET.

This present work has various possible extensions that could be aimed as later research work. Some directions based on the present work.

The work can be expanded to incorporate the effects of mobility enhancement by introducing strain in JLDG SON structure. A lot of scope lies in investigating the effect of different materials like SiGe, SiC as the channel material on the characteristic JLDG SON structure. The concept of underlap double gate can be introduced in the JLDG SON concept for superior device performance

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