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Pre-Analyze the Noise Performance of Switched-Capacitor Low-Pass Filter

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***Abstract*—The switched-capacitor low-pass filter (LPF) is a very crucial circuit block in analog to digital conversion systems. In the past decades, many researchers have devoted their efforts in trying to achieve better noise performance and frequency response. Unfortunately, these studies skipped a very important function that the designers needed. The previous works did not implement the output noise numerical calculation during the design stage. Therefore, today's circuit designers have to tune up the circuit parameters manually in order to achieve better noise performance, a very time consuming process. In this paper, we adopted the Marco Amplifier Model as the basis upon which to construct a pre-analyzed noise performance topology for switched-capacitor low-pass filter (SCLPF). From the experimental results, it can been seen that by using this novel topology, the noise performance can be correctly pre-analyzed during the circuit design stage. The analysis procedure for this noise performance topology has been demonstrated by a 4th order SCLPF. The simulation results have been verified by using standard 0.35-µm CMOS process technology.**

***Index Terms*—Switched-capacitor low-pass filter (SCLPF), noise performance, Marco amplifier model, noise model, analysis procedure.**

I. INTRODUCTION

In a conventional analog to digital (A/D) conversion system, the switched-capacitor low-pass filter is a crucial circuit block. In the past decades, this circuit has been well studied and designed to achieve better noise performance and frequency response [1]-[8]. Unfortunately, until now, numerical calculation of output noise during the design stage has been impossible. Thus, most circuit designers still need to tune up the circuit parameters manually to achieve better noise performance, and it is time consuming.

A design-oriented estimation algorithm was proposed by Schreier, Silva, Steensgaard and Temes (2005) to estimate the thermal noise of a switched-capacitor filter [9]. They proposed a mathematical model to mimic the effect caused by thermal noise of a switched-capacitor circuit and operational amplifier (op-amp). Although the mentioned approach can efficiently estimate the total thermal noise of the switched-capacitor filter, it still needs a huge amount of calculations to build an accurate noise model. Moreover, the effectiveness of this approach did not verify the operation of real CMOS circuits.

In this paper, we adopted a Marco Amplifier Model as the basis upon which to construct a pre-analyzed noise performance topology for a switched-capacitor low-pass filter (SCLPF). Based upon this novel topology, a switched-capacitor equivalent circuit was examined and the Marco Amplifier Model adopted to construct this switched-capacitor low-pass filter (SCLPF). This proposed topology can be used to efficiently estimate the noise performance of the switched-capacitor filter. The Marco Amplifier Model features several op-amp characteristics: flicker noise, thermal noise, dc gain and noise bandwidth (NBW). By offering the desired specifications of CMOS op-amp, the Marco Amplifier Model can accurately estimate the noise. In this study, the analysis procedure for this noise performance topology is demonstrated by a 4th order switch-capacitor low-pass filter. The simulation results have been verified by using standard 0.35-µm CMOS process technology.

The rest of this paper is organized as follows. Section 1 presents the introduction. Section 2 discusses the rationale of the noise model of the switched-capacitor low-pass filter. Section 3 shows the experimental results of the proposed topology. Finally, Section 4 concludes this paper.

II. NOISE MODEL OF A SWITCHED-CAPACITOR LOW-PASS FILTER

To construct the noise model of a switched-capacitor filter, a 4th order switched-capacitor low-pass filter shown in Fig.1 has been selected to demonstrate the analysis procedure.

A. Equivalent Circuit of a Switched-Capacitor Circuit

As shown in Fig. 1, the filter can be separated into two parts: the switched-capacitor circuit and amplifier. The switched-capacitor circuit contains four switches and one capacitor. The capacitor ratio is labeled in Fig. 1. The

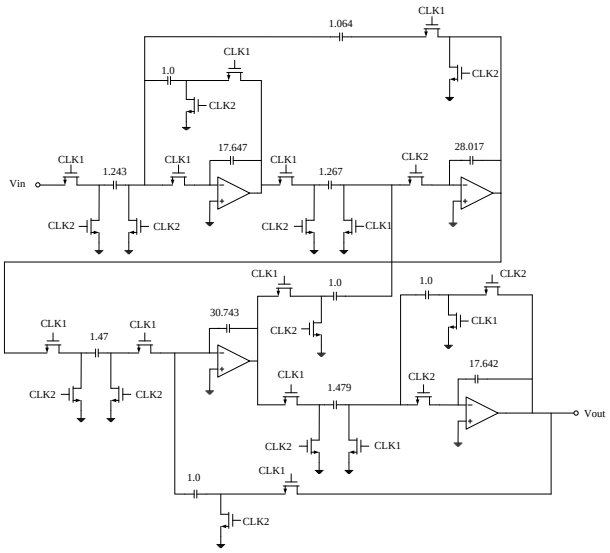

Fig. 1. Schematic of a 4th order switched-capacitor low-pass filter.

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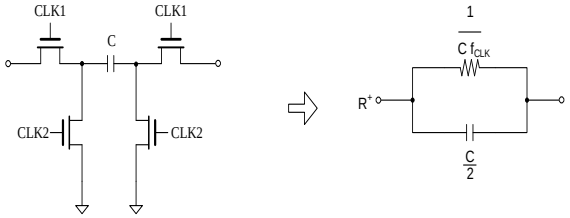

Fig. 2. Equivalent RC circuit of inverting switched-capacitor circuit.

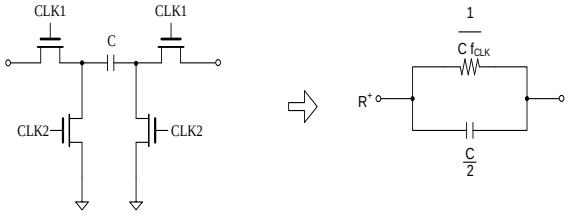

Fig. 3. Equivalent RC circuit of non-inverting switched-capacitor circuit.

designers can change the capacitor value by changing the unit capacitor, which has a ratio of 1.0.

From the schematic of the switched-capacitor filter circuit, it can be observed that the noise of the filter is mainly generated by two main circuit blocks: switched-capacitor circuit and amplifier. Therefore, if the noise of these two circuit blocks is estimated, the noise of the switched-capacitor filter can be accurately identified. In the switched-capacitor circuit, it is difficult to analyze the noise of the switch parts. However, the switched-capacitor circuit can be represented by the RC equivalent circuit [10]. The RC equivalent circuit of inverting and the non-inverting switched-capacitor circuit are shown in Figs. 2 and 3, respectively. The equivalent resistor and capacitor in the circuit can be obtained as follows:

$$R_{EQ} = \frac{1}{C\ f_{CLK}};\ \ C_{EQ} = \frac{C}{2} \tag{1}$$

where C is the capacitor and f_{clk} is the clock frequency. By replacing the switched-capacitor with the equivalent resistance, the switch resistance thermal noise then can be estimated.

B. Macro Amplifier Model

In the switched-capacitor filter, the noises are generated mainly by the op-amp. The noises of op-amp comprise two different kinds: (1) flicker (*1/f*) noise and thermal noise; (2) aliased op-amp wideband noise [10]. To analyze the *1/f* noise and thermal noise, we adopted a conventional diode to simulate the noise characteristics. The noise of the diode is given by:

$$\overline{i_{Diode}^2} = 2qI_D + \frac{KFI_D}{f};\ \ g_D = \frac{\partial I_D}{\partial V_D} = \frac{I_s}{V_T}e^{\frac{V_D}{V_T}} \approx \frac{I_D}{V_T} \tag{2}$$

where

$$I_D = I_s(e^{\frac{V_D}{V_T}} - 1); V_T = \frac{kT}{q}$$

where I_D is the current flowing through diode; I_s is the reversed-biased saturation current; V_D is the voltage across the diode; V_T is the thermal voltage; g_D is the small signal conductance of voltage fluctuation; k is the Boltzmann constant; KF is the flicker noise coefficient and T is the absolute temperature of the device in degrees Kelvin. In Eq. (2), the white noise part $\overline{i_{Ds}^2} = 2qI_D$ is shot noise and it will be used to simulate thermal noise. The thermal noise can be calculated as follows:

$$\overline{V_{Th}^2} = \frac{\overline{i_D^2}}{g_D^2} = \frac{2qI_D}{\left(\frac{I_D}{V_T}\right)^2} = \frac{2(kT)^2}{qI_D} \tag{3}$$

In practical application, $\overline{V_{Th}^2}$ is the value of desired thermal noise power density. I_D is the current that flows through the diode. By re-arranging the terms, the I_D value can be obtained as follows:

$$I_D = 2q\frac{V_T^2}{V_{Th}^2} \tag{4}$$

The *1/f* noise part in Eq. (2) is $\overline{i_{Df}^2} = KFI_D/f$ and the total noise can be calculated as follows:

$$\overline{V_{TOT}^2} = \frac{\overline{i_{D_{TOT}}^2}}{g_D^2} = \frac{2qI_D}{g_D^2} + \frac{KFI_D}{g_D^2 f} = \frac{2qI_D}{\left(\frac{I_D}{V_T}\right)^2} + \frac{KFI_D}{f\left(\frac{I_D}{V_T}\right)^2} \tag{5}$$

The equation of the total noise can then be rewritten as follows:

$$\overline{V_{TOT}^2} = \overline{V_{Th}^2} + \overline{V_f^2} = \frac{2qV_T^2}{I_D} + \frac{KFV_T^2}{fI_D} \tag{6}$$

In Eq. (6), the total noise contains thermal noise ($\overline{V_{th}^2}$) and flicker noise ($\overline{V_f^2}$). By rearranging the terms in Eq. (6), *KF* is obtained as follows:

$$KF = \left(\overline{V_{TOT}^2} - \overline{V_{Th}^2}\right)\frac{I_D f}{V_T^2} \tag{7}$$

where I_D is the forced current and $\overline{V_{TOT}^2}$ is the total noise power density at frequency *f*. From the discussions on *1/f* noise and thermal noise for op-amp, the noise model to set *1/f* and thermal noise can be obtained as shown in Fig. 4. The forced current I_{FORCE} can be derived in Eq. (3) as follows:

$$I_{FORCE} = \frac{2q}{\overline{V_{Th}^2}}V_T^2 = \frac{2q}{\overline{V_{Th}^2}}\left(\frac{kT}{q}\right)^2 \tag{8}$$

where $\overline{V_{Th}^2}$ is the thermal noise power. In Eq. (7), the *KF* can be written as follows:

$$KF_D = \frac{I_D f}{V_T^2}\left(\overline{V_{TOT}^2} - \overline{V_{Th}^2}\right) = \frac{2q\frac{V_T^2}{\overline{V_{Th}^2}}f}{V_T^2}\left(\overline{V_{TOT}^2} - \overline{V_{Th}^2}\right) = 2qf\frac{\left(\overline{V_{TOT}^2} - \overline{V_{Th}^2}\right)}{\overline{V_{Th}^2}} \tag{9}$$

where $\overline{V_{TOT}^2}$ is the noise power of op-amp at frequency *f*.

The other noise that must be considered in op-amp is aliased op-amp wideband noise. In the frequency domain, the filter will sample the desired signal at the sample frequency and fold back the signal into the interest frequency as shown in Fig. 5. However, it also folds back the noise around the

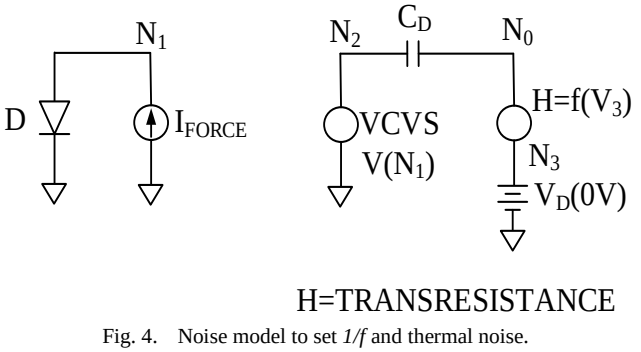

Fig. 4. Noise model to set *1/f* and thermal noise.

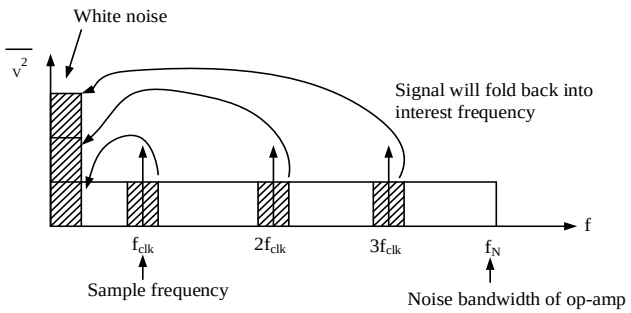

Fig. 5. Alias noise in frequency domain.

sampling frequency into the interest frequency. This alias noise can be approximated as:

$$\eta_T = V_{Th}^2\left[2\left(\frac{f_N}{f_{CLK}}\right)-1\right] = V_{Th}^2[NBW-1] \tag{10}$$

where

$$NBW = 2\left(\frac{f_N}{f_{CLK}}\right);\ f_N = \frac{\pi}{2} f_u$$

NBW is the noise bandwidth of the op-amp and f_u is the unity-gain frequency of the op-amp. Since this noise is white, it can be modeled by the thermal noise of a resistor, the value of which can be calculated by:

$$R_N = \frac{\eta_T}{4kT} \tag{11}$$

In SPICE, two resistors in parallel are required so $R_{NSPICE}=2R_N$, as shown in Fig. 6. After considering all the effects caused by the 1/f noise, thermal noise and aliased op-amp wideband noise, the complete Marco Amplifier Model of an op-amp can be constructed, as shown in Fig. 7.

The Amplifier's magnification coefficient is set to 10^4 and uses a voltage-controlled voltage source (VCVS) to simulate the op-amp. The value of DC gain can be changed according to the real amplifier performance.

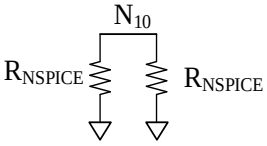

Fig. 6. Two resistors in parallel in SPICE.

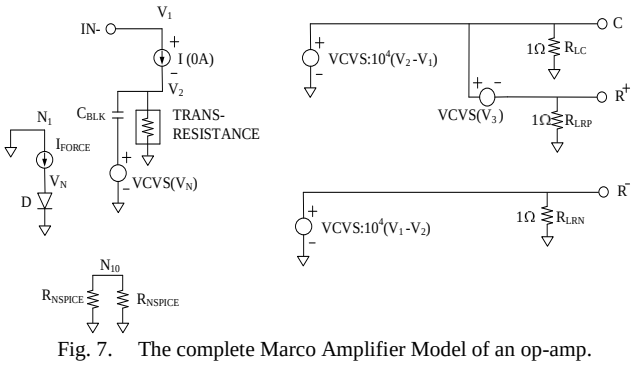

Fig. 7. The complete Marco Amplifier Model of an op-amp.

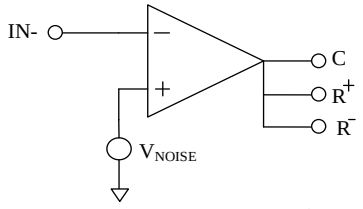

Fig. 8. The symbol of a Marco Amplifier Model.

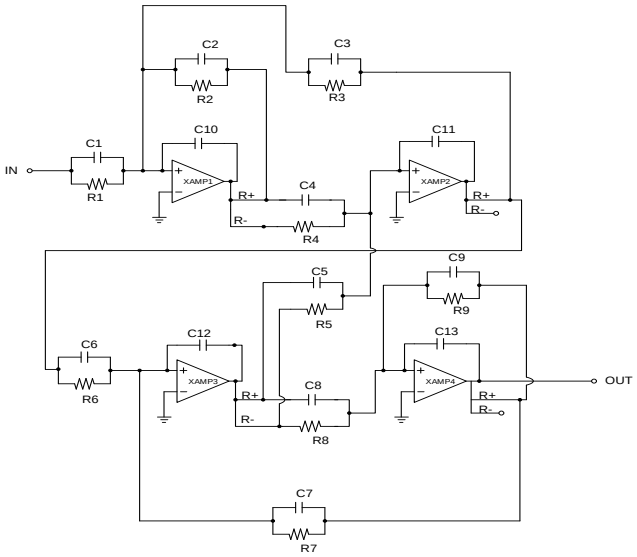

Fig. 9. The complete noise schematic of the 4th order switched-capacitor low-pass filter.

Table 1. Assumption values of circuit parameters in the Marco Amplifier Model.

Thermal noise ($n V/\sqrt{Hz}$)	1500
1/f noise ($n V/\sqrt{Hz}$)	15
DC gain of op-amp(dB)	80
NBW	20

To simplify the noise model of the switched-capacitor filter, the symbol of the Marco Amplifier Model has been applied to construct the complete noise model of the filter, as shown in Fig. 8. In the following sections, the symbol of Marco Amplifier Model is then being adopted for the construction of the proposed topology: "a pre-analyzed noise performance topology for SCLPF". By using this topology, the noise performance can be pre-analyzed during the circuit designing stage.

III. Experimental Results of Noise Model

The complete noise model of a 4th order switched-capacitor low-pass filter, as shown in Fig. 1, can be obtained based on the equivalent circuit of a switched-capacitor circuit and the Marco Amplifier Model of op-amp. Fig. 9 shows the complete noise schematic of the switched-capacitor low-pass filter (SCLPF).

The circuit parameters of the Marco Amplifier Model in Fig. 9 have been assumed to specific value as shown in Table 1.

It is noted that after pre-analyzing the noise performance of the switched-capacitor filter, the designers have to design the amplifier according to these specifications. From Table 1, the NBW is assumed to be 20. We assume the clock frequency to be 500kHz, and based on Eq. (10), the unity-gain frequency (UGF) can be calculated as follows:

$$UGF = \frac{f_{clk}\times NBW}{\pi} = \frac{500k\times 20}{\pi} \approx 3.18MHz \tag{12}$$

From the previous discussions, the designers must design the amplifier with thermal noise 1500n $V/\sqrt{Hz}$, 1/f noise 15n $V/\sqrt{Hz}$, DC gain 80dB and UGF 3.18MHz. Hence, after pre-analyzing the noise of switched-capacitor, the designers will have some clues for designing the corresponding

Table 2. Size of equivalent resistors and capacitors in a complete noise schematic.

Capacitor	Value(pF)	Resistor	Value(MΩ)
C1	0.32	R1	3.22
C2	0.25	R2	4
C3	0.27	R3	3.76
C4	0.32	R4	3.16
C5	0.25	R5	4
C6	0.37	R6	2.72
C7	0.25	R7	4
C8	0.38	R8	2.70
C9	0.25	R9	4
C11	14.01		

amplifier. To analyze the noise performance of the switched-capacitor filter in Fig. 1, the unit capacitor must be assigned a specific value.

If the capacitor size increases, the total noise of the filter will decrease. However, a large capacitor size means a large chip area. Hence, we will try to minimize the capacitor size to maintain the lowest chip area and to achieve the desired minimum output noise. In this paper, the goal is to design the performance of total output noise to meet $70\,\mu V_{rms}$ integrated from 10Hz to 10kHz.

To achieve the required specifications of noise, we first choose the value of each unit capacitor as 0.5pF. Secondly, we calculate all the equivalent resistor and capacitor values of the switched-capacitor circuit in Fig. 9, as shown in Table 2. With these circuit parameter values, the noise performance can be analyzed effectively.

From the simulation results, the total output noise is $69.26\mu V_{rms}$. According to the required noise performance discussed above, the total output noise can achieve the desired specifications during the pre-analysis stage. Therefore, the designers can start designing the amplifier based on the corresponding specifications without spending too much effort on analyzing the noise characteristics.

IV. Conclusion

In this paper, a switched-capacitor equivalent circuit is examined and the Marco Amplifier Model has been adopted to construct "a pre-analyzed noise performance topology for a switched-capacitor low-pass filter (SCLPF)". By giving the desired specifications of CMOS op-amp, this topology can estimate the noise performance of an SCLPF with high accuracy and efficiency.

The analysis procedure for the proposed topology has been demonstrated by a 4th order switch-capacitor low-pass filter. With the proposed SCLPF, the designers can pre-analyze the noise performance in an effective way, and speed up the whole design procedure.

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