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Implementation of High Speed, Low Power NAND Gate-based JK Flip-Flop using Modified GDI Technique in 130 nm Technology

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Abstract— **- This paper is introduce a high speed, low power synchronously clocked NOR / NAND gate based JK flip-flop by modified Gate Diffusion Input (GDI) procedure in 130 nm technology. We present two type of JK Flip Flop, NAND Gate based and NOR Gate based. We find the two types of issue, first is High power consumption and second is high number of transistor. In this paper, we are reducing the number of transistor with power consumption. For further enhance the performance of the JK Flip Flop, we use M-GDI technique. In which low number of transistors will use and power consumption will be also low. Modified GDI (gate Diffusion Input) is a technique for low power combinational digital circuit in which logic gates are design by use low number of transistor .This technique is able to reduce the power consumption, Propagation delay and area of the circuits with low complexity of logic design .**

***Index Terms*— Modified Gate Diffusion Input (MGDI) procedure, low power, high speed, power delay product (PDP), transistor count, area.**

I. INTRODUCTION

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bi stable multi vibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems [1].

Flip-flops and latches are used as data storage elements. A flip-flop stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal [1]-[2].

Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered). Although the term flip-flop has historically referred generically to both simple and clocked circuits, in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits; the simple ones are commonly called latches.

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The flip-flop is constructed in such a way that the output Q is AND with K and CP. This arrangement is made so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Similarly Q' is ANDed with J and CP, so that the flip-flop is cleared during a clock pulse only if Q' was previously 1 [3].

Using this terminology, a latch is level-sensitive, whereas a flip-flop is edge-sensitive. That is, when a latch is enabled it becomes transparent, while a flip flop's output only changes on a single type (positive going or negative going) of clock edge [4].

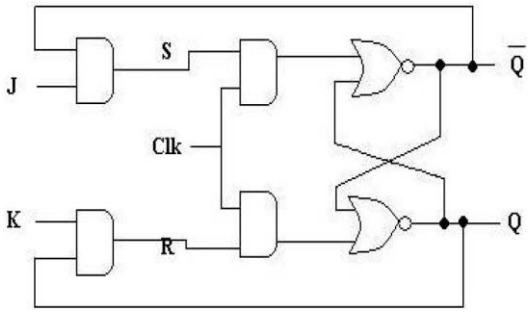

Fig 1 JK flip flop by AND, NOR gate

Table 1: Truth tables of JK flip flop

J	K	Function
0	0	Hold
0	1	0
1	0	1
1	1	Toggle

A. JK Flip Flop By AND, NOR Gate in Tanner Tool

As we can see in fig 2, we design the JK flip flop with the help of AND, NOR gate. We give the three inputs clk, J, K and Q , Q_bar as a output . In this we use four AND gate and two NOR gate for design the JK flip flop.

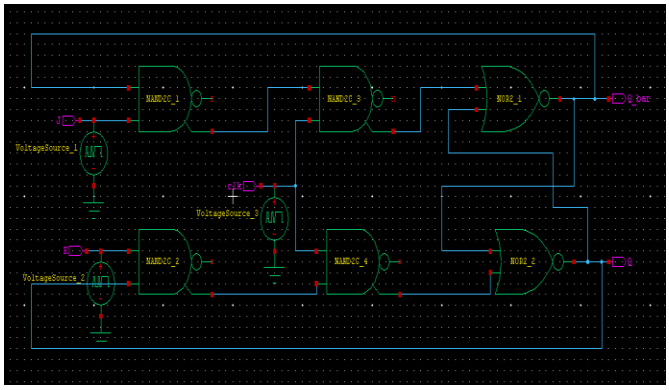

Fig 2 JK flip flop by AND, NOR gate design by Tanner Tool

B. JK Flip Flop By NAND Gate

As we can see from Fig 3, JK flip flop is design by use NAND gate. We are taking three inputs J,K and Clk as an input . Eight NAND gate is using for design the JK flip flop. In the given design two stages are showing for the final output that is Master Latch and Slave Latch. Fig 4 is showing the design of Tanner tool for JK flip flop with NAND gate. [6]

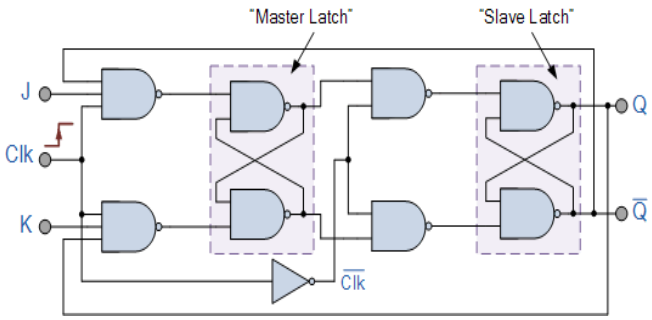

Fig 3 JK Flip Flop by NAND Gate

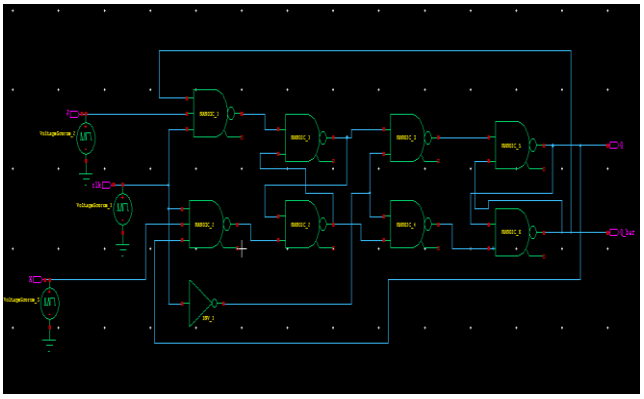

Fig 4 JK flip flop design by TANNER tool.

In the Fig 4 for give the inputs of the JK and clk we use voltage source of bits. In which we can give 10 bits at a single time.

II. Problem Statement

In the VLSI, main issue is power consumption and Area. In this paper , we are working for the two major problems , that's are

A . Power Consumption

In VLSI, Power consumption is the main issue which occurs in the CMOS design. As we can see Fig 2 and Fig 4 are using lots of Logic gates by which the power consumption is getting increase. We have to reduce the power consumption of the JK flip flop by apply proposed methodology. In the Fig 2 power consumption is 8.680838e-003 watts and in the Fig 4 power consumption are 5.736606e-003 watts. We have to reduce the power consumption from the existing power consumption results.[6,7]

B. Number of Transistor

As we can see from Fig 2 and Fig 4, lots of transistor and gates are using. As the number of transistor get increase the area get increase and due to this Power consumption also get increase. In our Paper, we are working for the number of transistor problem. In the Fig 2 Total number of transistors are using 32 for the JK flip flop design which we design by AND , NOR gate . In the second design total number of transistor are using 54 for the JK flip flop design in which NAND gate are using. So in this paper our first problem is reducing the number of transistor for both designs.

III. Proposed Methodology

For reduce the power consumption and number of transistor we are applying Modified GDI methodology. Morgenstern et al. investigated a high-speed and multipurpose logic style for low power electronics design, known as Gate Diffusion Input (GDI), [7] with reduced area and power necessities, and proficient of implementing a broad variety of logic functions. Fig 5 shows basic M-GDI logic cell, which is used for implementing verity of logic functions and circuits at low power and high speed design where G, P and N are three inputs and output is taken from D terminal. Table 1 represents the logic functions which can be implemented with the help of this basic M-GDI cell [1,2]. But this basic Gate Diffusion Input (M-GDI) logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic style [4, 5].

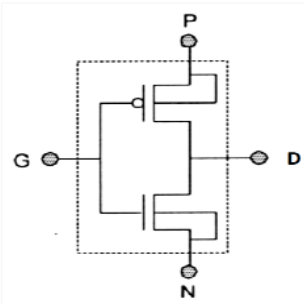

Fig 5 Basic M-GDI Cell

In addition to this physical implementation of basic M-GDI cell is not possible in traditional p-well progression. Furthermore, realizing via twin well/ triple-well mechanism would necessitate the fundamental M-GDI cell to possess an enhanced area owing to discrete wells per transistor. This fundamental conjecture is imprecise as the source along with drain nodule relies on the logic values provided at the input. Therefore, in the primary M-GDI cell, the substrate effect was eradicated in circumstances where the body was attached to the source, but an enhancement in threshold voltage transpired on attachment of the bulk to the drain. Moreover since the basic M-GDI cell obliges twin-well CMOS or SOl procedure to comprehend, accomplishment of a rudimentary M-GDI chip will be a dear one. The modified M-GDI cell as given away to overcomes the drawbacks suffered by primordial M-GDI cell and is extremely akin to the basic M-GDI cell except for the fact that the bulks of PMOS as well as NMOS transistors in a modified GDI cell are persistently fixed to V DD and GND, respectively. This facilitates effortless realization of the M-GDI gates in typical CMOS procedures. The consequence of the body effect on circuit functioning is enormously alike to that of crude M-GDI cell.

A. NOT gate using Modified GDI technique

Fig 6 displays the NOT gate created using modified GDI technique and is almost similar to that of a standard CMOS inverter.

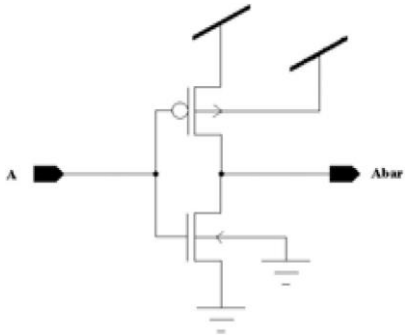

Fig 6 NOT gate using modified GDI technique

Fig 7 shows that the exudes the input as well as output waveform of a NOT gate utilizing modified GDI process in 130nm technology.[8]

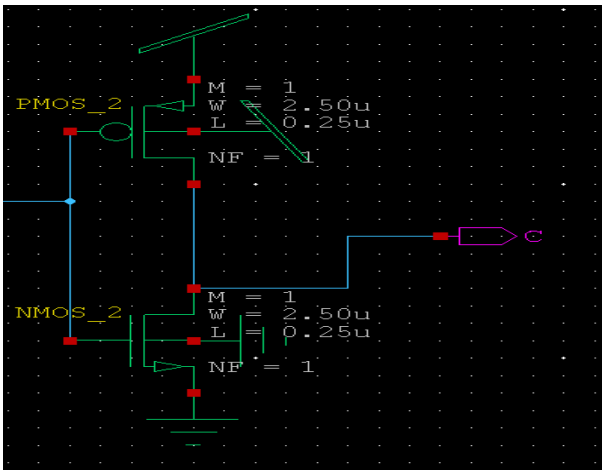

Fig 7 NOT gate design in Tanner by M-GDI Technique

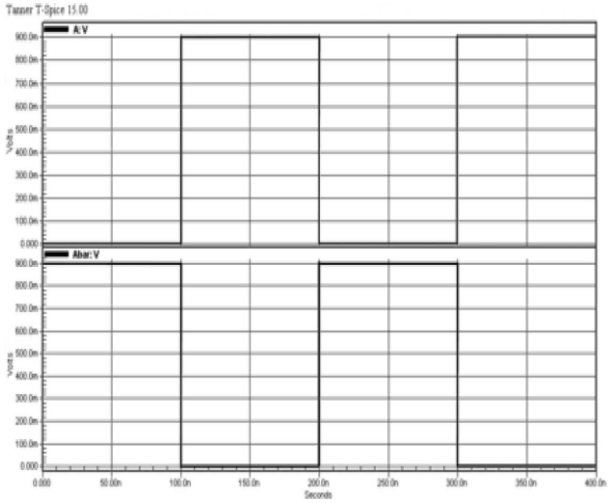

Fig 8 Input and output waveform of a NOT gate using modified GDI

B. *NOR gate using Modified GDI technique*

Fig. 9 depicts the NOR gate generated using modified GDI technique. It comprises of two modified GDI cells where the port 'P' of the first cell is given an input 'B' while port 'G' of the first cell is given an input' A'. Port 'N' of the first cell is supplied with Vdd and the output 'nl' is connected to port 'G' of the second cell which acts as a basic inverter complementing the output obtained from the first cell.

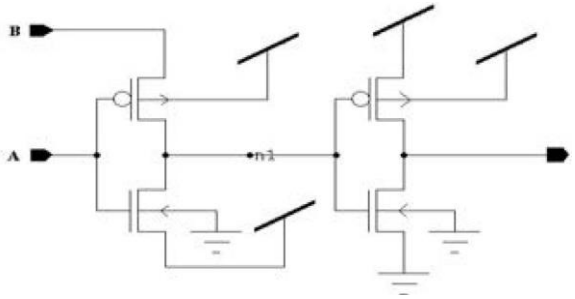

Fig 9 NOR gate using modified GDI technique

Fig. 10 portrays the input as well as output waveforms of the NOR gate designed using modified GDI technique in 130nm technology.

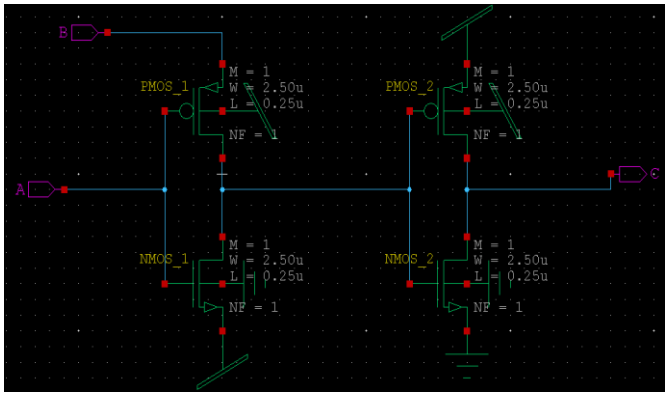

Fig 10 NOR gate Design by Tanner M-GDI Technique

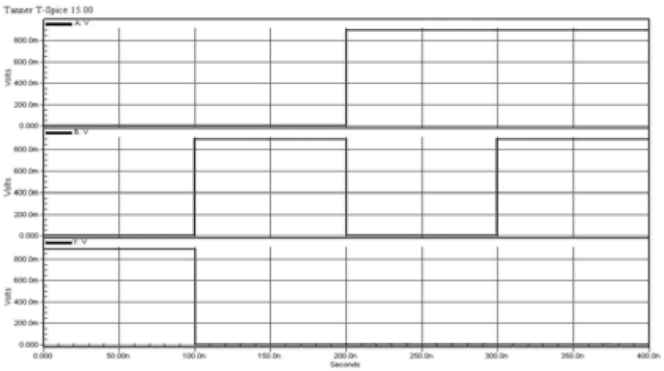

Fig 11 Input and output waveform of a NOR gate using modified GDI technique

C. *AND gate using Modified GDI technique*

Fig.12 shows an AND gate devised using modified GDI technique where port 'P' is connected to GND and port 'N' is supplied an input 'B'. Port '0' is given an input' A'.

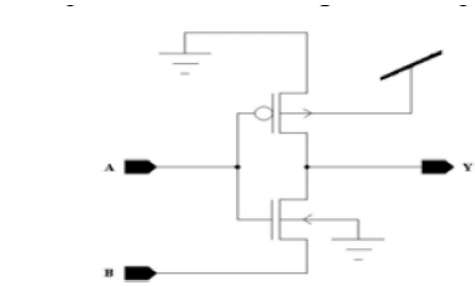

Fig 12 AND gate using Modified GDI technique

Fig. 13 shows the input and output waveforms of an AND gate conceived using modified GDI technique in 130 nm technology.

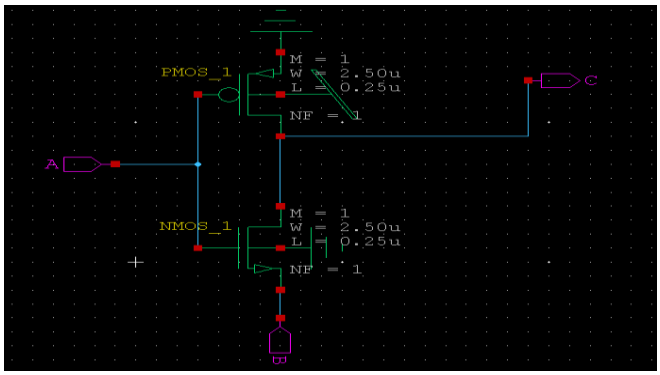

Fig 13 AND gate using Modified GDI technique by Tanner

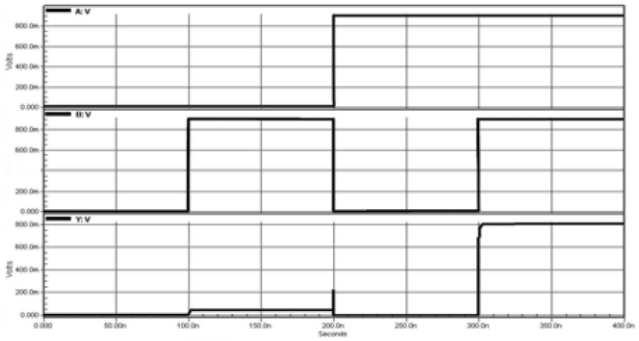

Fig 14 Input and output waveform of an AND gate using modified GDI

In the fig 15, we show the JK flip flop by use AND , NOR gate . As we can see in the fig 16 four AND gate , two NOR gate are using for design JK flip flop . For give the input to the J ,K and CLK we use voltage source .

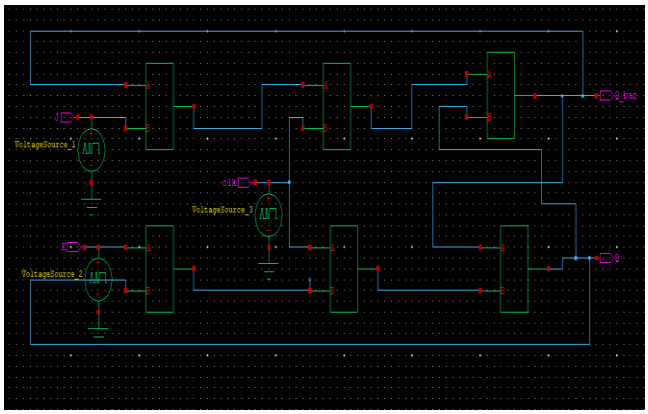

Fig 15 JK flip flop by use AND, NOR Gate

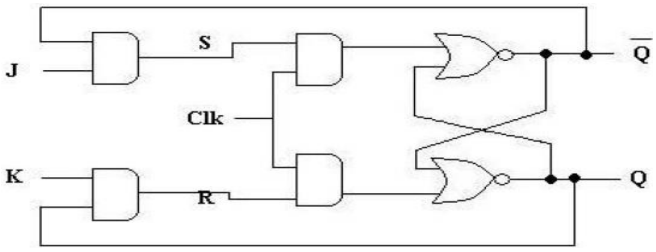

Fig 16 JK flip flop by AND, NOR gate

Fig 16 is showing the JK flip flop by using NAND gate. In this module NAN D gate is design by Modified GDI technique.

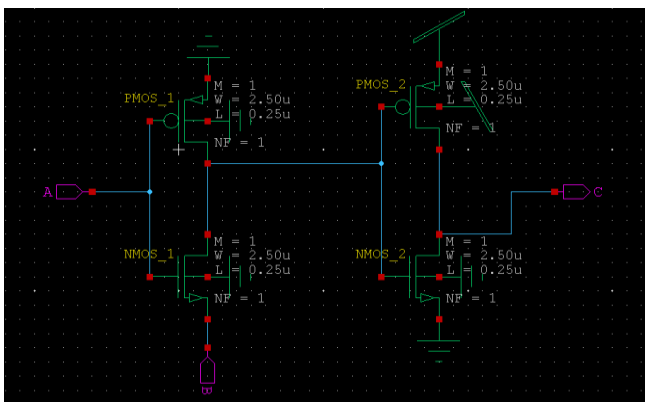

Fig 17 NAND gate design by M-GDI Technique

In figure 17 we design the NAND gate by use M-GDI technique. By the help NAND gate with M-GDI technique we design the JK flip flop as shown in fig 18.

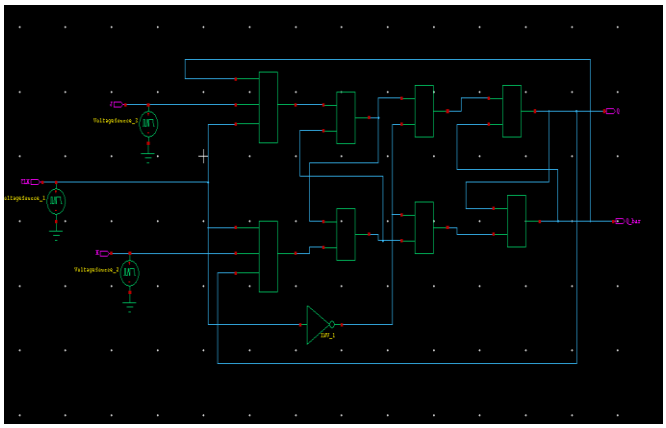

Fig 18 JK flip flop

IV. RESULTS

A. JK Flip Flop By AND, NOR Gate

As we can see from the fig 19, JK flip flop is design by use AND, NOR gate . To give the inputs voltage sources are connected to the J,K and clk input . Q and Q_bar is the output of the JK flip flop .

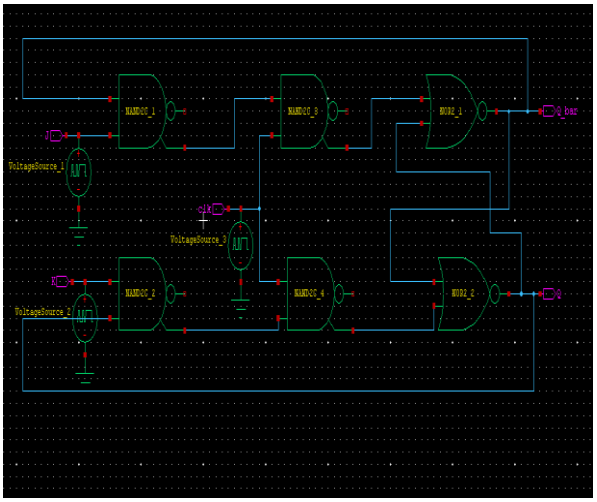

Fig 19 JK flip flop by use AND, NOR gate

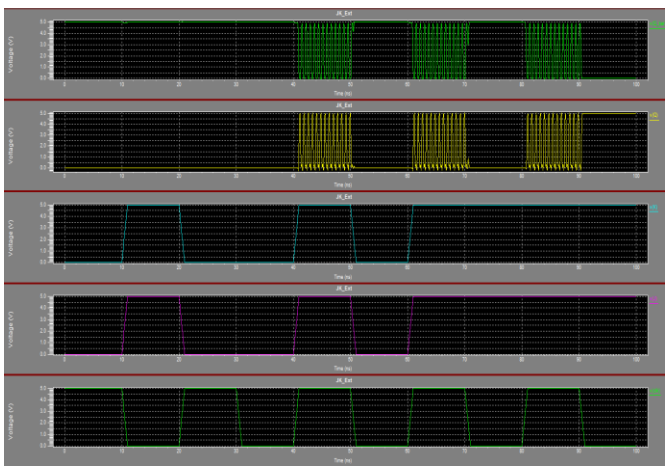

Fig 20 Output Waveform of JK flip flop by AND, NOR gate

In fig 19, CLK, J, K are the inputs and Q , Q_bar is output of JK flip flop . The power consumption for the JK flip flop with AND, NOR gate is 8.680838e-003 watts and number of transistors are 32.

B. JK Flip Flop By NAND Gate

As we can see from the fig 21, JK flip flop is design by use NAND gate . To give the inputs voltage sources are connected to the J,K and clk input . Q and Q_bar is the output of the JK flip flop.

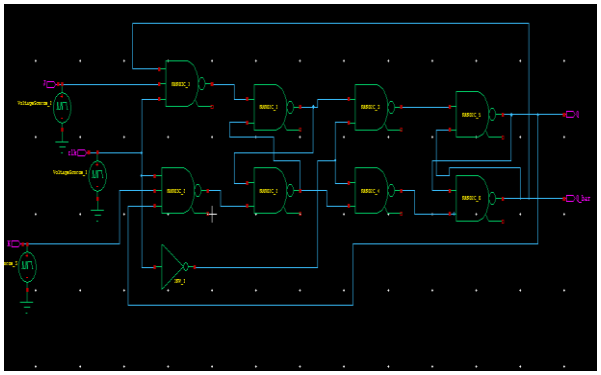

Fig 21 JK flip flop by use NAND gate

As we can see in the fig 21, CLK, J,K are the inputs and Q , Q_bar is the output of the JK flip flop . The power consumption for the JK flip flop with AND, NOR gate is 5.736606e-003 watts and number of transistors are 54.

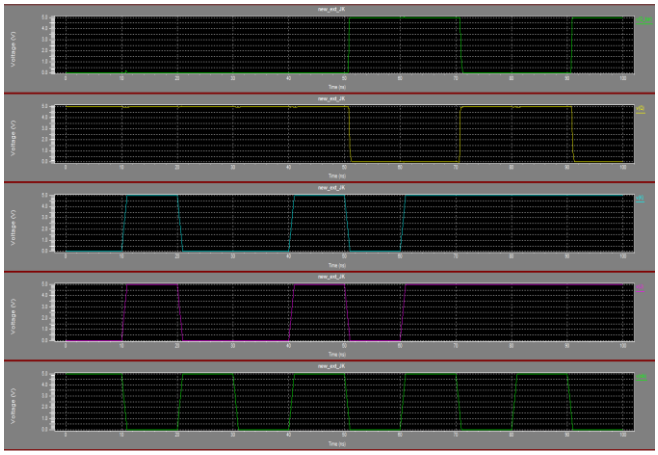

Fig 22 Output Waveform of JK flip flop by NAND gate

C. Proposed JK Flip Flop By AND , NOR Gate With M-GDI Technique

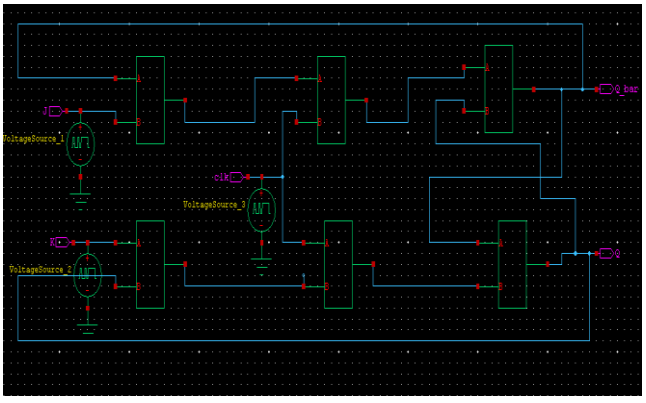

Fig 23 JK flip flop by use AND, NOR gate with M-GDI technique

As we can see from the fig 23, JK flip flop is design by use AND, NOR gate . To give the inputs voltage sources are connected to the J,K and clk input . Q and Q_bar is the output of the JK flip flop . For design the AND , NOR gate use M-GDI technique. As we can see in the fig 23, CLK, J,K are the inputs and Q , Q_bar is the output of the JK flip flop . The power consumption for the JK flip flop with AND, NOR gate by M-GDI Technique is 7.416163e-003 watts and number of transistors are16.

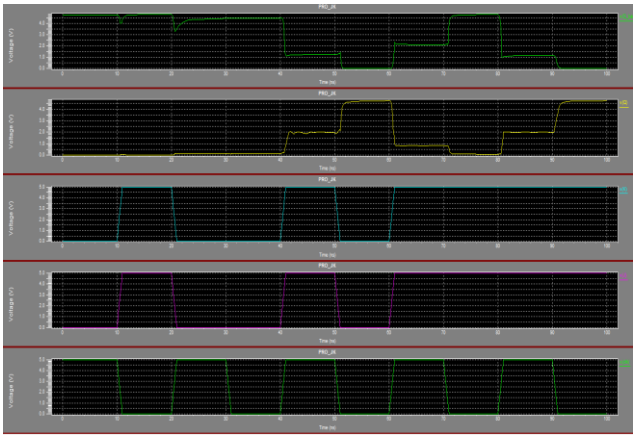

Fig 24 Output Waveform of JK flip flop by AND , NOR gate with M-GDI technique

D. Proposed JK Flip Flop By NAND Gate With M-GDI Technique

As we can see from the fig 24, JK flip flop is design by use NAND gate . To give the inputs voltage sources are connected to the J,K and clk input . Q and Q_bar is the output of the JK flip flop . For design the NAND gate use M-GDI technique.

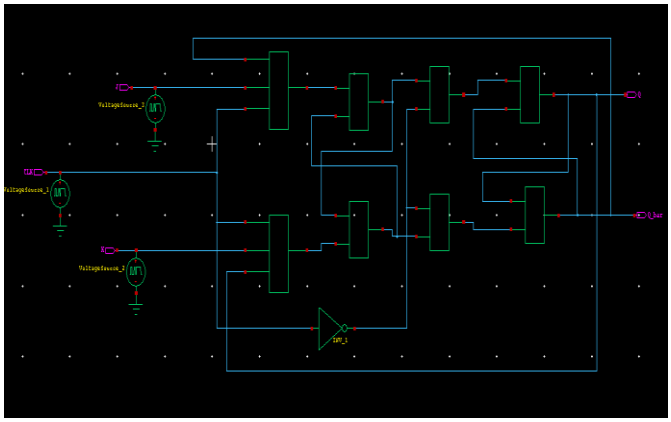

Fig 25 JK flip flop by use NAND gate with M-GDI technique

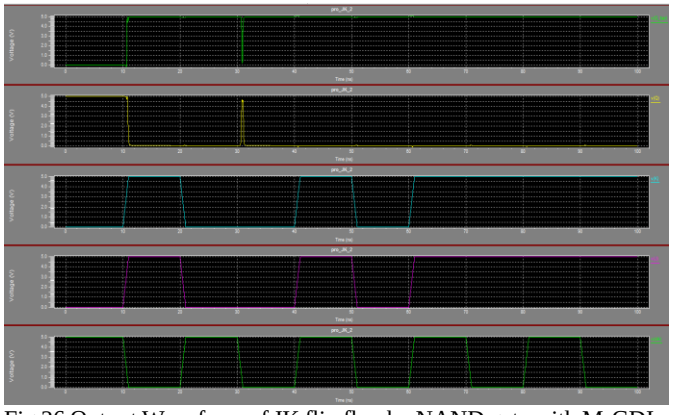

Fig 26 Output Waveform of JK flip flop by NAND gate with M-GDI technique

Table 2 Comparison Table

	Power consumption	Number of transistor
JK Flip Flop By AND , NOR Gate	8.680838e-003 watts	32
JK Flip Flop By AND , NOR Gate with M-GDI	7.416163e-003 watts	16
JK Flip Flop By NAND Gate	5.736606e-003 watts	54
JK Flip Flop By NAND Gate with M-GDI	2.603563e-003 watts	42

As per Table no. 2 in this paper reducing the power as per existing J-K flip flop. Using MGDI less no. transistors are required and low power consumption occurs.

V. CONCLUSION AND FUTURE SCOPE

In this paper, we design the JK flip flop by use two types of design. In the first design, we use AND , NOR gate and in the second design we use NAND gate based design . In the VLSI, main issue is high power consumption and Area. So In this paper we reduce the power consumption and number of transistor for the JK flip flop for both design . We proposed M-GDI technique by which the number of transistor and area get reduce. Without M-GDI technique the power consumption is 8.680838e-003 watts and 32 number of transistor for AND, NOR gate based design and 5.736606e-003 watts for NAND gate based JK flip flop design.

After apply M-GDI the power consumption for the AND, NOR gate based JK flip flop is 7.416163e-003 watts and 2.603563e-003 watts for NAND gate based JK flip flop.

In the future, we can apply proposed modified JK flip flop in Johnson counter. Power consumption and number of transistor can get reduce by apply modified JK flip flop in Johnson counter.

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