

Implementation of BER of 2X2 MIMO System Based On FPGA

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Abstract— MIMO systems are popularly used in the digital baseband communication system and also play a crucial role in the mobile technology such as 4G and LTE system. Thus MIMO can be implemented by using FPGA. The proposed FPGA with MIMO system develop a transmitter and receiver system which consist of the following units such as convolution encoder, maximum likelihood, and deinterleaver and AWGN noisy channel. This model is developed by using Xilinx simulated and integrated into FPGA kit. As a future scope FPGA based MIMO system can be modified and further extended to calculate bit error rate and SNR. The entire system is implemented as an IP core and suitable for a single FPGA device. The proposed system on FPGA shortens the time of design, limits complexity of software simulation and increases productivity.

Index Terms—MIMO, ML (Maximum Likelihood), Convolution Encoder, Viterbi Decoder

I. INTRODUCTION

BER is one of the important parameter used to measure the performance of the overall system where the data rates are calculated. BER is technique which depends on the modulation technique, Signal-to-Noise Ratio (SNR) and type of fading source used at the transmitted signal. BER is usually calculated by using the formula

$$\text{BER} = \frac{\text{number of errors}}{\text{Total number of Bits Sent}}$$

The concept of BER is to analyze a known sequence, the known sequence is send through the channel the channel may be AWGN the known sequence is compared at the received side, and this type of execution suffers a setback. A mixture of methods are used in order to find BER, one of the popular method is pseudorandom method where random sequence is transmitted. The information BER is affected by the signal strength of the forward error correction code. With increasing demand from the customer, technology is growing very fast so all the service provider want to provide better services, one such most popular metric used for the reliability of a wireless digital system is BER. The 2X2 MIMO system make use of Hardware simulation tool like FPGA which is efficient and Faster method compare to software simulation language such as C or FORTRAN.

II. LITERATURE SURVEY

To solve detection and decoding issues a well-organized Maximum likelihood approach is used and designs of best possible detectors and to mingle in channel decoder. The new propose system for channel modeling and STC

communication receivers is used and integrated behavior of detection and decoding for STC under unknown MIMO channel circumstances. The system or technology [1] used is Interference suppression the main purpose is to suppress a signal at interleaver level, maximum-likelihood estimation is used to provide optimal estimation of path to calculate a hamming distance, maximum-likelihood sequence detection, MIMO systems which consist of real and imaginary sequence, space-time coding is jointly organized with an error channel which is corrected at receiver side, soft information is a set of sequence given to the channel encoder. To calculate BER of communication channel different communication scheme are used and early simulation process of communication channel is carried out by programming language such as C or FORTRAN. The main purpose is to reduce the simulation time [2]. To reduce simulation time and other parameters it uses FPGA (Field Programmable Gate Array) technology. The operation in FPGA is carried out in parallel way, so that entire process execution will be faster. FPGA also provide suitable interfaces to the real environment. Comparison can also provide with the entire total simulated counterpart. It makes use of convolution encoder process at transmitter side and Viterbi decoder at receiver side in order to get original signal recover. The set of information which is transmitted is simulated with concept known as pseudo random noise generator. Different type of noise is also added and finally decoded and output which will be getting is compared with original input set of sequence. To obtained probability density function (PDF) the average of four parallel Box muller is taken average [3]. The main purpose is used to generate PDF to scaled SNR which is defined by E_b/N_0 . The decoder used is Viterbi decoder which is used to get back original set of sequence. The extensive hardware is removed by using system level design and Bit error rate is also calculated. The signal transmission parameters to the present circumstances of the wireless channels. Propose a new scheme. Suggest an adaptive radio interface systems for multiple antennas. Suggest a set of transmitter variables called Modulation, Coding and Antenna Schemes (MCAS) that are selected according to the present conditions of the wireless channel, in order to capitalize on the performance in stipulations of throughput and reliability. Three transmission modes methodology [4] is used. To maximize the throughput, for low E_b/N_0 and to robust transmitter parameters to provide high performance and increase the throughput of the entire system and switch. Hybrid receiver's tender cooperation among a diversity system and multiplexing system is used [4].

III. MIMO MODEL

To have strong signal strength, the signal should transmit multipath channel. Due to scattering, obstacles and thick density of trees loss of signal takes place, due to the loss of signals fading of channel take place and in turn there is variation of SNR also. Thus by using MIMO the coverage and

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channel quality is to improve and also provide improved performance of communication.



Fig 3.1: General idea of MIMO system

Multiple Inputs and Multiple Outputs system uses the array gain to provide average increase of receiver SNR and uses diversity gain in order to improve the coverage and quality of services (QoS) and multiplexing gain increases the efficiency of spectral and capacity. MIMO is an important model in wireless technology such as 4G,LTE and more recently MIMO is found in power link area Multiple sub carriers are orthogonal to each other due to that cross talk is avoided, in data lines MIMO is useful for many transmitter and receiver for ideal transmission and to improve the communication performance.

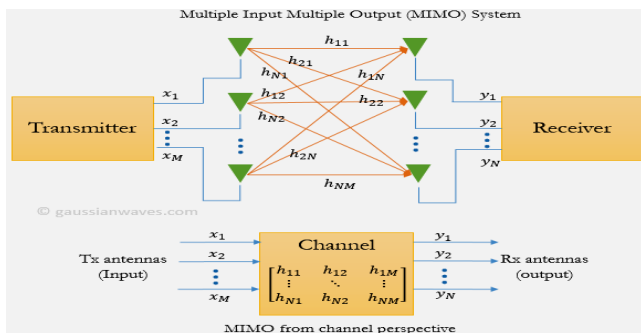


Fig:3.2 Typical MIMO system

The fig 3.2 indicate typical MIMO system which consist of transmitter and receiver sections the transmitter part consist of inputs from x_1, x_2, \dots, x_M and it consist of various channel matrix which is shown by h_{11}, h_{12}, h_{1M} and output section consist of y_1, y_2, \dots, y_N . MIMO technology has attracted wireless skills because it increase data throughput, link array without additional bandwidth and transmit power, ethereal efficiency and achieve diversity grow and enhanced link steadfastness because of this property. MIMO technology is one of the advance technology, capacity of MIMO is more compared to early technology, basic parameters that describe the quality of wireless link is speed, range and reliability and this can be achieved by using MIMO. The figure 3.3 & 3.4 RTL schematic of MIMO (Multiple Input and Multiple Outputs) which as Z_{11}, Z_{12}, Z_{21} and Z_{22} are the transfer matrix format which is diagonal matrix which uses concept of rank indicator in this results shown Z_{11} is 1 and Z_{22} is 1 which is diagonal lies are 1's which indicate complete transformation of information from transmitter to receiver side. The input clk signal is used to oscillates between two states which is high and low which is also used to open and close data alleyway and din1 and din2 are the input1 and input 2 which are 16 bit each and enable and reset which is used to initialize all the registers to zero and it act like cross clock domains and output which consist of real and imaginary part of 16 bit each which is represented by data_out1 and data_out2.

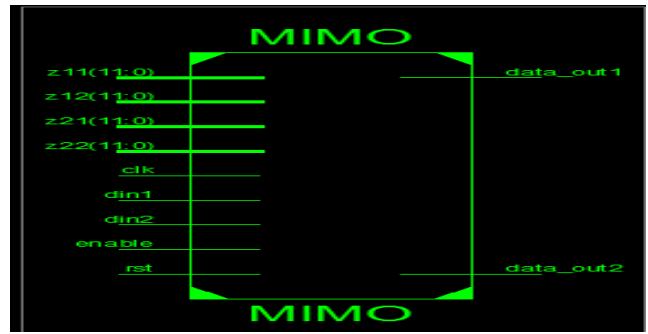


Fig 3.3 RTL Schematic MIMO (Multiple Inputs Multiple Outputs)

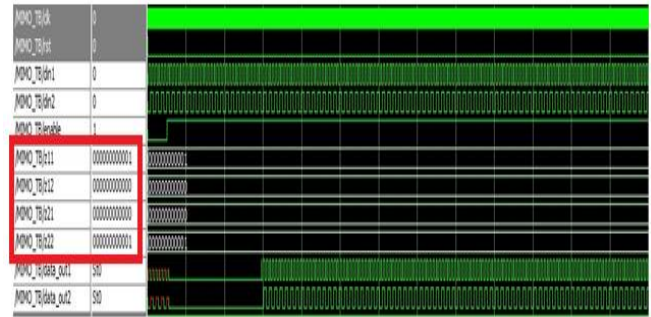


Fig 3.4: Waveform of MIMO

IV. TRANSMITTER

The 2X2 MIMO system consists of various blocks across transmitter and receiver and also has a channel which is noisy channel such as AWGN-additive white Gaussian Noise. The transmitter side consists of source, encoder which is convolution encoder, the interleaver which is a matrix interleaver. The Designer of data communication system looking for many new ways and there is one called forward error correction (FEC) that has been used to enable efficient high quality data communication. In digital communication [18] the FEC technology is in advance and successfully used to reduce the cost and increase performance in variety of cellular communication systems. As noisy channel create number of errors there is increase use of FEC, which improve the system like high data rate, extensive series, bandwidth efficiency, superior power and data consistency.

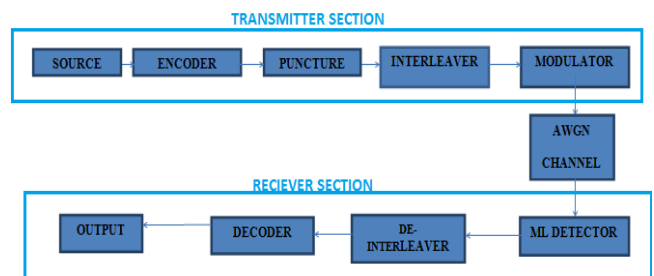


Fig 4.1: Implementation of the 2x2 MIMO system
The transmitter part consists of

1. Convolution Encoder
2. Puncturing
3. Interleaver
4. Modulator

4.1 Convolution Encoder:

The encoder which is used is convolution encoder. Peter Elias is a person who introduced convolutional codes. For

error-correcting codes in a digital communication require some coding process [15]. It uses the concept of polynomial function for a set of sequence and it generates parity symbols. It is basically defined by $[n, k, K]$.

4.2 PUNCTURING:

The output of the convolution encoder is given to the puncturing where some of the parity bits which is output from the convolution encoder is deleted as per the format of matrix which is known as puncturing matrix, the parity bits which are deleted are from code word, puncturing also act as a tradeoff between rate and performance in order to increase the code rate without increasing the complexity from code rate from $1/3$ to $1/2$ or more.

4.3 Interleaving and De-Interleaving:

Interleaving is a method intended for forward error correction with it is more robust with respect to burst errors. Numerous of the error defense coding techniques can correct for small numbers of errors, but cannot correct for errors that occur in groups.

4.4 Modulator:

To have mapping of binary information to analog modulator process is used, this is done to transmit over the communication channel. Changing of frequency, amplitude and phase of sinusoidal waveform can be done by using modulation techniques. In digital communication process signal changes from binary into continuous waveform and vice-versa.

4.5 AWGN Channel:

The Channel is one of the important medium to provide connection between transmitter and receiver. Channel plays a crucial role to send the information, the channel may be wired or wireless. Additive White Gaussian Noise is taken into contemplation for the analysis [12-15]. The noisy channel used is Additive White Gaussian Noise which is used in information coding to imitate the consequence of numerous random processes that occur in nature. Additive because it is added to any noise that may be inherent to the information coding. White because it has regular power diagonally to frequency band of the information coding, Gaussian because it has a normal sharing in frequency and time domain with average time value is zero.

4.6 RESULTS AND IMPLEMENTATION:

The transmitter part consist of various sub-blocks such as convolution encoder which uses for the model of shift register which is uses for impermanent storage of input bits and exclusive-OR logic circuits which produce the coded outputs from the bits currently held in the shift register .Puncturing where some of the parity bits which is outputted from the convolution encoder is deleted as per the format of matrix which is known as puncturing matrix. Interleaving is a method to create a structure more resourceful by arranging data in a non-contiguous manner, the interleaver used is matrix interleaver which fill a matrix with input symbols row by row and then sending the matrix contents to the outputs column by column. The modulator used is QAM (Quadrature Amplitude Modulation) which is used to generate in-phase and q-phase.

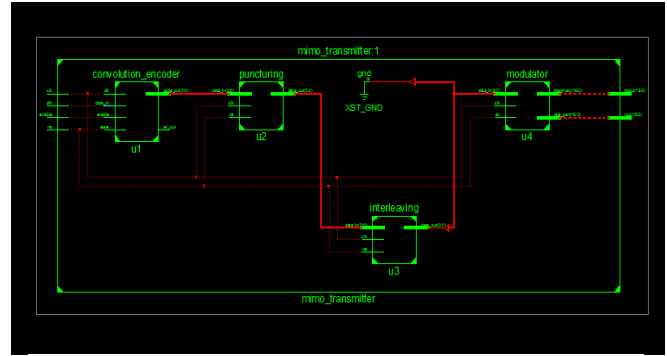


Fig: 4.2 Extraction RTL Schematic of MIMO Transmitter

V. RECIEVER

The Receiver part consists of:

1. ML Detector
2. De-Interleaver
3. Viterbi Decoder

5.1 ML Detector:

The technique of maximum likelihood corresponds too many well-known opinion methods in statistics. In wide-ranging, for a fixed set of data and fundamental statistical model, the process of maximum likelihood selects the set of principles of the model parameters that maximizes the likelihood function. The course of action of ruling the value of one or more parameters for a given statistics which makes the known likelihood distribution a maximum.

5.2 De-Interleaver:

In this project matrix de- interleaver is used which fill matrix with the input sequence row by row and after that transferring the matrix sequence to the output column by column. The use of interleaving must increases the capability of error defense codes to accurate for burst errors.

5.3 Viterbi Decoder:

The popular decoder used for convolution encoding is viterbi decoder. Convolution coding is commonly used in digital communication system, convolution coding is used for bit error correction [13-15]. The main aim of viterbi decoder is to calculate estimation of bit information. As the demand of digital communication increases speedily, the propose of low power viterbi decoder increases.

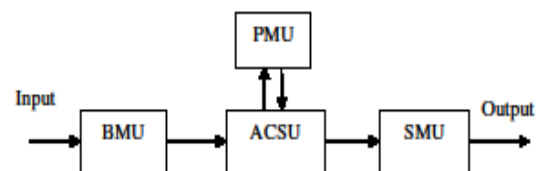


Fig: 5.1 Block diagram of Viterbi decoder

The viterbi decoder is breakdown into three stages:

- Branch metric generator (BMG)
- Add compare select unit (ACSU)
- Survivor Memory Unit (SMU)

The one more name of viterbi algorithm is optimum algorithm, because it will reduce the probability of error.

Viterbi Decoder can be solved in three steps:

1. Find the branch metrics that is weigh the trellis, Branch metric generator is used to measure the distance between transmitted and received ones which are also known as hamming distances.
2. Compute the shortest path from time n to time n-1. During this step survivor path of the input sequence will be observed and updated. It is known as add-compare-select (ACS).
3. Shortest path finally provide trellis state from step 2. The shortest path which is obtained is called survivor path of particular state. The exclusive path which will be obtained is the likely signal path which is obtained by tracing of survivors paths.

5.4 Results and Implementation:

The MIMO model which is used consist of trx1 and trx2 which is used to generate 2X2 MIMO thus extraction of receiver which is shown in fig uses various sub blocks and the decoder which is uses is viterbi decoder since transmitter1 (TRX1) and transmitter2 (TRX2) due to 2 transmitter the sub blocks used are also 2 sub-blocks each.

5.5 NML DETECTOR:

The NML Detector RTL & waveform is shown in fig 5.2 & 5.3. The waveform is shown with real and imaginary 16 bits and waveform of optimal estimate.inp 1 and inp2 and 2X2 MIMO is represented by z11, z12, z21,z22 and clk which act as input clock the clock which is used is master clock, reset and enable input is also used. The done 3,done 4 and all done pins is used to calculate the hamming distance.

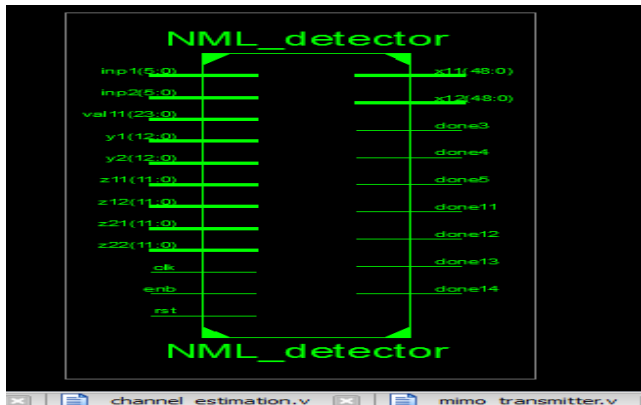


Fig:5.2 RTL Schematic of NML detector

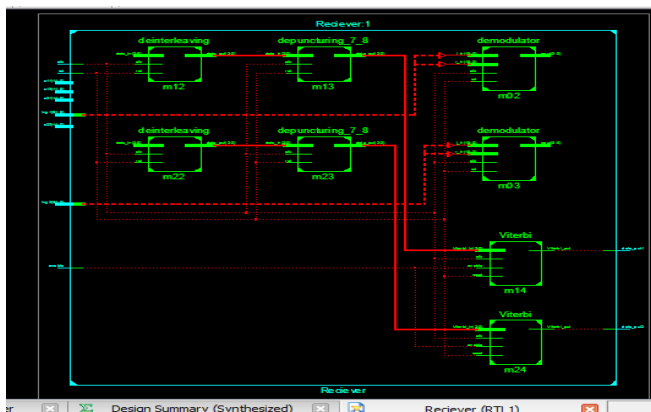


Fig 5.3 Extraction of RTL of receiver

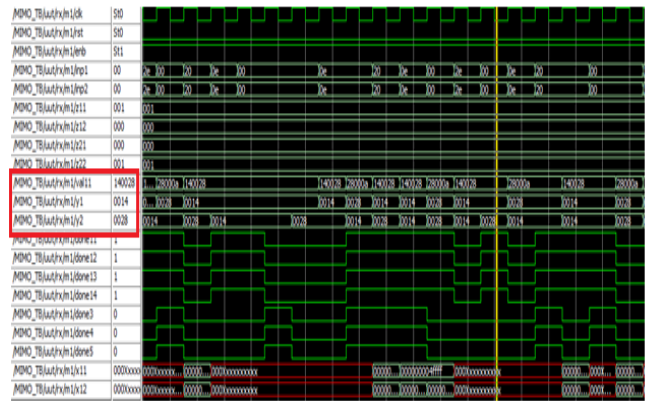


Fig: 5.4 waveform of NML detector

5.6. EXTRACTION OF VITERBI DECODER:

The figure 5.5 indicate extraction of viterbi decoder which consist of branch metrics unit (BMU), Add compare select unit (ACSU) and survivor unit (SMU).

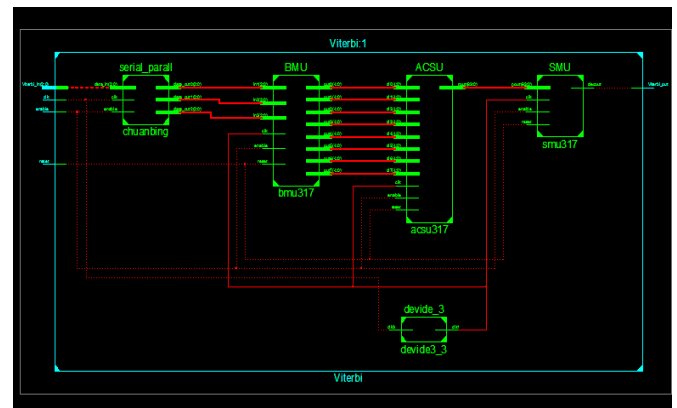


Fig:5.5 extraction of viterbi decoder

5.7 VITERBI DECODER:

Fig: 5.6 indicate waveform of viterbi decoder and BMU (Branch metric Unit) is calculated. Waveform of viterbi input and viterbi output and waveform of BMU.

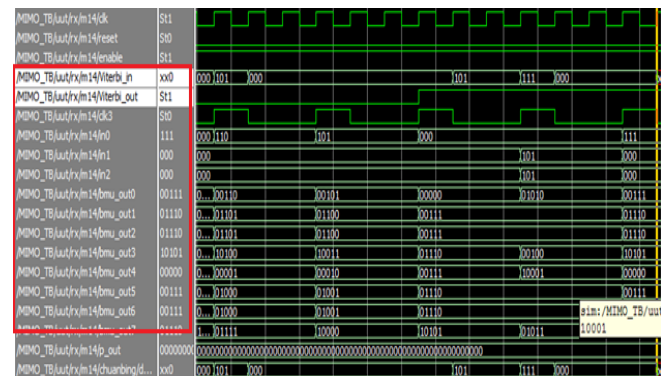


Fig:5.6 waveform of viterbi decoder

VI. DESIGN SUMMARY

6.1 Entire System Design Summary:

The entire design device utilization summary and timing summary shown in table 6.1 when implemented on spartan 3. Here the device utilization is less in number of slices,slice flip flops,input output blocks and in look up tables almost less than half the available device utilization is used. The five gate clock is used.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	11125	89088	12%
Number of Slice Flip Flops	12241	178176	6%
Number of 4 input LUTs	18657	178176	10%
Number of bonded IOBs	7	960	0%
Number of GCLKs	5	32	15%

Speed Grade	-11
minimum period	25.392ns
minimum input arrival time before clock	6.570 ns
maximum output required time after clock	4.892 ns

Table:6.1 Entire System Device Utilization and timing summary

6.2 Comparson of proposed and previous technology:

Module name	Proposed frequency (HZ)	Previous frequency (HZ)	Changes	Proposed slices	previous slices	changes
encoder	613	126	(+487)	13	50	(+37)
interleaver	266	117	(+149)	248	49	(-199)
detector	205	76	(+129)	491	947	(+456)
deinterleaver	119	115	(+4)	267	50	(+217)
decoder	39	80	(-41)	5320	438	(-4882)
entire system	40	52	(-11)	11125	13436	(+2311)

Table 6.2 Comparson table of new technology with old technology

VII. CONCLUSION AND FUTURE SCOPE

The modules are developed using Xilinx, simulated and integrated into FPGA kit done successfully. Hardware prototyping is necessary to pace up the description of computationally and speedily developing current wireless communication system. The FPGA based BERT is a cost effectual compared to other Bit error rate techniques. The MIMO fading channel simulator was successfully premeditated in favor of bit error rate (BER) performance corroboration of a 2X2 MIMO wireless system on FPGA. The speed of hardware prototyping 2X2 MIMO system is more compared to software simulations. The encoder used is convolution encoder which is characterized to trellis diagram which is unfolded sequence of state diagram and Maximum Likelihood is used to find the shortest path successfully. The viterbi decoder is used to find out transmitter sequence by using BMU, ACS and SMU was successfully done. The transmitter and receiver have been completed successfully. As a scope of future work the FPGA based MIMO communication system can also be modified and extended to calculate Bit error rate, SNR etc.

REFERENCES

- [1] Title: On Maximum-Likelihood Detection and Decoding for Space-Time Coding Systems Author(s): Erik G. Larsson, Petre Stoica, Jian Li Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: 50, No 4, April 2002 page 937-943
- [2] Title: Accelerating BER analysis using an FPGA based processing platforms Authors: Eric Lord Malachy Devlin Neil Harold Craig Sanderson Nallatech Ltd Cumbernauld, Glasgow, Scotland Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: 2002
- [3] Title: Accelerating Bit Error Rate Testing Using a system Level Design Tool Author(s): V. Singh, A. Root, E. Hemphill, N. Shirazi and J. Hwang Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: Apr. 2003, pp. 62-68.
- [4] Title: Exploiting Dimensions of the MIMO Wireless Channel: Multidimensional Link Adaptation Author(s): W.C. Freitas Jr, F.R.P. Cavalcanti, A.L.F. de Almeida, R.R. Lopes Publication (place & year if

- book): IEEE Conference Volume no, Month & Year, pages: 2005, page 924-928
- [5] Title: A hardware Gaussian Noise generator using the Box-Muller method and its error analysis Authors: Dong-U Lee, John D. Villasenor, Wayne Luk, Philip H.W. Leong Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: VOL. 55, NO. 6, JUNE 2006
- [6] Title: Modeling and Hardware Implementation Aspects of Fading Channel Simulators. Authors: Amirhossein Alimohammad, Bruce F. Cockburn Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: 57, NO. 4, JULY 2008
- [7] Title: A Flexible Layered Architecture for Accurate Digital Baseband Algorithm Development and Verification Author(s): Amirhossein Alimohammad, Saeed F. Fard, Bruce F. Cockburn Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: 2009, 45-50
- [8] Title: An Efficient FPGA Based hardware implementation of MIMO wireless systems Author(s): Mostafa Wasiuddin Numan, Norbahiah Misran, Mohammad Tariqul Islam Publication (place & year if book): IEEE-International Conference on space science and communication Volume no, Month & Year, pages: 26-27 October 2010 pages 47-50
- [9] Title: Implementation of Convolutional codes Authors: Sajjad Ahmed Ghauri, Hasan Humayun, Muhammad Ehsan ul Hag, Farhan Sohail Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: 2012
- [10] Title: FPGA Implementation of MIMO-OFDM Eigen beam-Space Division Multiplexing Systems for future wireless communication Networks Authors: Nguyen Trung Hieu, Bui Huu Phu, Vu Dinh Thanh, and Yasutaka Ogawa Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: 2013
- [11] Title: Efficient FPGA Implementation of Address Generator for WiMAX Deinterleaver. Authors: Bijoy Kumar Upadhyaya, and Salil Kumar Sanyal Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: VOL. 60, NO. 8, AUGUST 2013
- [12] Title: FPGA-Based Bit Error Rate Performance Measurement of Wireless Systems. Authors: Amirhossein Alimohammad and Saeed Fouladi Fard Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: VOL. 22, NO. 7, JULY 2014.
- [13] Title: Monte Carlo Simulation with Error Classification for Multipath Rayleigh Fading Channel Authors: Liang Dong, Wang Wenbo, Li Yonghua Publication (place & year if book): IEEE Conference Volume no, Month & Year, pages: JULY 2009.
- [14] Title: Single-user MIMO versus multi-user MIMO in distributed antenna systems with limited feedback Authors: Stefan Schwarz, Robert W Heath, Markus Rupp Publication (place & year if book): EURASIP Journal on Advances in Signal Processing 2013, 2013:54
- [15] Title: Viterbi Decoder Architecture for Interleaved Convolutional Code Authors: Jun Jin Kong and Keshab K. Parhi Publication: IEEE, Volume no, Month & Year, pages: 2002.



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