

Leakage Power Reduction and Power Delay Product (PDP) Improvement using Dual Stack Method

Nitesh Kumar Kiran, Khemraj Deshmukh

Abstract— Leakage power reduction of CMOS technology is nowadays a vast challenge. International Technology Roadmap for Semiconductors (ITRS) [1] information that Leakage power consumption can come to dominate total chip power consumption as the technology feature size get smaller. Leakage is a serious problem particularly for CMOS circuits in nanoscale technology. This paper presents the designing and analysis on inverter, chain of four inverters and 4:1 multiplexer circuits with dissimilar types of power gated parameter using low power VLSI design techniques and exhibit the evaluation between different nanometer technologies. In this paper the performance of the conventional inverter circuit, chain of four inverter circuits and 4:1 multiplexer circuit is compared with the performance of the different types of power gated parameters. In the dissimilar types of power gated parameters are good high degree of power reduction is reported. Another factor such as delay and power delay product (PDP) is also been calculated for all the circuits. All the circuits are simulated in HSPICE and delay is calculated using Cosmo scope.

Index Terms— VLSI, power delay product (PDP), Dual stack, state saving technique,

I. INTRODUCTION

In the past, the main concern for the designers of the VLSI circuits was the area, performance and reliability of the design. But through the modern years, as the requirement for the portable devices have gained importance, the main concern for the designers is the power, comparable to the area and speed considerations. The low power VLSI designs have much awareness in the current years with reference to insist for long battery life in portable devices and high heat removal in non-portable devices.

The problem for low power VLSI design can be broadly classified into two major categories: Analysis and Optimization. Analysis is apprehensive to be the accurate estimation of the power or energy dissipation during the different designing phase of the circuit. Analysis techniques differ in their accuracy and efficiency. The accuracy of analysis depends on information available to design a particular design. Optimization is the process of produce the best design, specified an optimization goal, without violate design terms.

The interests in low power chips and systems are driven by both business and technical needs. The industry for low power

consumer electronic products is booming with a rapidly growing market. At the similar time, current generations of semiconductor processing technologies present more rigorous requirements to the power distribution of digital chips due to increased speed, device density, and complexity.

The conventional inverter is a basic circuit, with the help of inverter drawing the chain of four inverter circuit. We are also analyzing 4:1 multiplexer circuit. Its designing as shown in the figure. The main aim of this paper is to reduce the power dissipation and improve the power delay product (PDP) of these circuits using different methods.

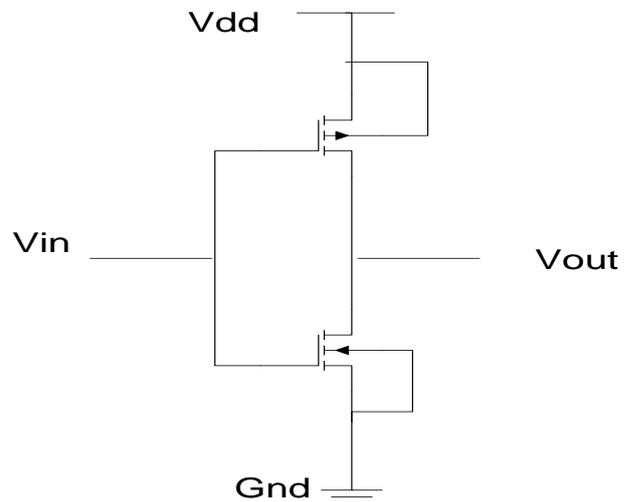


Figure 1: Conventional Inverter

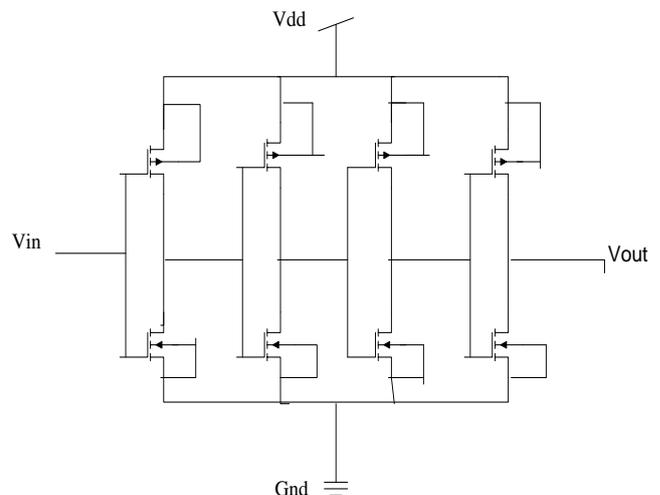


Figure 2: Conventional Chain of Four Inverter Circuit

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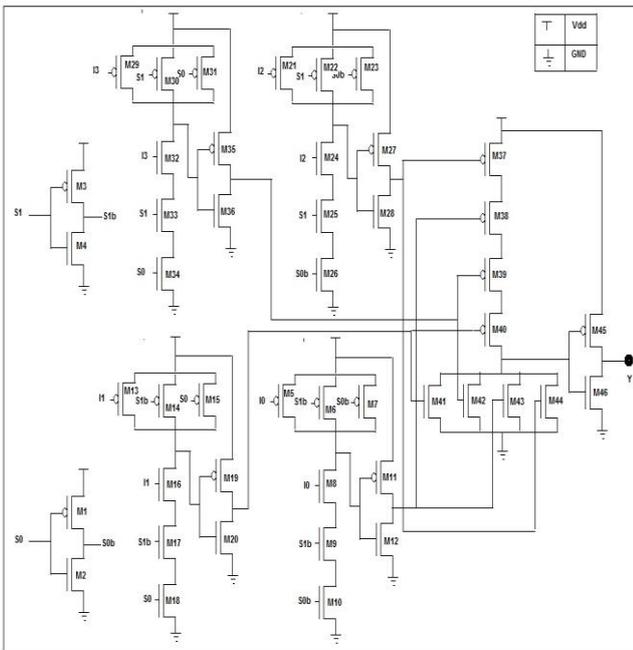


Figure 3: Conventional 4:1 Multiplexer Circuit

II. EASE OF USE

The growth of digital integrated circuits is challenged by higher power spending. The arrangement of high clock speeds, bigger functional integration, and minor procedure geometries has contribute to considerable growth in power density. Scaling helps to increase speed and frequency of operation and hence higher performance.

Leakage power has become a serious concern in nanometer CMOS technologies. Nowadays, leakage power has become a progressively more important issue in processor hardware and software design.

A. Power Dissipation

Power is defined as the rate at which the energy is transferred or exchanged in the circuit. Power dissipation in the circuit is defined as the rate at which the energy is taken from source and is converted to heat.

Advances in CMOS fabrication technology double the number of transistor per chip every two years and double the operating frequency every three years. Consequently, the power dissipation per unit area grow, rising the chip temperature. This extreme temperature reduces the reliability and lifetime of the circuit. Hence, large cooling device and expensive packaging are required to dissipate the extra heat.

B. Sources of Power Dissipation

For the most recent CMOS feature sizes, leakage power dissipation has become an overriding concern for VLSI circuit designer. International technology roadmap for semiconductors (ITRS) reports that leakage power dissipation may come to dominate total power consumption. There are three sources of power dissipation in CMOS digital circuits: dynamic power, short circuit power and leakage power. Previously, the dynamic power was main and the other two parts were negligible. On the other hand leakage power is

Appropriate more and more significant as the CMOS technology goes into the deep submicron scale. At present, all three are main and leakage power is beginning to dominate.

C. Dynamic Power

Dynamic power is the powers compulsory to charge and discharge the load capacitances when transistors switch.

The technique for dynamic power is specified by

$$P_{dynamic} = \alpha C_L V_{DD}^2 f$$

where f is the clock frequency and α is the node transition activity factor.

D. Short-Circuit Power Dissipation

When transistors switch, both nMOS and pMOS networks may be momentarily on at once. This leads to a blip of short circuit current. The short circuit power is known as:

$$P_{short-circuit} = I_{mean} \cdot V_{DD}$$

Where I_{mean} is average short-circuit current. For a symmetric inverter.

$$I_{mean} = \frac{\beta}{12} (V_{DD} - 2V_t)^3$$

E. Leakage Power

Leakage power, also called static power, is owed to the off-state current of a transistor when it is off. Suppose that there are N transistors in a circuit, and I_{offi} is the off-state current of the i_{th} transistor. after that, the whole leakage power of the circuit can be expressed in the following formula:

$$P_{leakage} = V_{DD} \sum_{i=1}^N I_{offi}$$

F. Power Delay Product (PDP)

Power delay product (PDP) is a fundamental parameter which is often used for measuring the quality and the performance of CMOS process and gate design.

$$PDP = C V_{DD}^2$$

III. CHAIN OF FOUR INVERTERS

Basic building blocks of most of the logic circuits are formed by inverter. Inverter is a small and very important circuit in low power designing. It is the basic block of many circuits. Chain of four inverter circuit is realized by placing the four inverter circuit in the series. It is also the basic block of many circuits. Therefore reducing power consumption and improving in inverter and chain of four inverters is very important in low power circuits. The main aim of the project is to reduce the power dissipation and improving the power delay product (PDP) of the circuits.

IV. MULTIPLEXER

Multiplexer is a digital switch. It allows digital information from several sources to be routed onto one output line. The

essential multiplexer has several information input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are input lines and n selection lines whose bit combinations determine which input is selected. Therefore, multiplexer is, many into one and it provides the digital equivalent of an analog selector switch. The 4:1 multiplexer has four inputs and one output. In addition, it has two selection lines. Depending on the two selection lines, one output is selected at a time from among the four input lines.

Table 1: Truth table of 4:1 multiplexer

Selection lines		Inputs				Output
S0	S1	I0	I1	I2	I3	Y
0	0	1	0	0	0	I0
0	1	0	1	0	0	I1
1	0	0	0	1	0	I2
1	1	0	0	0	1	I3

V. LOW POWER TECHNIQUES

Power dissipation of a circuit can be reduced and power delay product (PDP) can be improved by using different techniques.

A. Sleep Approach

The most recognized traditional approach is the sleep approach [2][3]. In the sleep approach, an additional "sleep" PMOS transistor is placed between Vdd and the pull-up network of a circuit and an additional "sleep" NMOS transistor is placed between the pull-down network and Gnd. A sleep inverter is shown in Figure 4

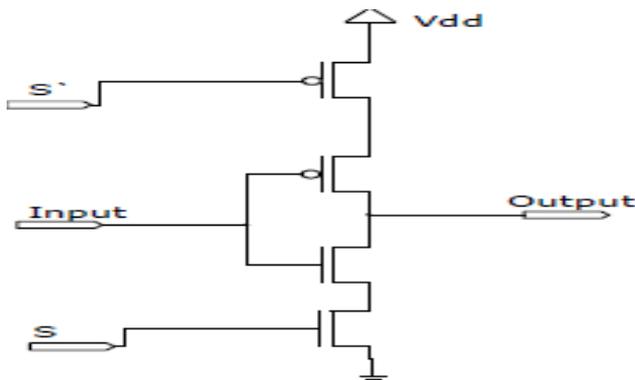


Figure4. Sleep Approach

The sleep transistors are turned off while the logic circuits are not in use. through isolating the logic networks using sleep transistors, the sleep transistor technique significantly reduces leakage power in sleep mode. Though, the added sleep transistors increase delay and area. Also, the pull-up and pull-down networks will have floating values and thus will lose state during sleep mode. These floating values

considerably impact the wakeup time and energy of the sleep technique due to the requirement to recharge transistors which lost state during sleep.

B. Sleepy Stack Approach

Another technique for leakage power reduction is the stack approach, which forces a stack effect by floating down an existing transistor into two half size transistors [5]. Fig 3 shows its structure. As the two transistors are turned off together, induced reverse bias among the two transistors results in sub threshold leakage current reduction. Though, divided transistors raise delay significantly and could limit the usefulness of the approach. The sleepy stack technique combines the sleep and stack techniques. The sleep transistor and the stacked transistor in each network are made parallel. Now the width of the sleep transistors is compact. Changing the width of the sleep transistors may provide additional tradeoffs between delay, power and area.

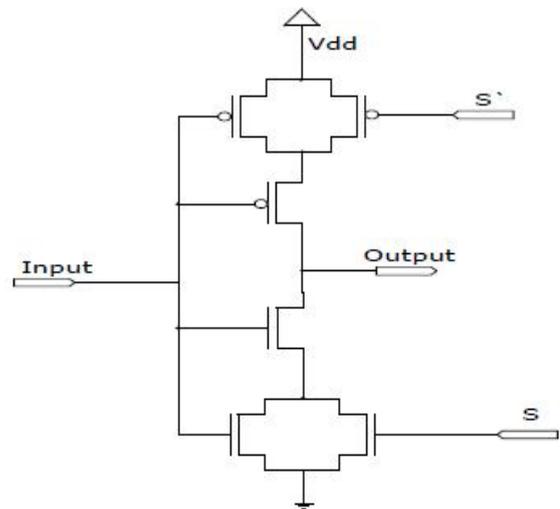


Figure5. Sleepy Stack Approach

The sleep transistors are turned on during active mode and turned off during sleep mode. The sleepy stack structure can reduce the circuit delay in two ways. Primary, as the sleep transistors are always on during active mode so there is always a current flow through the circuit. That's why it gives a faster switching time. The high threshold voltage transistors are used for the sleep transistor and the transistors parallel to the sleep transistor without incurring large delay increase. The delay time is increasing here but it gives low leakage. During sleep mode both the sleep transistors are turned off. But the sleepy stack structure maintains exact logic state, So sleepy stack structure achieves ultra low leakage power consumption during sleep mode while retaining the exact logic state. But the main drawback of this sleepy stack technique, however, is increasing area a lot.

C. Dual Sleep Approach

Another technique called Dual sleep approach [6]. Figure 6 shows its structure, uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. It uses two pull-up sleep transistors and two pull-down sleep transistors.

A. DESIGNING OF INVERTER CIRCUIT

The conventional Inverter Circuit will be designed using the sleep approach, sleepy stack approach, dual sleep approach and dual stack approach and will be compared with the conventional Inverter for the result. The Conventional Inverter which has to be analyzed is shown below:

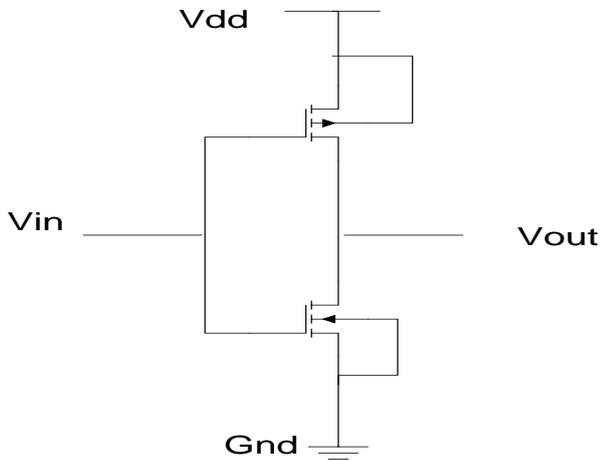


Figure 10: Conventional Inverter

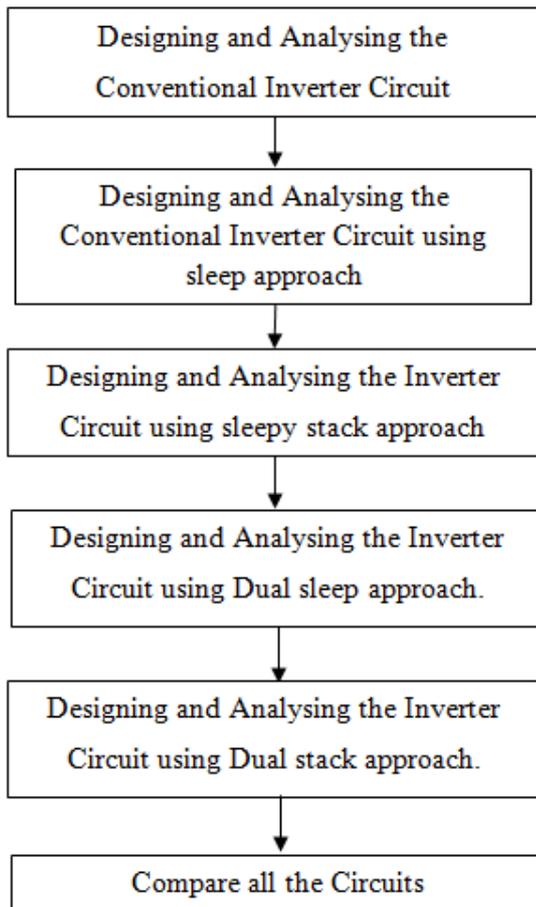


Figure 11: Flow graph for designing and analyzing of Inverter Circuit

B. DESIGNING AND ANALYSING CHAIN OF FOUR INVERTER CIRCUIT:

The process for designing the Chain of four Inverter circuit is exactly the same as that of the Inverter circuit. The Chain of four Inverter circuit is designed in sleep approach, sleepy stack approach, dual sleep approach and dual stack approach to analyze it for the better outcome and better performance of the circuit.

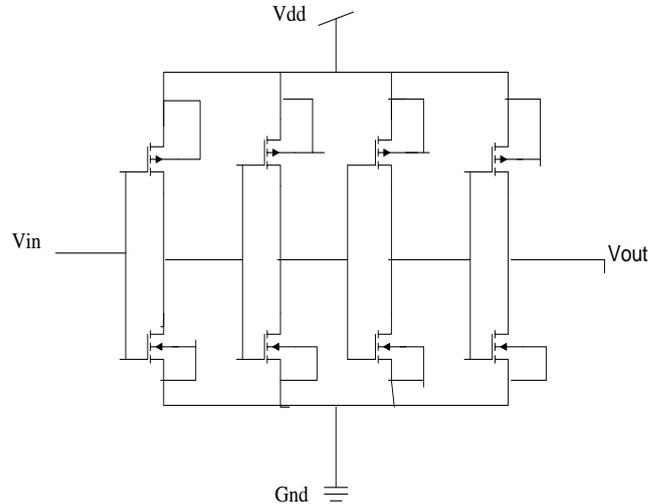


Figure 12: Conventional Chain of Four Inverter Circuit

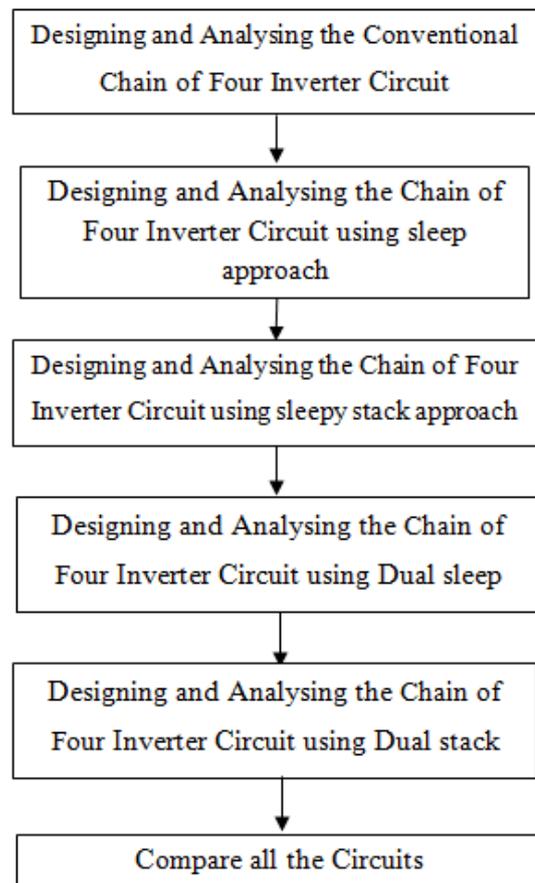


Figure 13: Flow graph for designing and analyzing of Chain of four Inverter Circuit

VII. RESULT AND DISCUSSION

C. DESIGNING AND ANALYSING 4:1 MULTIPLEXER CIRCUIT:

The process for designing the 4:1 Multiplexer circuit is same as that of the Inverter circuit. The 4:1 Multiplexer circuit is designed in sleep approach, sleepy, dual sleep approach and dual stack approach to analyze it for the better outcome and better performance of the circuit which is one of the main component of the Arithmetic and Logic Unit (ALU) of all the electronic devices.

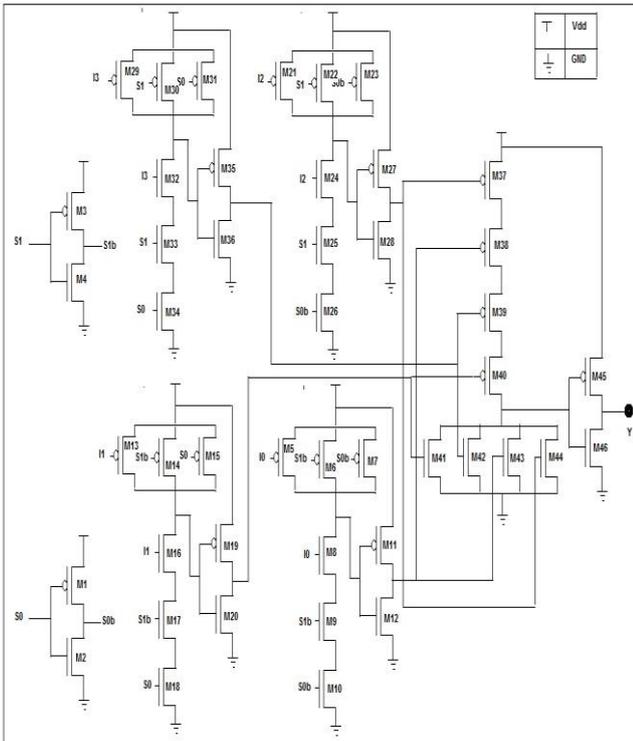


Figure 14: Conventional 4:1 Multiplexer Circuit

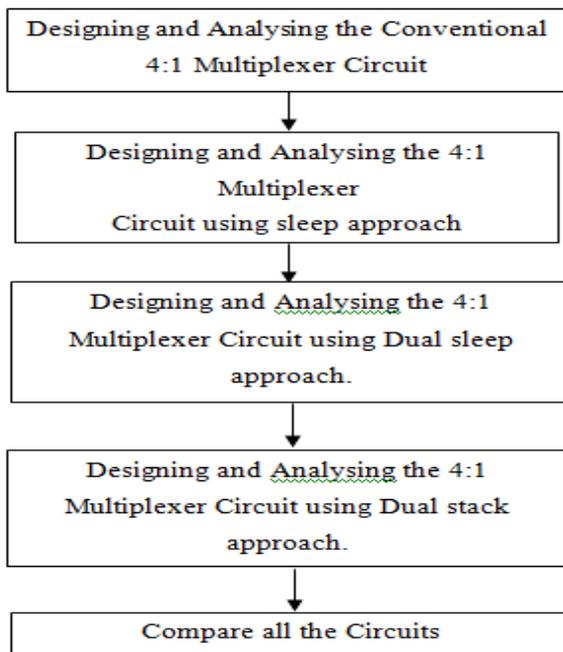


Figure 15: Flow graph for designing and analyzing of 4:1 Multiplexer Circuit

A. INVERTER

The conventional Inverter circuit is designed using the Sleep Approach, Sleepy Stack Approach, Dual Sleep Approach and Dual Stack Approach, the following result is obtained.

Average Power Dissipation Graph for Inverter Circuit using different methods

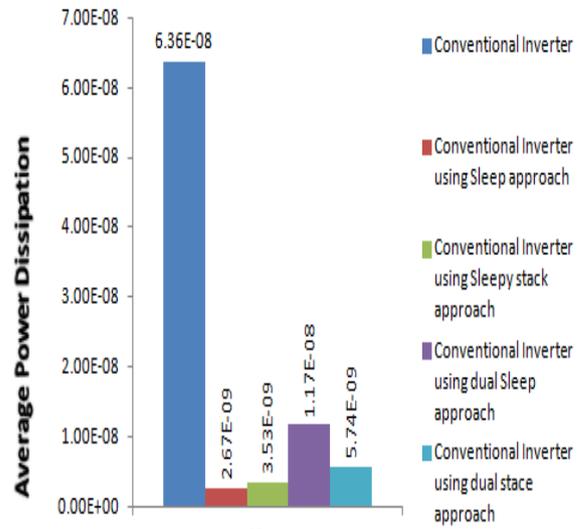


Figure 16: Combined graph for the comparison of all the methods used in designing Inverter Circuit

Delay Graph for Inverter Circuit using different methods

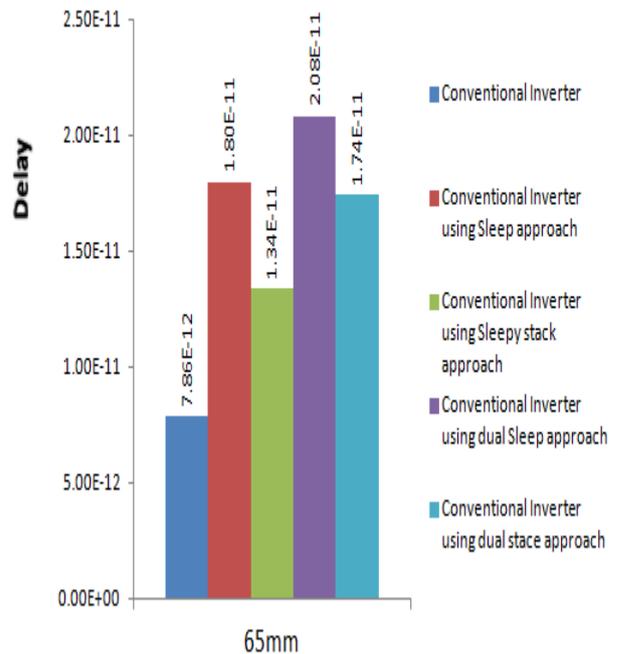


Figure 17: Combined graph for the comparison of all the methods used in designing Inverter Circuit

Power Delay Product (PDP) Graph for Inverter Circuit using different methods

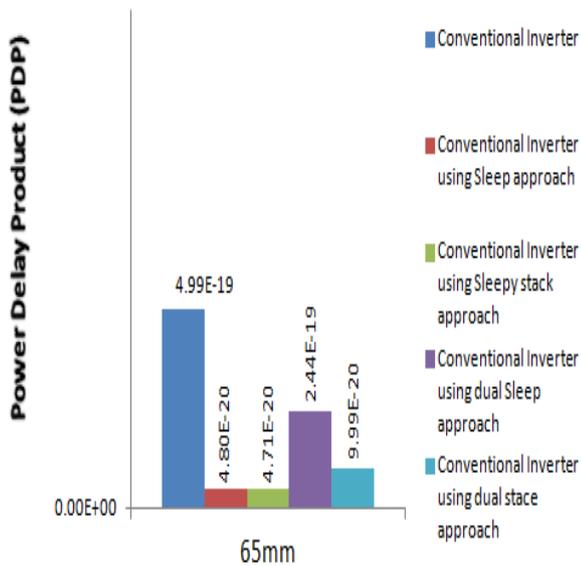


Figure 18: Combined graph for the comparison of all the methods used in designing Inverter Circuit

A. CHAIN OF FOUR INVERTER CIRCUIT

The Chain of four inverters is also one of the main components of most of the electronic devices whose performance has also to be improved. Using the same methods used in analyzing the Inverter is also implemented in the Chain of four inverters and the following result is obtained.

Average Power Dissipation Graph for Chain of 4 Inverter Circuit using different methods

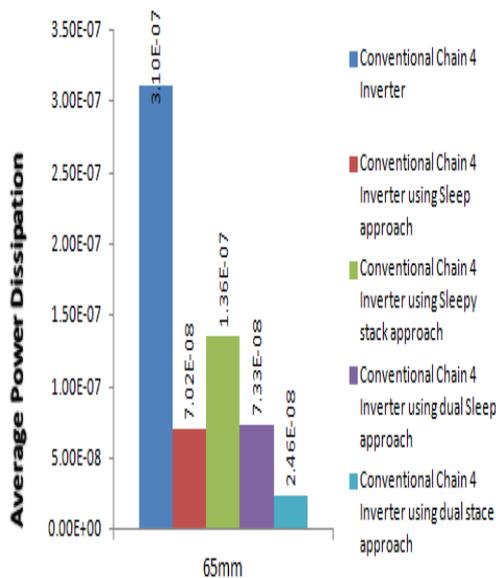


Figure 19: Combined graph for the comparison of all the methods used in designing Chain of Four Inverter Circuit

Delay Graph for Chain of 4 Inverter Circuit using different methods

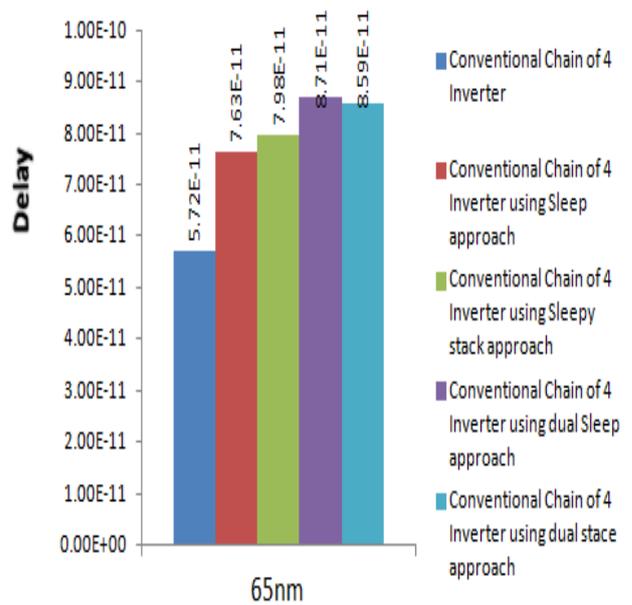


Figure 20: Combined graph for the comparison of all the methods used in designing Chain of Four Inverter Circuit

Power Delay Product (PDP) Graph for Chain of 4 Inverter Circuit using different methods

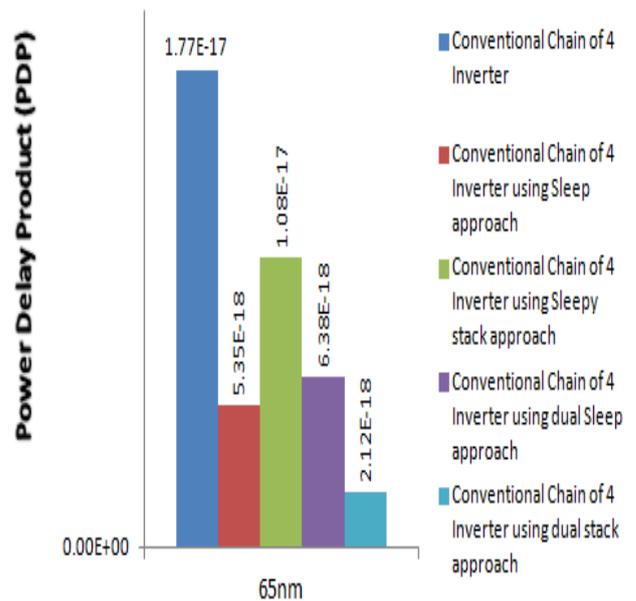


Figure 21: Combined graph for the comparison of all the methods used in designing Chain of Four Inverter Circuit

B. 4:1 MULTIPLEXER CIRCUIT

The 4:1 Multiplexer is also one of the main components of most of the electronic devices whose performance has also to be improved. Using the same methods used in analyzing the 4:1 Multiplexer is also implemented in the Chain of four inverters and the following result is obtained.

Average Power Dissipation Graph for 4x1 Multiplexer Circuit using different methods

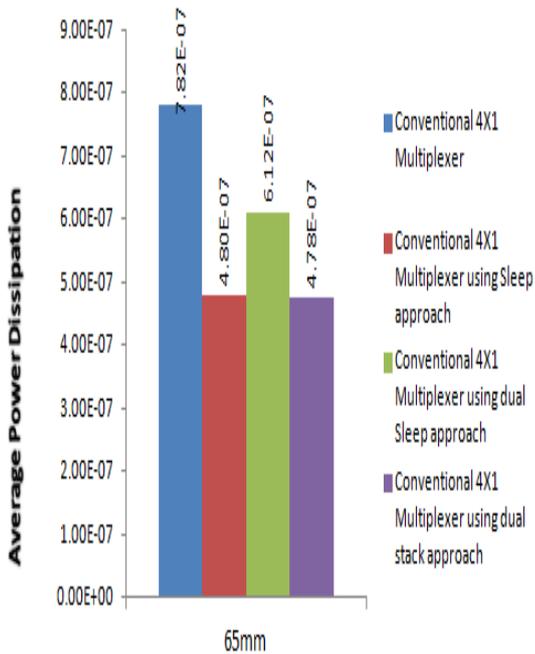


Figure 22: Combined graph for the comparison of all the methods used in designing 4:1 Multiplexer Circuit

Power delay Product(PDP) Graph for 4X1 Multiplexer Circuit using different methods

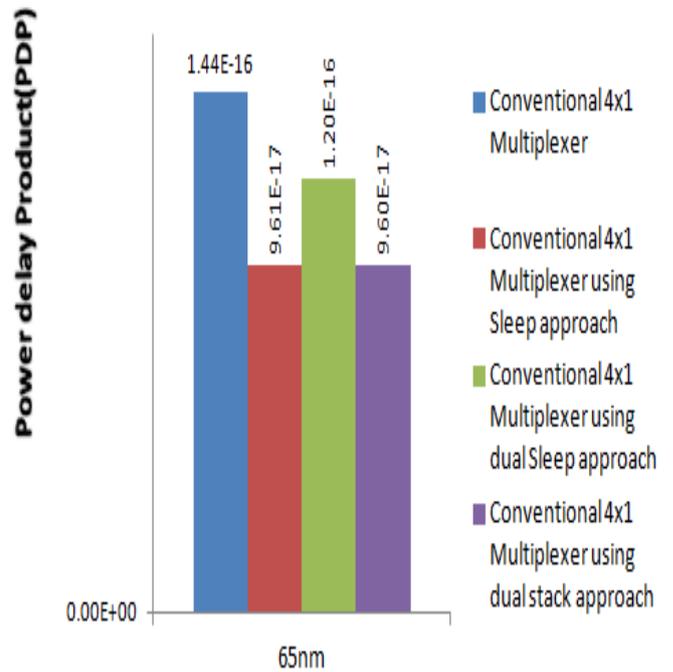


Figure 24: Combined graph for the comparison of all the methods used in designing 4:1 Multiplexer Circuit

Delay Graph for 4X1 Multiplexer Circuit using different methods

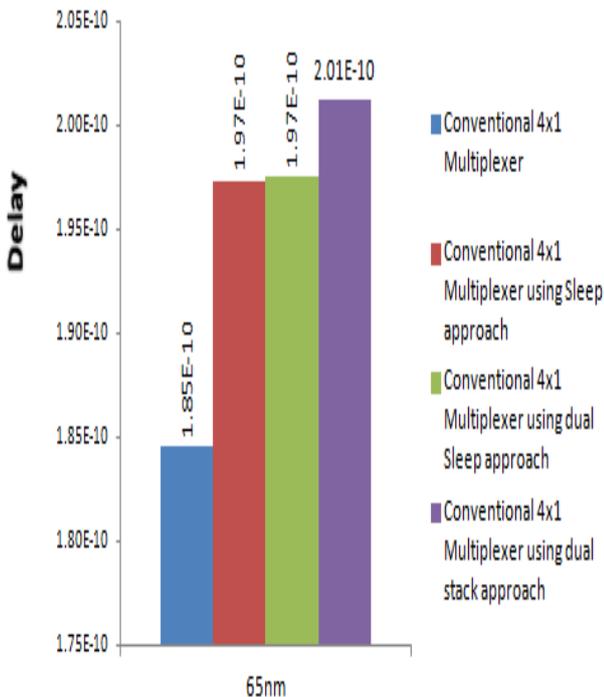


Figure 23: Combined graph for the comparison of all the methods used in designing 4:1 Multiplexer Circuit

VIII. CONCLUSION

From the above following results have been drawn, which show that the Conventional Inverter, Conventional Chain of Four Inverters Circuits and the 4:1 Multiplexer Circuit can be implemented using the above techniques for the better performance of the circuits.

Table 1: Percentage Improvement in the parameter of Power Dissipation, Delay and Power delay product (PDP) with respect to Conventional Inverter

Method (65nm)	Average Power Dissipation	Delay	Power Delay Product (PDP)
Sleep Approach	95.79%	-128%	90.38%
Sleepy Stack	94.44%	-69%	90.56%
Dual Sleep	81.57%	-165%	51.14%
Dual Stack	90.96%	-121%	80.00%

Table2: Percentage Improvement in the parameter of Power Dissipation, Delay and Power delay product (PDP) with respect to Conventional Chain of Four Inverters

<i>Method (65nm)</i>	<i>Average Power Dissipation</i>	<i>Delay</i>	<i>Power Delay Product (PDP)</i>
<i>Sleep Approach</i>	77.37%	-33.40%	69.82%
<i>Sleepy Stack</i>	56.23%	-39.52%	38.94%
<i>Dual Sleep</i>	76.36%	-52.32%	64.00%
<i>Dual Stack</i>	92.05%	-50.20%	88.06%

Table 3: Percentage Reduction in Power Dissipation, Delay and Power Delay Product (PDP) in all the methods with respect to Conventional 4:1 Multiplexer Circuit

<i>Method (65nm)</i>	<i>Average Power Dissipation</i>	<i>Delay</i>	<i>Power Delay Product (PDP)</i>
<i>Sleep Approach</i>	38.59%	-7.31%	33.26%
<i>Dual Sleep</i>	21.72%	-7.02%	16.67%
<i>Dual Stack</i>	39.08%	-9.03%	33.34%

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