International Journal of Engineering and Technical Research (IJETR)
ISSN: 2321-0869 (O) 2454-4698 (P), Volume-4, Issue-4, April 2016

A Bypass Circuit for 802.11n RF LNA/Switch Module

Shen-Whan Chen, Chi-Ming Chou, Yin-Wei Chang, Rey-Chue Hwang, Shuming T. Wang

***Abstract*—In this paper, a new method is proposed to implement the bypass circuit for 802.11n RF LNA/Switch modules. Unlike traditional method, which uses decoder for mode and RF switch control, this method adopts diodes only for controlling. Also, less than -10dB input and output return loss under bypass mode operation can be achieved by using this method without introducing extra impedance matching circuit which would increase the die size of a MMIC chip. This method provides a better accuracy of signal attenuation control and less die size implementation for bypass mode operation.**

***Index Terms*—Low Noise Amplifier, RF Switch, Bypass Mode, 802.11n**

I. INTRODUCTION

In LNA/Switch module design [1-8] for 802.11n, a RF bypass channel will be implemented to receive signal in case when input receiving signal becomes too large that would saturate the transistors of low noise amplifier. -6dB signal attenuation is typically implemented for RF bypass channel. Although, the RF bypass circuit shares the same RF switch channel to antenna as well as to transceiver with the low noise amplifier's circuit, but in between they are two separate RF circuits if it is implemented by using the traditional method. Input and output impedance matching circuit is typically not implemented due to the inductors have to be used for both input and output sides. In this case, it will result in a typical -8dB input and output return loss when operating under the bypass mode. The mismatch of impedance may increase the unnecessary coupling of the reflected signal to other places. Also, traditionally, digital decoder is used for mode switching control.

In this paper, we implement a new method for the RF bypass channel. This new approach adopts a patented method of using diode [9], instead of digital decoder, for mode switching and for the control of RF switch. Beside, extra inductors are not needed to be used for input and output match. This new method can not only save the precious real estate of MMIC chip, but also not increase the I/O counts of control signal. Input and output match for bypass mode RF circuit is implemented by sharing the existing input and output matching circuit of the low noise amplifier. That is the reason why chip size is not increased and the input as well as the output return losses are improved to be about -12dB.

Shen-Whan Chen, Department of Communication Engineering Department, I-Shou University, Kaohsiung City, Taiwan, R.O.C., +88676577711-6763.

Chi-Ming Chou, Department of Communication Engineering Department, I-Shou University, Kaohsiung City, Taiwan, R.O.C., +88676577711-6652.

Yin-Wei Chang, International College, Xiamen University, Xiamen City, Fujian, China, +86-592-2086139.

Rey-Chue Hwang, Department of Electrical Engineering, I-Shou University, Kaohsiung City, Taiwan, R.O.C., +88676577711-6622.

Shuming T. Wang, Department of Electrical Engineering, I-Shou University, Kaohsiung City, Taiwan, R.O.C., +88676577711-6624.

II. CIRCUIT DESIGN

In this research, the schematic circuit of low noise amplifier module is shown in Fig. 1. The EFET (Enhancement Field Effect Transistor) is used for the receiving-signal amplification. Fig. 2 shows the corresponding low noise amplifier MMIC chip design.

In the schematic circuit, depletion mode FET, SW3, SW4, and SW5 are used for the implementation of bypass circuit. Diodes, instead of decoder, are used for the control of mode operation. When CR=L(Low), VB=L, and CT=H(High), the system is in transmitting mode and signals transmits through SW2. Under this mode, SW1, SW3, SW4, SW5, SW6 and EFET are turned off and considerable amount of isolation is required. In this design, -38dB isolation between transmitting to receiving has been achieved. When CR=H, VB=H, and CT=L, the module operates under normal receiving condition and EFET amplifies signals with 2.3dB noise figure.

When system detects the receiving signals exceeding -20dBm, the module is switched to bypass mode in order to avoid a saturated EFET to be happened. Under bypass mode, CR=H, VB=L, and CT=L, SW2, SW6 and EFET are turned off as well as SW3, SW4 and SW5 are turned on. SW4 is the RF switch for receiving signals to pass through. Its FET size is selected to attenuate signals by an amount of 6dB. Unlike all other designs [1-8], to achieve less than -10dB input and output return losses, extra inductive matching components were used. If not, reflected signals will cause signals attenuation to be sensitive to source and load impedance. In this design, additional SW3 and SW5 are added to improve impedance match. These switches can use very small sizes of depletion mode FETs (50um total gate width is used for each) which make the increment of dies size almost nothing. Under bypass mode operation, SW3 and SW5 are turned on and input and output matching are improved with the help of L1 and L2. Since L1 and L2 are necessary for LNA's noise impedance match and output impedance match, the improved impedance match for bypass mode is achieved without using any extra inductive components. Due to very small size of DFETs, SW3 and SW5, these additional switching RF channels cause very small shunt admittance load to the main LNA RF channel, which practically does not affect noise and output impedance match of the main LNA receive RF channel.

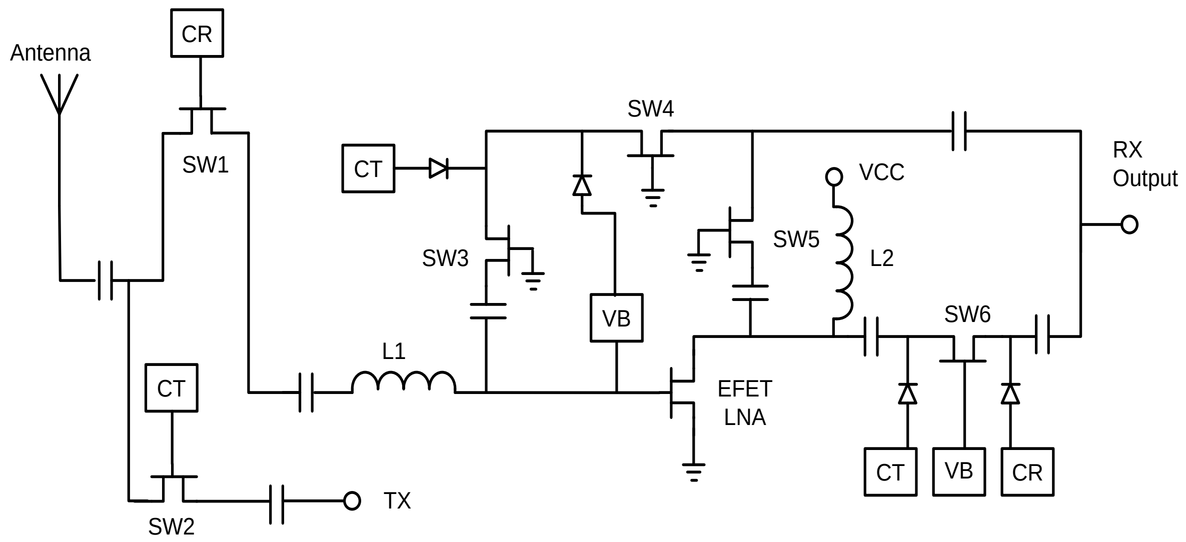

Fig. 1. Schematic circuit of low noise amplifier module.

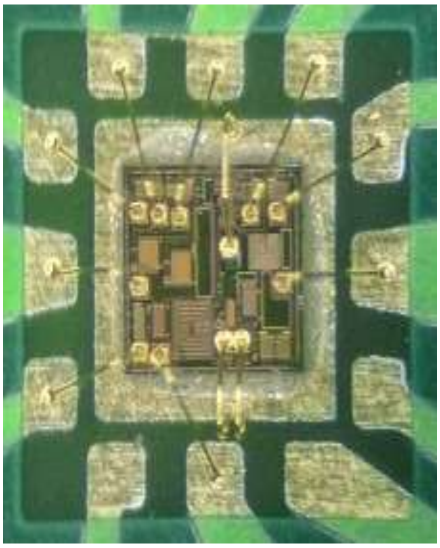

Fig. 2. MMIC chip of low noise amplifier module.

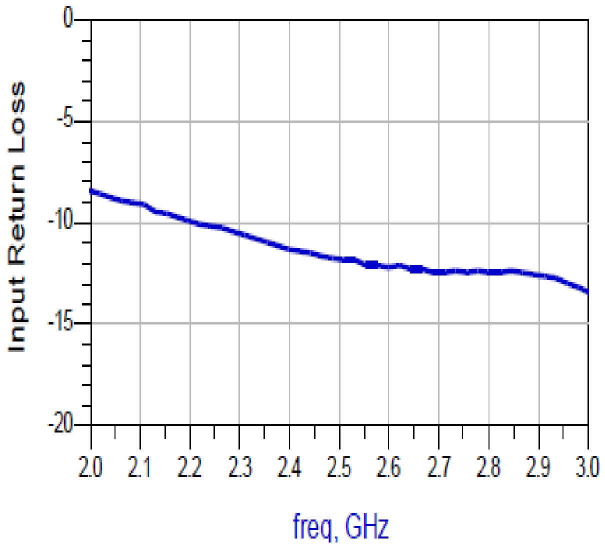

Fig. 3. Measured input return loss of bypass circuit.

III. Experiments

This new LNA module is implemented by using 0.5um E/D FET GaAs technology. Table 1 shows the operating conditions and measurement results. The measured input return loss, output return loss, and gain of bypass circuit are depicted in Fig. 3, Fig. 4, and Fig. 5, respectively. After de-embedding, the actual attenuation of bypass circuit is -7.3dB. Larger size of FET can be used for SW4 to have attenuation become -6dB. Under bypass mode operation, only 0.2uA current is drawn from power supply. In Table 1, -6.2dB input return loss for RX mode seems to be poor, but this is a compromise based on dies size and gain consideration. Otherwise, degenerative inductor has to be used for its improvement and both gain and dies size would be degraded.

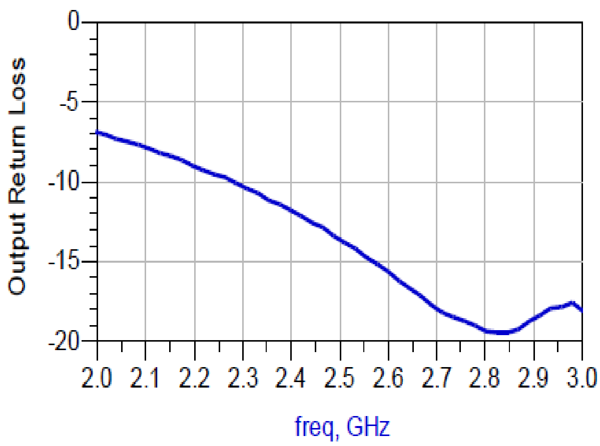

Fig. 4. Measured output return loss of bypass circuit.

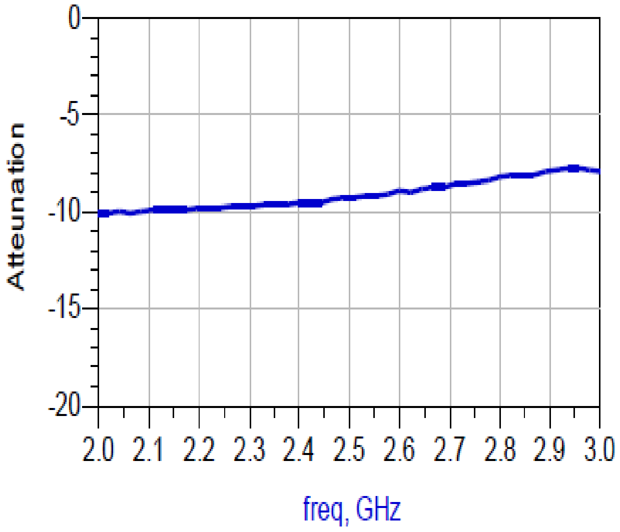

Fig. 5: Measured gain of bypass circuit.

Table 1: Measured results of LNA module.

T=25℃, VDD=3.6V, VCX=3.1V			
RX Mode	**2.45 GHz**	**RX Bypass Mode**	**2.45 GHz**
Gain (9mA)	13.02 dB	Insertion Loss	-7.3 dB
Gain (7mA)	12.57 dB	ANT Port Return Loss	-11.3 dB
Noise Figure	2.3 dB	RX Port Return Loss	-12.2 dB
ANT Port Return Loss	-6.2 dB	VDD Supply Current	0.2 uA
RX Port Return Loss	-15.5 dB		
LNA Current	205 uA		
TX Mode			
Insertion Loss	-0.3 dB		
TX to RX Isolation	-38 dB		
ANT Port Return Loss	-21 dB		
TX Port Return Loss	-21 dB		

IV. Conclusion

Diode control instead of decoder is used for the design of a LNA module for 802.11n application. Compare these two methods, diode and decoder method, decoder's digital output control voltage levels will be lower than diode control method, since power supply voltage can be applied directly for switch control by using diode control method. This gives diode control a better choice method in terms of the RF performance of RF switches. Besides, diode control method consumes less real estate if compared with decoder method. Also, in this design, a new approach is adopted to improve the input and output return loss of the bypass circuit. This new approach has the advantage of not using any extra inductors, just simply borrowing the inductors that are necessary to be used for the LNA circuit.

Acknowledgment

This work was supported by the Ministry of National Science and Technology of Taiwan, Republic of China under contract No. MOST-103-2221-E-214-050.

References

[1] J. S. Yao, X. P. Sun, B., "1.5–2.7 GHz ultra low noise bypass LNA," *2014 IEEE International Microwave Symposium* (*IEEE MTT-S*), pp. 1-3, 2014.
[2] H. K. Lee, H. M. Fuad, "A high linearity, low noise amplifier module integrated with fail-safe bypass switch for tower mounted amplifier application," *2011 European Microwave Integrated Circuits Conference (EuMIC)*, pp. 268-271, 2011.
[3] Y. H. Chow, T. Chong, Z. Hasan, C. C. Loh, T. L. Tan, E. C. Chew, "A miniature dual-band low-noise amplifier module for IEEE 802.11 b/g/a WLAN applications," *2005 IEEE International Microwave Symposium Digest (IEEE MTT-S)*, pp. 2, 2005.
[4] Z. Hasan-Abrar, Y. H. Chow, Y. W. Eng, "A low-voltage, fully-integrated (1.5-6) GHz low-noise amplifier in E-mode pHEMT technology for multiband, multimode applications," *2008, European Microwave Integrated Circuit Conference (EuMIC 2008)*, pp. 306 - 309, 2008.
[5] S. Kumar, M. Vice, H. Morkner, L. Wayne, "Enhancement mode PHEMT low noise amplifier with LNA linearity control (IP3) and mitigated bypass switch," *2002 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 213 - 216, 2002.
[6] H. Morkner, M. Frank, S. Yajima, "A 1.7 mA low noise amplifier with integrated bypass switch for wireless 0.05-6 GHz portable applications," *2001 IEEE International Microwave Symposium Digest (2001 IEEE MTT-S)*, pp. 293-296, 1, 2001.
[7] S. Kumar, M. Vice, H. Morkner, W. Lam, "Enhancement mode GaAs PHEMT LNA with linearity control (IP3) and phased matched mitigated bypass switch and differential active mixer," *2003 IEEE International Microwave Symposium Digest (2003 IEEE MTT-S)*, pp. 1577-1580, 2003.
[8] G. Watanabe, H. Lau, R. Holbrook, K. Leung, "Low noise amplifier design for CDMA receivers," *IEEE Radio and Wireless Conference, 2001(RAWCON 2001)*, pp. 85 - 88, 2001.
[9] S. W. Chen, S. M. Wang S. M., "The circuit design method of low-current front-end switch used in handset," Patent, I285977, Taiwan, R.O.C.

Shen-Whan Chen, received his Ph.D degree in Electrical Engineering from University of Illinois at Chicago. Currently, he is an associate professor of Communication Engineering Department, I-Shou University. His research interests include the areas of signal processing, microwave engineering, high frequency circuit design.

Shuming T. Wang, received his Ph.D degree in Electrical Engineering Department, Marquette University U.S.A. Currently, he is an associate professor of Electrical Engineering, I-Shou University. His research interests include the areas of microwave engineering, high frequency circuit design, acoustic wave device design.

Chi-Ming Chou, was a master student of Communication Engineering Department, I-Shou University. His research interests include the areas of microwave engineering and high frequency circuit design.

Yin-Wei Chang, is an assistant professor of International College, Xiamen University, Xiamen city, Fujian, China. His research interests include the areas of signal analysis and commercial application.

Rey-Chue Hwang, received his Ph.D degree in Electrical Engineering from Southern Methodist University, Dallas, TX, in 1993. Currently, he is a full professor of Electrical Engineering Department, I-Shou University, Taiwan, R.O.C. Dr. Hwang has published more than 250 papers in various journals and conferences in the areas of artificial intelligent system, signal processing and fuzzy control. He is now a Fellow of IET and a senior member of IEEE. He chartered the IEEE CIS Chapter, Tainan Section and served as the co-chair and chair from year 2004 to year 2009.