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Low Power and High Performance Dynamic CMOS XOR/XNOR Gate Design Using Body Bias Technique

Mukendra Kumar, Khemraj Deshmukh

***Abstract*— This thesis presents a novel thirteen transistor dynamic XOR/XNOR gate intended for advanced microprocessor inbuilt arithmetic and logic unit (ALU). The objectives are to reduce power consumption through dynamic body bias that reduces the threshold of dynamic gate. Traditional dynamic N-Type, dynamic P-Type and dynamic hybrid type is designed and compare with proposed on the basis of following parameter like leakage power, dynamic power, and layout area. Proposed method utilizes the concept of input body to source bias voltage approach to improve the performance of dynamic XOR//XNOR. It is observed that the new design has lower power dissipation and small layout area. The Monte Carlo simulation of dynamic power consumption also performed to observe the robustness of design against temperature variation.**

***Index Terms*— Body Bias, Dynamic power, Layout Area, XOR/XNOR.**

I. INTRODUCTION

Highly scaled chip design using CMOS technology have made it possible to design very dense ALU offers high speed at low power consumption. To obtain this goal, the feature size of CMOS devices has been drastically scaled to nanometre dimensions. Power dissipation and chip density have become the key limitations in many designs as nanoscale devices are becoming a reality at rapid pace. Dynamic XOR/XNOR gates essential blocks in various CMOS circuits especially circuits used for performing arithmetic and logical operations in high speed data processing device such as adders, multipliers, word line selection logic, multiplier and comparators [1–4]. This block is a part of the complex function, so influencing the overall delay and power consumption of the entire system [4]. The dynamic power consumption proportional to the square root of supply voltage whiles the leakage power dissipation proportional to the supply voltage.

The dynamic XOR gate is one of the most important components of arithmetic and logic unit used in microprocessor. This plays an important role in Embedded system and SoC (silicon on chip) to design ALU in small die area that reduce manufacturing cost. This system inbuilt ALU occupy more area on silicon chip that dissipate more heat and elevate the temperature of chip. This thing degrades the performance of system. In order to save the chip heat sink is needed that release the internal heat to external environment.

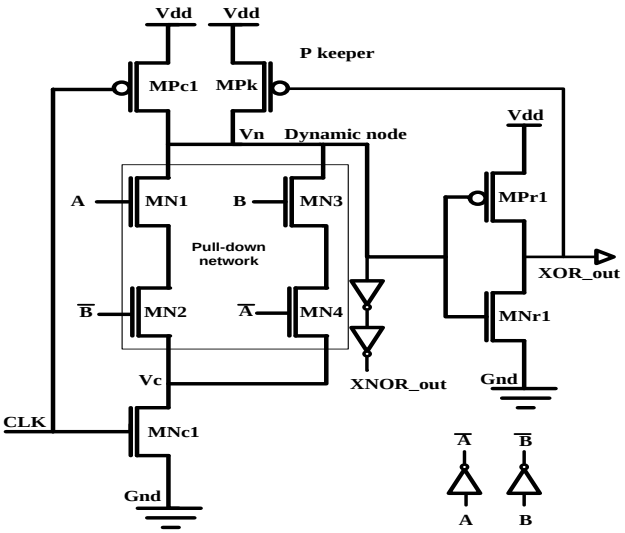
As the operating frequency of dynamic XOR improves, dynamic power consumption becomes dominant that introduce heating problem as mentioned above. To overcome this problem, dynamic XOR gate proposed with minimum delay and smaller power consumption.

II. PREVIOUS WORK

A. Dynamic XOR/XNOR using NMOS (DXN)

The dynamic XOR gate uses only NMOS transistors for evaluation network design. "Fig." 1 shows the design of dynamic XOR/XNOR using NMOS (DXN). DXN provides output XOR and XNOR signal utilizing pull-down NMOS for evaluation [4, 15].

In this design series combination of NMOS transistor pair MN1, MN2 and NMOS transistor pair MN3, MP4 are connected in parallel. Here additional inverters are required to obtain inverted input of input vector (A, B). During precharge phase, dynamic node Vn is charged to supply voltage through transistor MPc1 and XOR_out set to low voltage. During evaluation phase, if input vectors (0, 1) or (1, 0) is applied, dynamic node is discharged to low voltage and XOR_out is charged to high voltage.



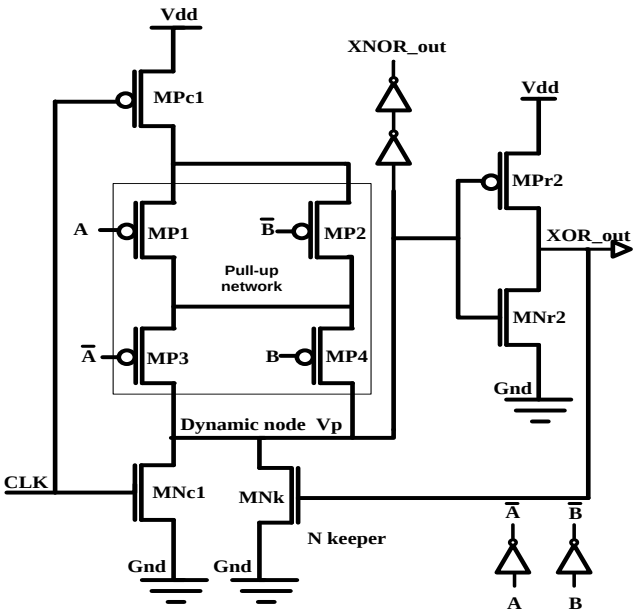
"Fig."1 Dynamic XOR/XNOR using NMOS pull-down network (DXN)

Mukendra Kumar, Electronics & Telecommunication, C.S.V.T.U Bhilai/ Shri Shnkaracharya Group Of Institutions(FET) , Raipur, India, 9753227225.

Khemraj Deshmukh, , Electronics & Telecommunication, C.S.V.T.U Bhilai/ Shri Shnkaracharya Group Of Institutions(FET) , Bhilai, India,, 9755985151.

B. Dynamic XOR/XNOR using PMOS (DXP)

This dynamic XOR gate replace NMOS evaluation network by PMOS evaluation network. "Fig."2 shows the design of dynamic XOR/XNOR using PMOS (DXP). Here, DXP generates output XOR/XNOR signal using pull-up PMOS network in evaluation phase. But DXP offers superior leakage characteristics as compared to DXN because of the higher barrier height of holes tunneling from the conduction band than the electron tunneling form the valance band [9, 15]. Therefore, PMOS transistor produces smaller gate leakage current. But the evaluation speed of the DXN is faster than the DXP due to higher mobility of electron than the holes ($\mu_e<\mu_h$). So, DXN consumes higher power at a cost of higher speed than DXP.

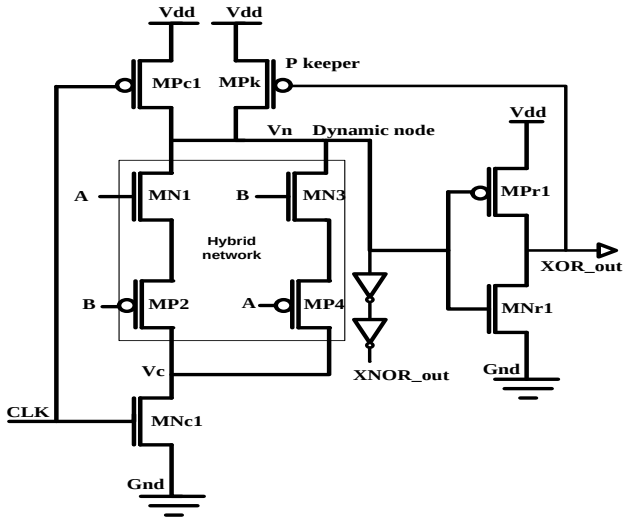


"Fig."2 Dynamic XOR/XNOR using PMOS pull-up network (DXP)

C. Dynamic XOR/XNOR using Hybrid network (DXH)

Previously existing DXN and DXP design, either offer higher speed or offer smaller leakage power. But, both are equally important in single design. Therefore, DXH is designed to obtain this design objective. "Fig."3 shows the design of dynamic XOR/XNOR using hybrid of NMOS and PMOS (DXH). The hybrid network is placed in the PDN which is designed using NMOS and PMOS [5, 6, and 15]. This design obtains low leakage power, low dynamic power dissipation and high speed with smaller layout area.

Here additional inverters are not required to obtain inverted input of input vector (A, B). During precharge phase, dynamic node Vn is charged to supply voltage through transistor MPc1 and XOR_out set to low voltage. During evaluation phase, if input vectors (0, 1) or (1, 0) is applied, dynamic node is discharged to low voltage and XOR_out is charged to high voltage. While input vector (0, 0) or (1, 1) is applied, dynamic node preserved its high state and output node is discharged to low voltage. This design obtains low leakage power, low dynamic power dissipation and high speed with smaller layout area as compared to DXN and DXP.



"Fig."3 Dynamic XOR/XNOR using Hybrid pull down network with fixed threshold (DXH)

III. PROPOSED METHODOLOGY AND CIRCUIT

A. Proposed Methodology

This work has performed in several stages to obtain the desired delay, power dissipation and layout area. Complete circuit design, layout design and its characterization performed in HSPICE. Complete work performed in the following order as shown in design flow.

Complete designing takes place in two phases:

1. Design Phase
2. Simulation Phase

This section discussed in detail in upcoming chapters.

Objective of work: To improve the performance of SRAM cell following parameters need to be considered:

1. Smaller read delay
2. Smaller leakage power
3. Smaller dynamic power
4. Smaller layout area

Design Logic Explanation: fixed body bias offers fixed threshold in precharge and evaluation phase. This may offers higher power dissipation or time delay depends on threshold of MOS. Practically, we expect that in evaluation phase when dynamic node discharge to ground PMOS offers smaller threshold otherwise PMOS offers higher threshold in evaluation network. Therefore, this work is going to design a XOR gate that offer higher speed and lower power dissipation. This is possible by varying the body to source voltage of PMOS by using input.

Evaluation Delay: This is the time difference between changes in the states of the clock to the change in XOR gate output.

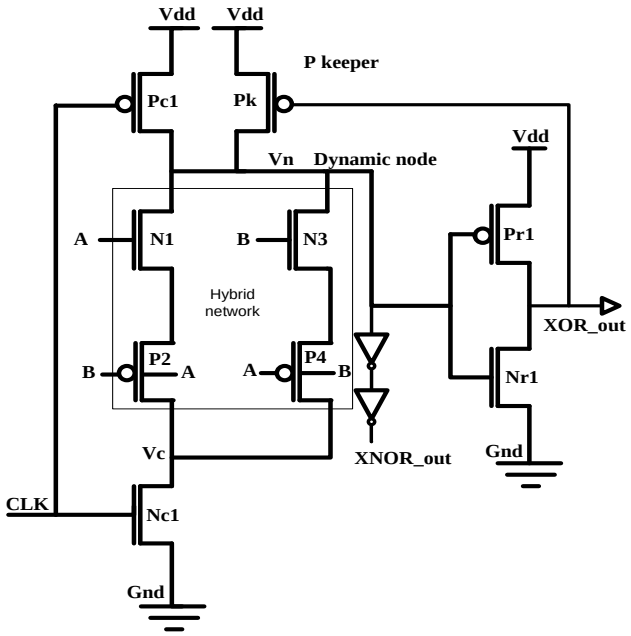
Leakage Power: whenever device operate in idle state, the power consume by gate is equivalent to leakage power. This is depends on sub threshold leakage, gate leakage and body leakage.

Dynamic Power dissipation: Total power dissipation is a sum of static and dynamic power. Whenever, XOR gate in running state dynamic power dominate while cell in idle state leakage power dominate. Here, Average power dissipation equivalent to dynamic power.

Layout Area: Area occupied on silicon wafer according to lambda rule, is called layout area.

B. Proposed Circuit

This technique adopt NMOS and PMOS transistor to form hybrid network as shown in "Fig."4. In this design series combination of transistor pair N1, P2 and transistor pair N3, P4 is connected in parallel [Ref]. The gate and body terminal of P2 connected with input A and B respectively while gate and body terminal of P4 connected with input B and A respectively. This cross body bias speed up dynamic gate and reduce dynamic power consumption



"Fig."4 Proposed input body bias dynamic body bias XOR/XNOR

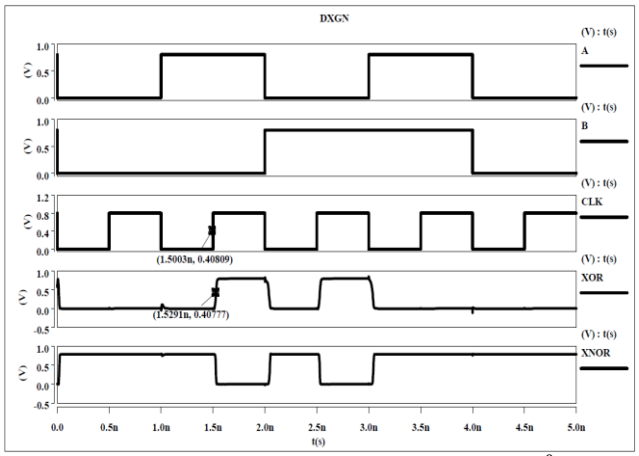
IV. .IMPLEMENTATION RESULTS AND COMPARISONS

To examine the performance of dynamic XOR/XNOR gate, it is necessary to study the transient analysis and process variation. We have performed complete study using Hspice and Microwind at 45nm technology node.

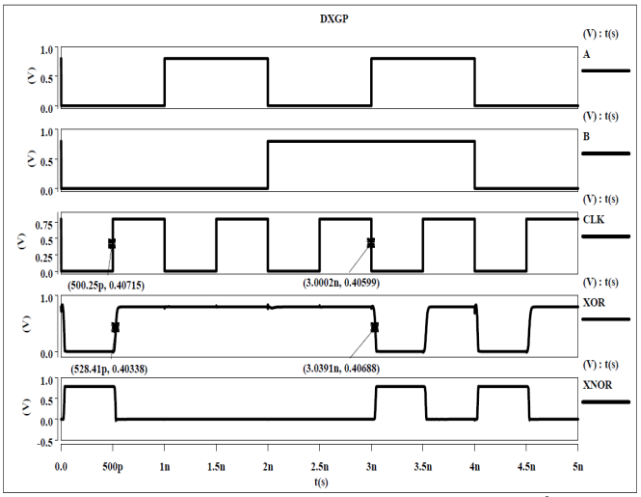
DXGN, DXGP, and DXGH are simulated respectively based on 45 nm BSIM4 models [10] by the HSPICE tool. The temperature variation also examine at 27^0C and 110^0C, where each dynamic gate drives a capacitive load of 8 fF and is turned to operate at 1 GHz clock frequency for fair comparison of the leakage power, the dynamic power, the layout area and the noise margins of different gates. The layout area of dynamic gates is calculated using Microwind tool at 45nm [18, 19, and 20]. The threshold voltage of NMOS and PMOS transistors and supply voltage are fixed at 0.22, -0.22, and 0.8 V, respectively.

A. ACTIVE POWER DISSIPATION AND DELAY MEASURMENT

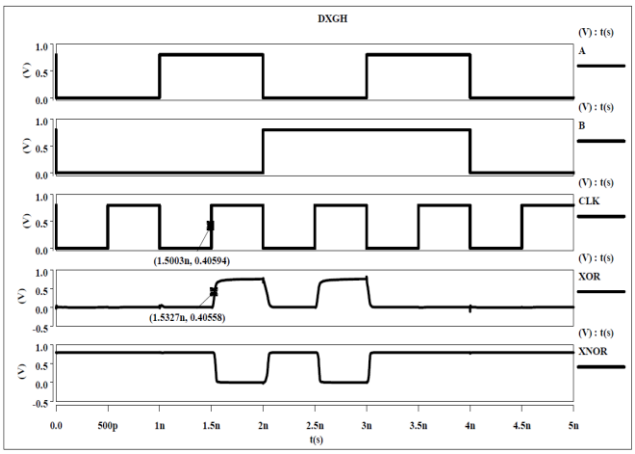
The active power is evaluated using average power consumption takes place during 4nSec interval. The delay is defined as the time required changing in output vector XOR_OUT with respect to change in input vector CLK. The delay estimation of DXGN, DXGP, DXGH and Proposed are shown in "Fig."5, "Fig."6, "Fig."7 and "Fig."8 respectively



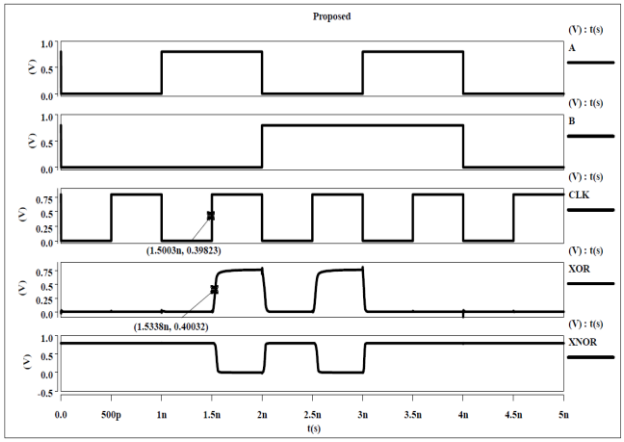
"Fig."5 Delay Measurement of DXGN at 25^0C



"Fig."6 Delay Measurement of DXGP at 25^0C

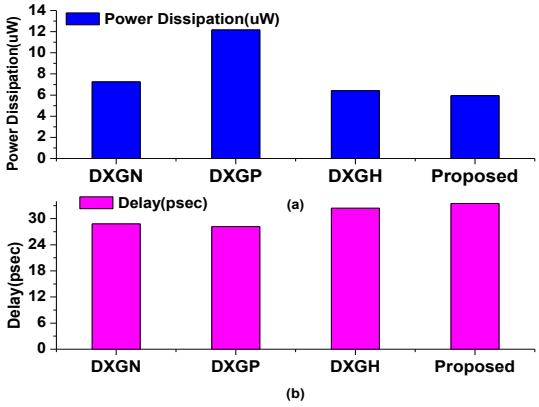


"Fig."7 Delay Measurement of DXGH at 25^0C



"Fig."8 Delay Measurement of Proposed at 25^0C

Design Parameters	DXGN	DXGP	DXGH	Proposed
Delay(psec)	28.8	28.16	32.4	33.5
Power Dissipation(uW)	7.2538	12.171	6.4123	5.9452



"Fig."9 Active Power Dissipation Comparison among various XOR/XNOR at 25^0C

Table I Value of Active Power Dissipation and Delay Measurement in Various Dynamic adders at 25^0C

V. CONCLUSION

Standard dynamic CMOS XOR/XNOR gates are extensively employed in modern high performance microprocessors because of high speed and controllable evaluation by clock node, but they suffer from high power consumption and input signal skew. In this work, a novel dynamic XOR/XNOR gate based on hybrid network is proposed to decrease, respectively, the leakage power, the dynamic power, and the layout area up to as compared o standard N type dynamic CMOS XOR/XNOR gate under similar delay time. What's more, the novel dynamic CMOS XOR/ XNOR gate shows superior robustness under process and temperature variations. DXM gates are fundamental units in various circuits especially circuits used for performing arithmetic operations in high speed microprocessor. The proposed method obtains 18% reduction in dynamic power compare to DXN and 48% reduction in layout area at a cost of slight variation in leakage power. Apart of that process variation using Monte Carlo shows appreciable improvement in dynamic power.

ACKNOWLEDGMENT

The result of this proposed circuit gives us so much pleasure. I would like to express my sincere gratitude to my project guide **"Mr. Khemraj Deshmukh"** for giving me the opportunity and guideline to work on that. It would never be possible for us to take this project to this level without his innovative ideas and his relentless support and encouragement.

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