Implementation of LDPC Code for 24-bit Decoder Based on VLSI Using Verilog Code

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***Abstract*—Low density parity check (LDPC) codes are used in several applications such as the digital satellite broadcasting system (DVB-S2), Wireless Local Area Network (IEEE 802.11n) and Metropolitan Area Network (802.16e). Error correcting codes are widely used in low density parity-check (LDPC)codes. In this paper present a design approach for low density parity-check (LDPC) coding system hardware implementation by jointly conceiving irregular LDPC code construction . Low -density parity check decoder using Verilog technique is implemented. belief propagation (BP) algorithm are used design for partially parallel decoder. IV Summit of the technology used with Mentor Graphics Leonardo Spectrum synthesis and ModelSim is used to simulate.**

Index Terms*— *Low density parity check (LDPC) code; Error correcting code(ECC); Modelsim; Xilinx.

I. INTRODUCTION

Using the low -density parity check noisycommunication channel (LDPC) codes to minimize the possibility of loss of information is used , which is an error correcting code . LDPC codes are capacity-approaching codes, which means that practical constructions exist that allow the noise threshold to be set very close the theoretical maximum (the Shannon limit) for a symmetric memory less channel. | Which has lost much of the information can be reduced , noise limits define an upper limit , is to channel noise.

Low density parity check (LDPC) codes are also known as Gallager codes because these codes proposed by R.G. Gallager in 1962[1]. since the hardware at that time could not attain the requirements needed by the encoding process. With increased capacity of computers and the development of relevant theories such as belief propagation algorithm, LDPC codes were rediscovered by Mackay and Neal in 1996[2].

LDPC codes are linear block codes that can be denoted as (n, k) or (n, wc, wr), where n is the length of the codeword, k is the length of the message bits, wc is the column weight (i.e. the number of nonzero elements in a column of the parity-check matrix), and wr is the row weight (i.e. the number of nonzero elements in a row of the parity-check matrix).

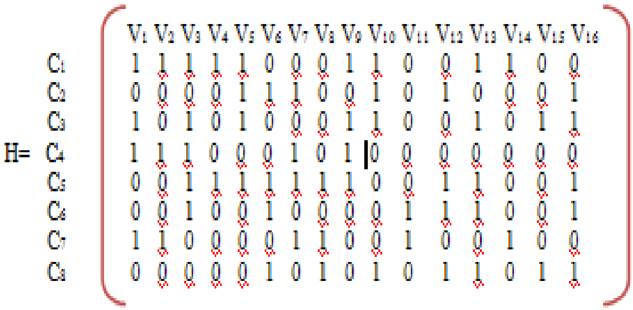
II. CHARACTERISTICS FOR LDPC CODES

A. Parity-check

LDPC codes are represented by a parity-check matrix H, where H is a binary matrix that, must satisfy cHT = 0, where c is a codeword.

B. Low-density

H is a sparse matrix (i.e. the number of ‘1’s is much lower than the number of '0's). It is the sparseness of H that guarantees the low computing complexity.



$$H= \begin{array}{c} \\ C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \\ C_7 \\ C_8 \end{array} \left(\begin{array}{cccccccccccccccc} V_1 & V_2 & V_3 & V_4 & V_5 & V_6 & V_7 & V_8 & V_9 & V_{10} & V_{11} & V_{12} & V_{13} & V_{14} & V_{15} & V_{16} \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \end{array} \right)$$

Figure 1. H-matrix

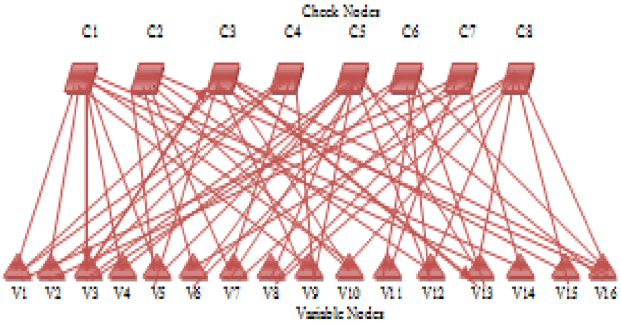


Figure 2. Tanner graph corresponding to the parity check matrix

Here we consider H be the parity check matrix of irregular (16, 8) LDPC code and its tanner graph is also shown in fig. 1. For this LDPC code the path (c1 → v3 → c3 → v13 → p1) with the black bold lines. In recent year studies the decoding is done by various algorithms and different types of decoders are designed such as partially

parallel decoder, memory efficient decoders. Good approximate belief propagation decoder decoding in the decoding scheme is to give birth ..In this paper the belief propagation decoding algorithm is define then modified sum product algorithm is defined and in next part of this paper decoder is implemented in Xilinx using Verilog.

The rest of the paper is arranged as follows: belief propagation algorithm is defined in section (a); Modified sum product algorithm is described in section (b); Experimental results are presented in section 4; Finally, the conclusion is given in section 5.

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III. LDPC DECODER USING BELIEF PROPAGATION

Sum product algorithm is also known as Bayesian networks and Markov random fields , such as graphical models, belief propagation algorithm is passing a message to display on the estimate . Calculating the marginal distribution for each node is indirect , conditional to any observed nodes .Artificial intelligence and information theory is the belief propagation and low density parity check code is used , in many applications including turbo codes have demonstrated empirical success.

a).Belief Propagation Algorithm:-

Update Check Messages

For each check node j, and for every bit node associated with it j compute: we assume BPSK modulation, which maps a codeword c= (c1,c2,c3,………, cN) into a transmitted sequence s= (s1,s2,s3,…..sN). Then S is transmitted over a channel corrupted by additive white Gaussian noise (AWGN) [5].

The following step is formed consisting of the sum product algorithm . First LLRs used for priori message probabilities, then parity check matrix H and maximum number of allowed iterations I max.

Steps for sum product algorithm

Initialize

Set Qij = λj, this initialize the check nodes with priori message probabilities.

$$Rij = 2\, tanh - 1 \prod_{\alpha\varepsilon V(j,\alpha\neq i)} \tanh\left(\frac{Q\alpha j}{2}\right) \qquad (1)$$

Test for valid codeword

Codeword for a temporary decision to

$$Li = \lambda\, j + \sum_{j\varepsilon c\ (j)} Q\alpha j \qquad (2)$$

If number of iterations is Imax or valid codeword has been found then finish

Update Bit Messages

For each bit node j, and for every check node associated with it j compute:

$$Qij == \lambda\, j + \sum_{j\varepsilon c\ (j)} R\alpha j[k-1] \qquad (3)$$

(b). Modified Sum Product Algorithm:-

SPA algorithm in the context of a general algorithm is estimated that the amount modified product is applied using algorithm decoders. SPA modified decoder is easy to implement [12].

Variable node decoder output is then transmitted through AWGN channel encoder output . Let M (n) denote the set of check nodes connected to the symbol node n and N (m) the set of symbol nodes participating in the m-th parity-check equation.

Step1

Initialization

The value LC = 2 / σ2, assuming AWGN channel with noise variance is σ2. Initialization , in every situation parity check matrix H (m , n) is used .

$$\lambda n \rightarrow m\ (Un) = L\ (Un) \qquad (4)$$

$$\lambda m \rightarrow n\ (Un) = 0 \qquad (5)$$

Step 2

Iterative Process

Update the check-node LLR, for each m and for each n∈ N (m), as

$$\Lambda m \rightarrow n\ (Un) \quad = 2\tanh \ -1 \left\{\prod_{\frac{n' \varepsilon N(m)}{n}} \tanh\left[\frac{\lambda n' \rightarrow m(un')}{2}\right\}\right.$$

Note that both the tanh and tanh−1. functions are increasing and have odd symmetry. Thus , a simplified version can be used in the magnitude of incoming messages and signatures .as

as

$$\Lambda m \rightarrow n\,(Un) = 2\left\{\prod_{n' \varepsilon N(m)/n} \sinh\left[\lambda n' \rightarrow m(un')\right]\right\} \tanh - 1 \left\{\prod_{n' \varepsilon N(m)/n} \tanh\left[\frac{\lambda n' \rightarrow m(un')}{2}\right]\right\} \qquad (7)$$

Step 3

Variable node update

Update the variable node LLR, for each n and for each m ∈ M (n), as

$$\lambda n \rightarrow m(Un) = L(Un) + \sum_{\frac{m' \varepsilon M(n)}{m}} \Lambda m' \rightarrow n(un) \qquad (8)$$

Step 4

Decision Process

Decide if *λ*n (un) ≥ 0, then un=0 and if *λ*n (u) ≤ 0 then un=1. Then compute the syndrome uHT=0, then the codeword (*u*) is the final codeword, otherwise the iteration takes place till valid code word is obtained.

IV. EXPERIMENTS AND RESULTS

(a).Simulation result

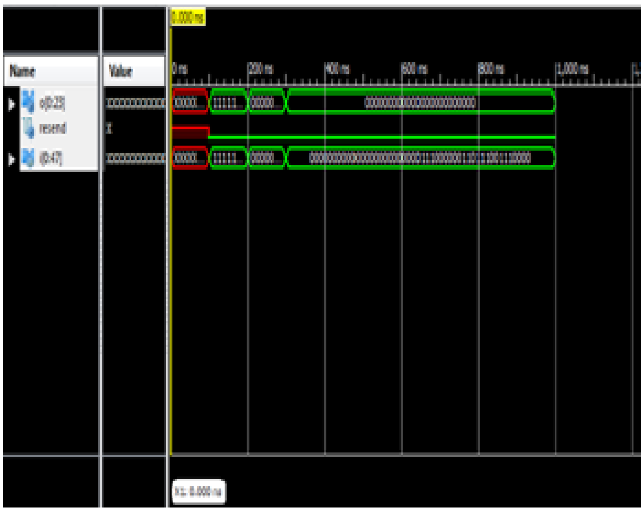


Figure 3. Simulation Result

(b).Synthesis

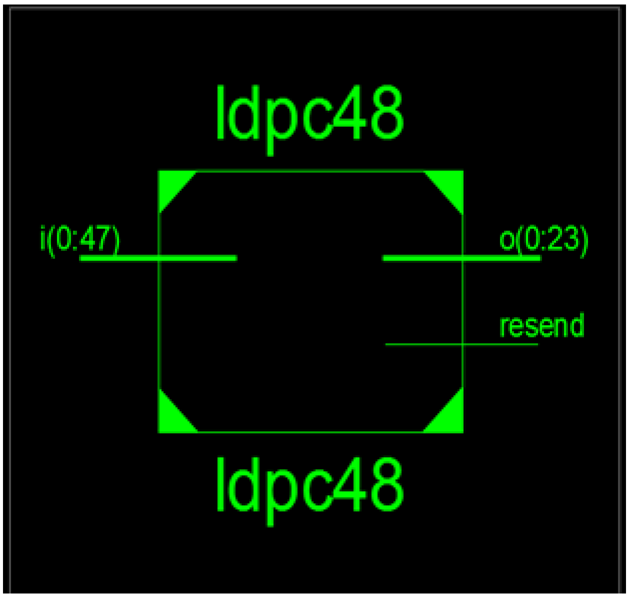


Figure 4. Top level schematic of decoder

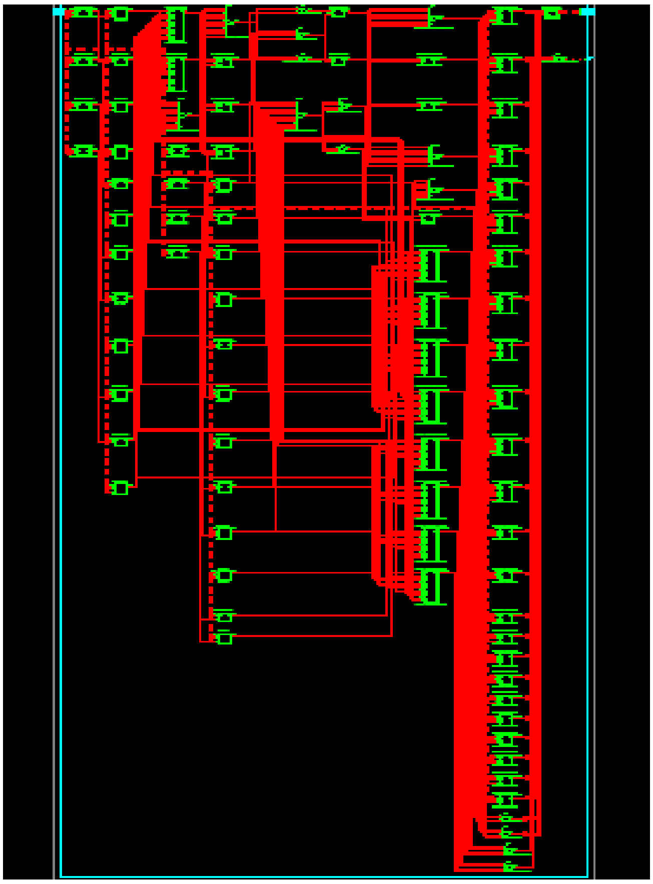
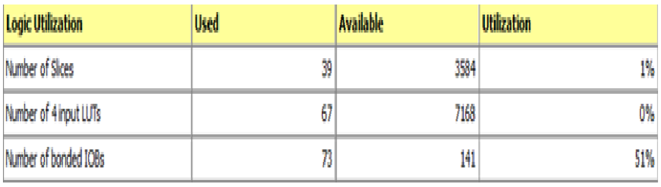


Figure 5. RTL schematic of decoder



Logic Utilization	Used	Available	Utilization
Number of Slices	39	3584	1%
Number of 4 input LUTs	67	7168	0%
Number of bonded IOBs	73	141	51%

Figure 6. Device Utilization of Decoder

V. CONCLUSIONS

Bipartite graph is implemented with the use of the decoder for the LDPC code. In Xilinx using Verilog code is implemented and is using Modelsim for simulation. Decoder for decoding algorithm modified products have been found to be effective . We observed that high throughput LDPC decoding architectures should exploit the benefit of parallel decoding algorithms.

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