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A Modified Carry Select Adder Using Common Boolean Logic

Sanooja S, Aswathi B

***Abstract*— carry select adder (CSLA) is known to be the fastest adder among the conventional adder structure. The logic operations involved in conventional carry select adder an binary to excess-1 converter (BEC)-based CSLA are analysed to study the data dependence and to identify redundant logic operations. The common Boolean logic (CBL) based CSLA can remove the redundant logic operations in the conventional carry select adder. The proposed CSLA design involves significantly less area and delay than BEC-based CSLA. It is based on the proposed logic, the efficient logic design for CSLA is derived. The CSLA involves significantly less area-delay-produce(ADP) and offers the best area-delay-power efficiency than the existing CSLAs .Due to the small carry output delay, CBL-based CSLA is good candidate of SQRT-CSLA design.**

***Index Terms*— Carry select adder, Binary to excess-1 converter, Common boolean logic, Area-delay-product.**

I. INTRODUCTION

An adder is the main component of an arithmetic unit and a complex digital signal processing system involves several adders. Area efficient, low power and high-performance VLSI systems are increasingly used in portable and mobile devices, wireless receivers, and biomedical instrumentation. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. A ripple carry adder (RCA) uses a simple design, but the main concern is that carry propagation delay (CPD).

Carry select adder (CSLA) is the fastest adder among the conventional adder structure. A conventional carry select adder is an RCA–RCA configuration that generates a pair of sum words. The output carry bits corresponding the anticipated input-carry (cin 0 and 1) and selects one out of each pair for final-sum and final-output-carry. A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA. After the few attempts,

made to avoid dual use of RCA in CSLA design and used one RCA and one add-one circuit instead of two RCAs.

The BEC-based CSLA involves less logic resources than the conventional CSLA, but it has marginally higher delay. The logic operations involved in conventional carry select

adder and binary to excess-1 converter (BEC)-based CSLA are analyzed to study data dependence and to identify redundant logic operations. To removing redundant logic operations by using CSLA based on common Boolean logic (CBL). It is also involves significantly less logic resource than the conventional CSLA , which is almost equal to that of the RCA.

In this paper, a modified carry select adder by sharing the common Boolean logic term is proposed. After Boolean simplification, it can remove the redundant logic operations in the conventional carry select adder. It generates a redundant sum and Carry-out signal by using NOT and OR gate and select value with the help of multiplexer. The multiplexer is used to select the correct output according to its previous carry-out signal. The proposed CSLA provides less area-delay –power.

Sanooja S, Applied Electronics and Instrumentation, Younus College Of EngineeringAndTechnology,kollam,India.
Aswathi B, Department Of ECE,Asst. Professor, Younus College Of EngineeringAndTechnology,kollam,India.

II. RELATED WORKS

Ripple Carry Adder consists of cascaded "N" single bit full adders and the output carry of previous adder becomes the input carry of next full adder. The carry of this adder traverses longest path. The value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. Now CSLA provides a way to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage.

A. Conventional CSLA

The conventional CSLA makes use of Dual RCA's to generate the partial sum and carry by considering input carry Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers. Basically CSLA has two units: 1) the sum and carry generator unit (SCG) and 2) the sum and carry selection unit .The SCG unit consumes most of the logic resources of CSLA and it contributes to the critical path. Different logic designs have been suggested for efficient implementation of the SCG unit. The carry select adder achieves higher speed of operation at the cost of increased number of devices used in the circuit. This in turn increases the area and power consumed by the circuits of this type structure. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. The RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. carry i.e. 0 and 1. Now conventional CSLA provides a way to get around this linear dependency is to anticipate all possible values of input the original value.

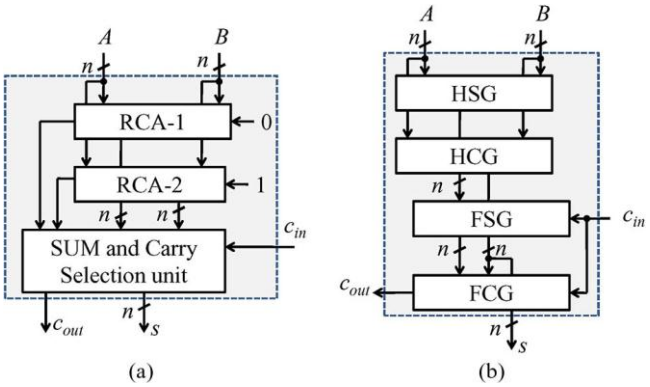

Fig. 1.(a) Conventional CSLA; n is the input operand bit-width. (b) The logic operations of the RCA..

Fig.1(a) shows, the sum and carry unit of conventional CSLA is composed of two n-bit RCAs, where n is the adder bit-width and the logic operation of the n-bit RCA is performed in four stages: 1) half-sum generation (HSG); 2) half-carry generation (HCG); 3) full-sum generation (FSG); and 4) full carry generation (FCG). Consider two n-bit operands are added in the conventional CSLA, then RCA-1 and RCA-2 generate n-bit sum (s0 and s1) and output-carry ($c0_{out}$ and $c1_{out}$) corresponding to input-carry (cin = 0 and cin = 1), respectively. Logic expressions of RCA-1 and n-bit CSLA are given as

$$S_0^0(i) = A(i) \oplus B(i) \quad C_0^0(i) = A(i) \cdot B(i) \tag{1}$$

$$S_1^0(i) = S_0^0(i).C_1^0(i-1) \tag{2}$$

$$C_1^0(i) = C_0^0(i) + S_0^0(i).C_0^1(i-1) \quad C_{out}^0 = C_1^0(n-1) \tag{3}$$

$$S_0^1 = A(i) \oplus B(i) \quad C_0^1(i) = A(i) \cdot B(i) \tag{a}$$

$$S_1^1(i) = S_0^1(i)\, C_1^1(i-1) \tag{b}$$

$$C_1^1(i) = C_0^1(i) + S_0^1(i)\, .\, C_1^1(i)\ (i-1) \quad C_{out}^1 = C_1^1(n-1) \tag{c}$$

where $C_1^0(-1) = 0$, $C_1^1(-1) = 1$, and $0 \leq i \leq n-1$.

Expressions (1)–(3) are redundant logic operations. That can be removed by using an add-one circuit instead of RCA-2 in the CSLA, in which a BEC circuit is used in for the same purpose and the BEC-based CSLA offers the best area–delay–power efficiency among the existing CSLA.

B . BEC-based CSLA

The modified Carry select adder has a single ripple carry adder with Binary to Excess-1 converter, which replace the ripple carry adder with Cin=l, in order to reduce the area and power consumption of the conventional CSLA. To replace the n-bit RCA, an n+ 1 -bit BEC is required.

The importance of the BEC logic systems from the large silicon area reduction when the CSLA with large number of bits are designed.The Binary to Excess-1 Converter is a digital circuit that excess the value of the input to 1 means the value of input gets increased by 1 with the help of BEC-1.It is a digital circuit that uses 1 NOT gate, 2 AND gate and 3 XOR gates to perform the operation. Since Regular Carry Select Adder uses multiple RCAs to perform the addition operation of input bits.The main advantage of the BEC-based CSLA is that to reduce the number of gates compared to conventional type CSLA. Numbers of gate will be reduces the area of the structure is also reduce.

Let us see the logic diagram and logic Equations of BEC converter.

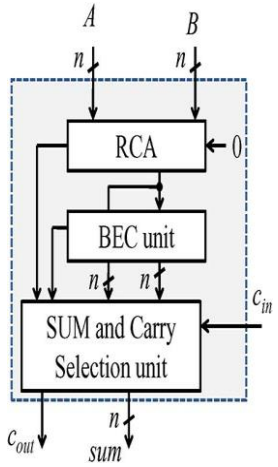

Fig.2 Structure of the BEC-based CSLA; n is the operand bit width.

$$S_1^1(0) = S_1^0(0) \quad C_1^1(0) = S_1^0(0) \tag{d}$$

$$S_1^1(i) = S_1^0(i)\ C_1^1(i-1) \tag{e}$$

$$C_1^1(i) = S_1^0(i).C_1^1(i-1) \tag{f}$$

$$C_{out}^1 = C_1^0(n-1) \oplus C_1^1(n-1) \tag{g}$$

for $1 \leq i \leq n-1$.

From the expressions (1)-(3) and (d)-(g),the BEC-based CSLA,C_1^1 depends on S_1^0. The BEC method therefore increases data dependence in the CSLA.

C .Carry Select Adder Design

The main drawback of the Conventional and BEC-based CSLA is that logic expressions involves large number of redundant logic operations. So it can be eliminating by use Carry Select(CS) adder design. This is the modified scheme. The main advantages of the design is that,

1) Calculation of S_1^0 is avoided in the SCG unit
2) the n-bit select unit is required instead of the (n + 1) bit
3) small output-carry delay.

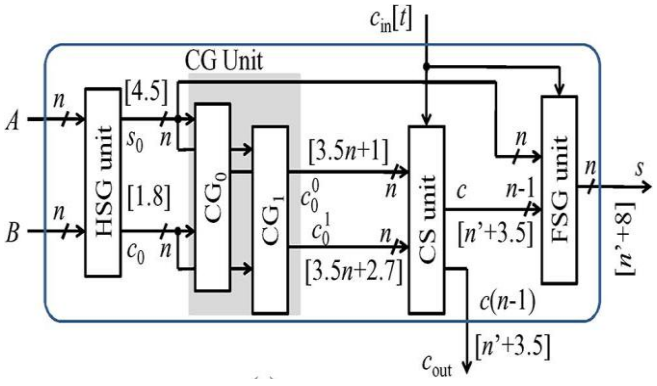

Fig.3.Carry selection adder Design

Fig .3.shows the modified CSLA (Carry Select Adder Design) consists of one HSG unit, one SG unit, one CG unit, and one CS unit and the CG unit is composed of two CGs (CG0 and CG1) corresponding to input-carry '0' and '1'. The HSG receives two n-bit operands (A and B) and generate half-sum word S_0 and half-carry word C_0 of width 'n' bits each. Both CG0 and CG1 receive *s*0 and *c*0 from the HSG unit and generate two n-bit full-carry words C_1^0 and C_1^1 corresponding to input-carry '0' and '1', respectively. The optimized designs of CG0 and CG1 are shown in Fig and respectively.

The Carry Selection unit selects one final carry word from the two carry words available at its input line using the control signal Cin. It selects *c*01 when *c*in = 0; otherwise, it selects *c*11. The CS unit can be implemented using an *n*-bit 2-to-l MUX. However, we find from the truth table of the CS unit that carry words C_1^0 and C_1^1 follow a specific bit pattern. If C_1^0 (i) = '1', then C_1^1 (i) = 1, irrespective of S_0 (i) and C_0 (i), for $0 \leq i \leq n-1$. This feature is used for logic optimization of the CS unit. The optimized design of the CS unit is shown in Fig. 3(e), which is composed of 'n' AND–OR gates. The final carry word *c* is obtained from the CS unit. The MSB of *c* is sent to output as *c*out, and (*n* − 1) LSBs are XORed with (*n* − 1) MSBs of half-sum S_0 in the FSG to obtain (n − 1) MSBs of final-sum (s). The S_0 in the FSG to obtain (n − 1) MSBs of final-sum (s). The LSB of output sum is XORed with input carry to obtain the LSB of sum.

III. PROPOSED ADDER DESIGN

In proposed work, an area-delay-power efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder. Through analyzing the truth table of a single-bit full adder, To find out that the output of summation signal as carry-in signal is logic "0" is the inverse signal of itself as carry-in signal is logic "1 ".

To share the common Boolean logic term, it only needs to implement one OR gate with one INV gate to generate the Carry signal and summation signal pair. Once the carry-in signal is ready, then select the correct carry-out output according to the logic state of carry-in signal. BEC-based CSLA has large ADP than CBL based CSLA. The proposed CSLA provides less ADP due to less area complexity.

Cin	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig.3. Truth table of single bit full adder.

As compared with the Modified Carry Select adder, the proposed CSLA is little bit faster, but the speed is nearly equal to the Regular CSLA. The delay time in our proposed adder design is also proportional to the bit number N; however, the delay time of multiplexer is shorter than that of full adder. The Proposed common Boolean based CSLA is area efficient, low power and delay efficient than modified BEC based carry select adder.

This method replaces the Binary to Excess-1 converter add one circuit by common Boolean logic. As compared with modified CSLA, the proposed structure is little bit faster. The delay time in our proposed adder design is also proportional to the bit number N; however, the delay time of multiplexer is shorter than that of full adder.

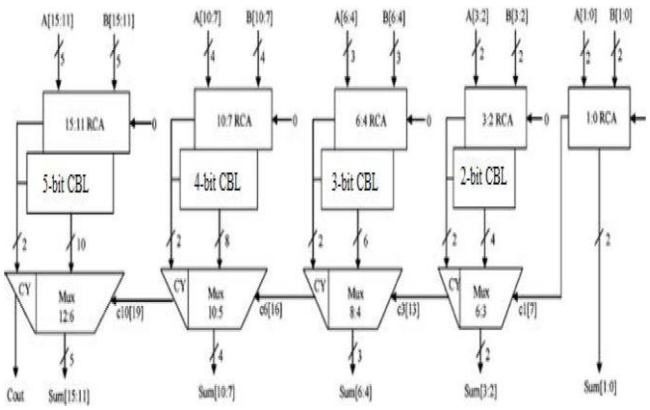

Fig.4. The Proposed SQRT CSLA based CBL

The Proposed 16-bit SQRT CSLA using CBL. This method replaces the BEC add one circuit by Common Boolean Logic. The output waveform of full adder for carry in signal is '1' is generate summation and carry signal by just using an INV and OR gate.

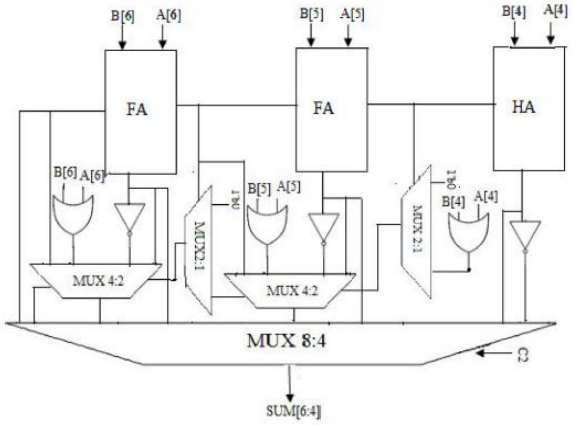

Fig.5.Internal structure of the proposed area-delay-power efficient carry select adder is constructed by sharing the common Boolean logic term

The logic for the required carry is chosen using 2:1 mux circuits. This results in reduced gate numbers than existing carry select adders. Hence it has the area minimized and operating computational speed is more. The CBL term can remove the redundant logic operations in the conventional carry select adder. It provides less area-delay-product (ADP) than existing CSLA. Due to output carry with multipath carry propagation unit, the modified CBL-based CSLA design is more favorable than existing CSLA design. Table.1 shows synthesis results of conventional (RCA),modified (BEC) and proposed (CBL).

TABLE.I
Synthesis Result

Word Size	Adder	Area (no. Of gate count)	Delay (ns)	Power (mW)
8bit CSLA	Modified(CS) Proposed(CBL)	186 130	16.212 13.124	25 22
16 bit CSLA	Modified(CS) Proposed(CBL)	366 294	24.824 18.268	35 32
32 bit CSLA	Modified(CS) Proposed(CBL)	810 734	30.028 27.826	46 42

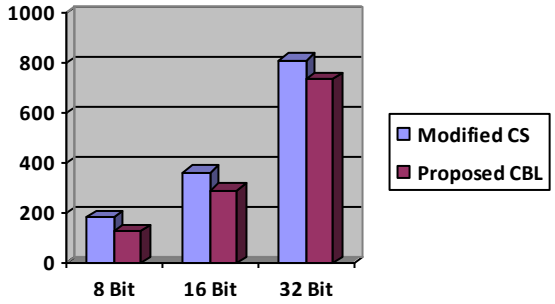

FIG.6. COMPARISON OF ADDERS FOR AREA

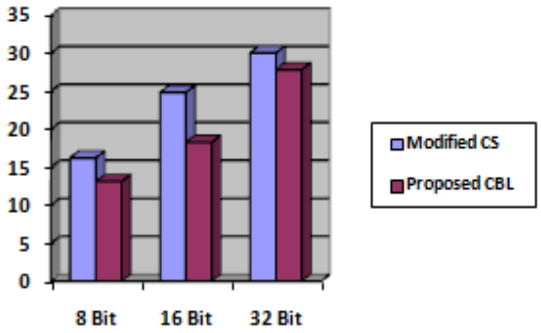

FIG.6. COMPARISON OF ADDERS FOR DELAY

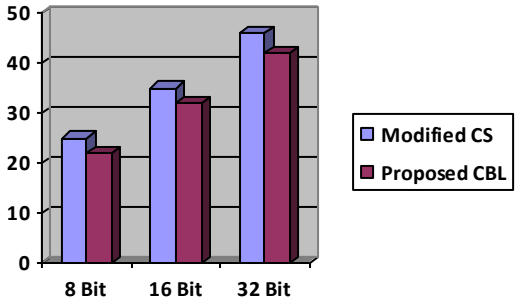

FIG.6. COMPARISON OF ADDERS FOR POWER

IV. CONCLUSION

The logic operations involved in the conventional and BEC-based CSLAs are analysed and to identified the redundant logic operations. Eliminated the redundant logic operations by using CBL based CSLA. This type of CSLA design involves significantly less area–delay-product than BEC-based CSLA and due to the small carry output delay, the CBL-based CSLA is a good candidate for the SQRT. The conventional CSLA has the disadvantage of more power consumptions and occupying more chip area. The BEC-based CSLA reduces the area and power when compared to conventional CSLA with increase in delay. This proposed scheme, which reduces the delay, area and power than carry selection adder design.

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sanooja s, M.Tech Student, Applied Electronics and Instrumentation, Younus College Of Engineering And Technology, kollam,India.

Aswathi B Asst. Professor, Department Of ECE, Younus College Of Engineering And Technology, kollam,India.