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Efficient Designs of Low Power 32nm XOR-XNOR Gate using CMOS Inverters

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***Abstract*— Different designs of XOR-XNOR gate have been designed using different components like Transmission Gates, NMOS switches, Pass Transistors & GDI (Gate Diffusion Input) cell that can be operated at higher frequencies. All designs have been designed using 32nm UMC CMOS technology and compared the factors for the supply voltage of 0.9V. These designs are simulated in HSPICE tool for the successful function. Best optimized design of XOR/XNOR gate is found out. It is being widely used in a high speed microprocessors like adders, comparators etc for performing different arithmetic operations. Improved features of XOR/XNOR circuit increases the performance of full adder and other circuits.**

***Index Terms*— XOR, XNOR, CMOS, VLSI, SIMULINK.**

I. INTRODUCTION

The fundamental functions for many circuits like adders, comparators, subtractors, parity checkers, multipliers, full adders, etc. are exclusive-OR (XOR) and exclusive-NOR (XNOR). There are two types of MOS i.e. the p-channel Metal Oxide Semiconductor (PMOS) and the n-channel Metal Oxide Semiconductor (NMOS). It is known that NMOS transistor is able to transmit the "LOW" signal (or "0") completely and it shows poor performance when the "HIGH" signal (or "1") has to be transmitted. If a switch device has to be implemented using a NMOS transistor, a control signal should be added to the terminal of gate and sets one of its end at "HIGH", whereas other end will fall to threshold voltage of NMOS, V_{Nth}. The PMOS transistor can easily transmit a "HIGH" signal completely but it can barely handle a "LOW" signal. In a switch device, if a signal goes "LOW" at the source of PMOS transistor, the other end will not sink to "LOW" signal, as it could not fall below threshold voltage of PMOS, V_{Pth}. MOSFET scaling has many advantages like higher speeds, lower power dissipation and higher packaging density. The concept behind MOSFETs scaling is the various parameters of the MOSFETs structure for better functioning of the device.

Dissipation in power can be determined by using some methods like node capacitances where node capacitance is made of gate, diffusion and wire capacitances, switching activity and size of control circuit. There are three main components of power dissipation in (CMOS) circuits: Switching Power: Power that is consumed by circuit node capacitance when transistor switching is done;

Short Circuit Power: Power that is consumed due to the current flow from power supply to ground when the transistor switching process in ON;

Static Power: Power dissipation because of leakage in circuits and static currents.

The above mentioned first two components are said to be **dynamic power**. Dynamic power comprises the major part of the power dissipation in VLSI circuits. Dynamic power is the power dissipated at the time of charging and discharging the load capacitance in given circuit. Average power dissipated in a general digital CMOS circuit is given by:

$$P_{total} = P_{dynamic}\,(P_d) + P_{static} + P_{short\text{-}circuit}$$
$$= V_{DD} \cdot f_{clk} \cdot \sum (V_{iswing} \cdot C_{iload} \cdot \alpha_i) + V_{DD} \cdot \sum I_{isc} + V_{DD} \cdot I_l$$

Here,

f_{clk} = system clock frequency,

V_{iswing} = voltage swing at node i,

C_{iload} = load capacitance at node I,

αi = activity factor at node i.

I_{isc} = short circuit current

and I_l = leakage current.

Today the main concern issues for designing any CMOS circuit are power, delay and silicon area of the chip. Transmission gate is also used in designing of XOR/XNOR circuit because transmission gate has high switching speed, requires less power and gives less delay. Delay can be easily predicted by Spice simulations. These simulations help in minimizing chip area, power consumption, time delay and maximizing reliability.

Table I: Functions of XOR/XNOR gate

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

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II. SIMULATED DESIGNS

A. Designs of XOR/XNOR Gate

Different designs of XOR/ XNOR gate have been implemented using 32nm UMC CMOS technology. Figure 1 shows design of XOR/XNOR gate which uses eight MOSFTEs.

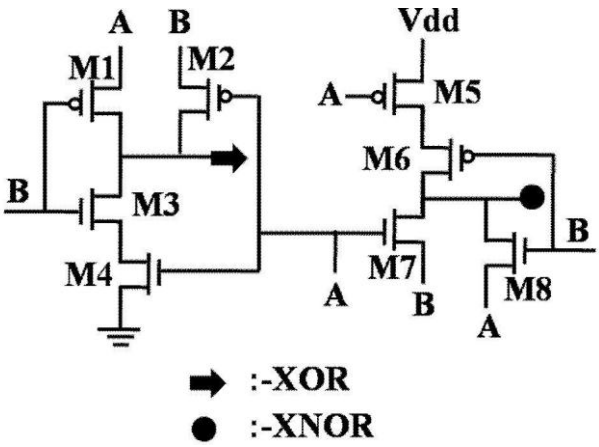

Figure 1: XOR/XNOR gate design-I

In this design When AB=00, M1, M2, M5, M6 gets ON. At this stage M1 & M2 gives XOR output '0' and M5 & M6 gives XNOR output Vdd as '1'. When AB=01, M2, M3, M5, M8 gets ON. At this stage M2 gives XOR output B as '1' and M8 gives XNOR output A as '0'. When AB=10, M1, M4, M6, M7 gets on, at this stage M1 gives XOR output A as '1' and M7 gives XNOR output B as '0'. When AB=11, M3, M4, M7, M8 gets on, at this stage M3 & M4 gives output '0' and M7 & M8 gives output '1'.

Similarly other designs are formed using different types of components like transmission gate, GDI cell etc.

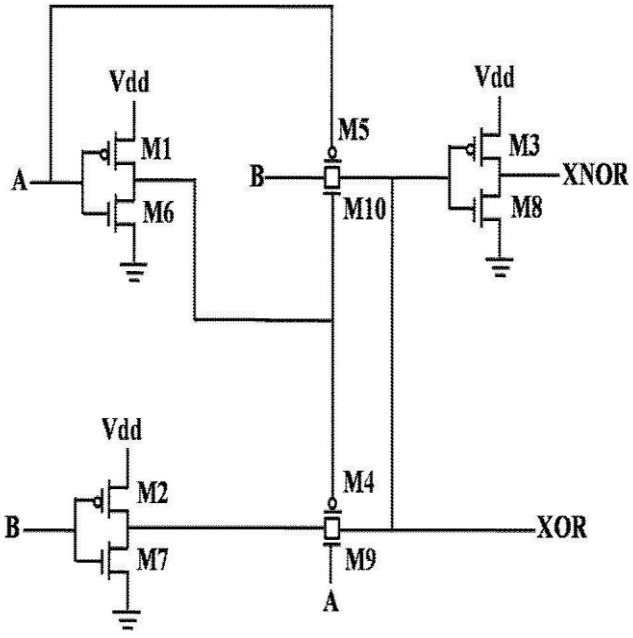

Figure 2: XOR/XNOR gate design-II

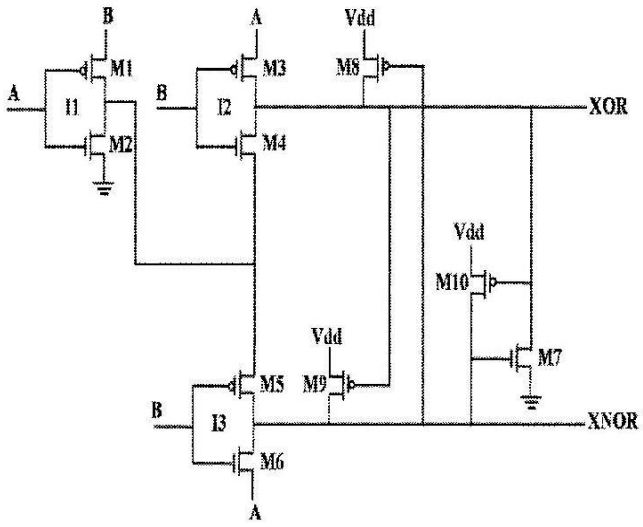

Figure 3: XOR/XNOR gate design-III

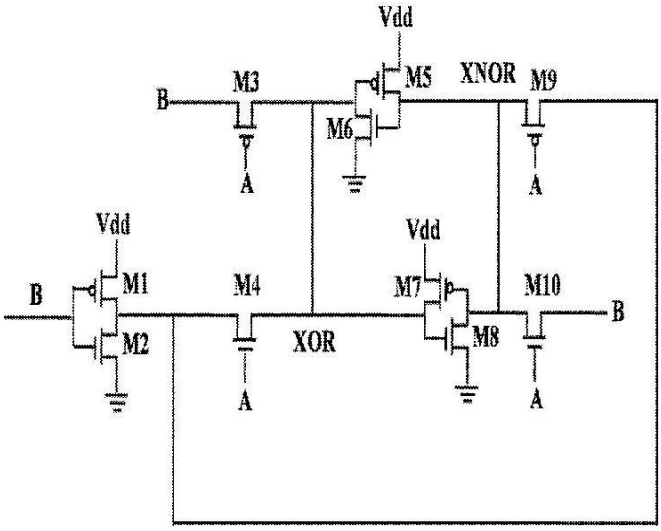

Figure 4: XOR/XNOR gate design-IV

III. SIMULATION RESULTS

Waveforms for all these XOR/XNOR designs (I, II, III, IV) are shown in Figures 5, 6, 7 and 8 respectively.

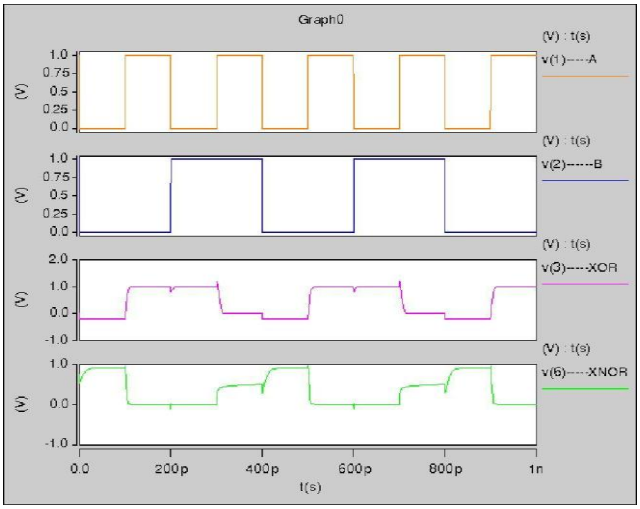

Figure 5: Output for design-I

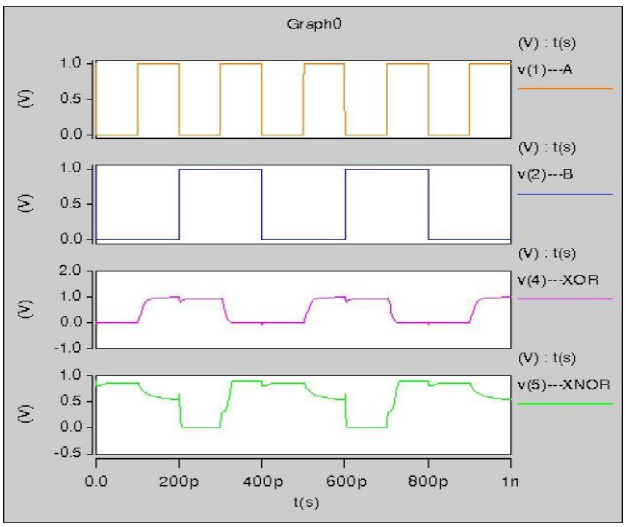

Figure 6: Output for design-II

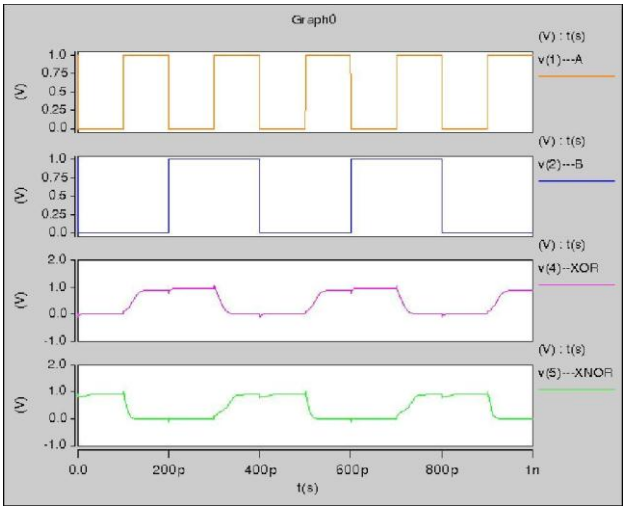

Figure 7: Output for design-III

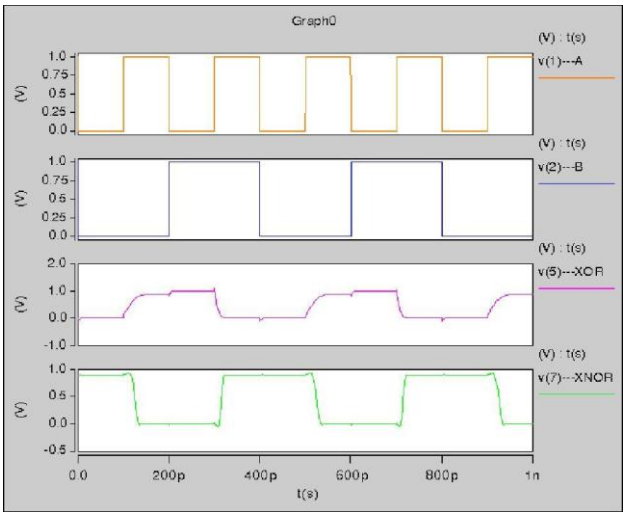

Figure 8: Output for design-IV

Comparison between all designs of XOR/XNOR gate with respect to different factors like power, delay etc at V_{dd} = 0.9V using 32nm UMC CMOS technology is mentioned in Table II.

Table II: Comparison between different designs

Parameter	Design I	Design II	Design III	Design IV
No. of Transistors	8	10	10	10
Average Power (µW)	0.22	0.87	0.91	0.42
Delay time for XOR (ps)	155.15	160.81	167.02	160.16
Delay Time for XNOR (ps)	203.77	209.86	168.09	170.02
PDP for XOR (fJ)	0.034	0.14	0.15	0.067
PDP for XNOR (fJ)	0.045	0.18	0.16	0.071

IV. CONCLUSION

In this paper we have proposed four designs of XOR/XNOR gate based on CMOS inverters, NMOS digital switches, pass transistors and GDI cell. Each circuit has been designed using 32nm UMC CMOS technology for the supply voltage of V_{dd} = 0.9V and simulated in HSPICE design tool. These circuits are efficient in arithmetic operations and other VLSI applications with less power consumption, less time delay and greater speed.

Transistors' characteristics for each design are mentioned below.

Table III: Transistors' characteristics for Design-I

MOSFET	W/L ratio
M1	0.438
M2	0.625
M3	0.375
M4	0.406
M5	0.469
M6	0.563
M7	0.469
M8	0.375

Table IV: Transistors' characteristics for Design-II

MOSFET	W/L ratio
M1	0.375
M2	0.469
M3	0.375
M4	0.469
M5	0.375
M6	0.625
M7	0.469
M8	0.563
M9	0.469
M10	0.375

Table V: Transistors' characteristics for Design-III

MOSFET	W/L ratio
M1	0.938
M2	0.781
M3	0.625
M4	0.625
M5	0.938
M6	0.625
M7	0.781
M8	0.625
M9	0.625
M10	0.625

Table VI: Transistors' characteristics for Design-IV

MOSFET	W/L ratio
M1	0.375
M2	0.625
M3	0.375
M4	0.469
M5	0.5
M6	0.469
M7	0.375
M8	0.469
M9	0.469
M10	0.375

ACKNOWLEDGEMENT

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Author's Profile

Rakesh Khandelwal is working as an Assistant Professor in MNIT, Jaipur. He has completed M.Tech from Malviya National Institute of Technology, Jaipur in VLSI Design. His interests are microelectronics, low power circuit design.