FIR Filter Designing Using Wallace Multiplier

Swati Chulet, Himanshu Joshi

***Abstract*— Finite Impulse Response filters are the most important element in signal processing and communication. FIR filter architecture contain multiplier, adder and delay unit. So, performance of FIR filter is mainly based on multiplier. In this paper we present FIR filter implementation of Wallace multiplier. This technique is used to improve the performance of delay, power and Area. The code is written in VHDL and it is simulated in ModelSim 6.3c and synthesis is done in Xilinx ISE 9.2i. Finally the design is implemented in Spartan-3 FPGA**

***Index Terms*—FIR filter, Wallace Multiplier, VHDL.**

I. INTRODUCTION

A filter is frequency selective network, which is used to modify an input signal in order to facilitate further processing. Basically there are two types of filters-analog and digital. Digital Filters are widely used in different areas, because Digital filters have the potential to attain much better signal to noise ratio than analog filters [1]. The digital filter performs noiseless mathematical operations at each intermediate step in the transform and their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain with analog filters Digital filters operate on numbers opposite to analog filters, which operates on voltages. The basic operation of digital filter is to take a sequence of input numbers and compute a different sequence of output numbers. There exists a range of different digital filters. FIR and IIR filters are the two common filter forms. A drawback of IIR filters is that the closed-form IIR designs are preliminary limited to low pass, band pass, and high pass filters, etc. secondly FIR filters can have precise linear phase.

Finite impulse response (FIR) filters are widely used in various DSP applications .This paper describes an approach to the implementation of low power digital FIR filter based on field programmable gate arrays (FPGAs).The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches [2]. Firstly, a single MAC unit is designed, with suitable geometries that give optimized power, area and delay. Similarly, the N no. of MAC units are controlled and designed for low power using a control logic that enables the each stage at appropriate time. Multiply –Accumulator unit has become one of the essential building blocks in digital signal processing applications such as digital filtering, video coding, speech processing, and cellular phone.

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II. MATHEMATICAL RELATION FOR FIR FILTER

Filters are very essential part of digital signal processing applications. Filters have two uses, one is signal separation and second one is signal restoration. Signal separation is used only when the signal is contaminated with noise or other unwanted signals [3]. Signal restoration is used only when the signal has been distorted. In general filtering is described by simple convolution operation such as

$$Y(n) = x(n) * f(n) = \sum_{k=0} f(k)\, x(n-k) \ldots\ldots (1)$$

The digital filters are commonly linear time invariant filters. The straight forward way of implementing LTI Finite Impulse Response filter is finite convolution of input series x(n) with impulse response coefficients is given by

$$Y(n) = x(n) * f(n) = \sum_{k=0} L-1 f(k)\, x(n-k) \ldots\ldots (2)$$

where L is the length of FIR filter, h(n) is filters impulse response coefficients, x(n) is input sequence and y(n) is output of FIR filter[4]. The above equations can also expressed in Z domain as

$$Y(z) = x(z)\, H(z) \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

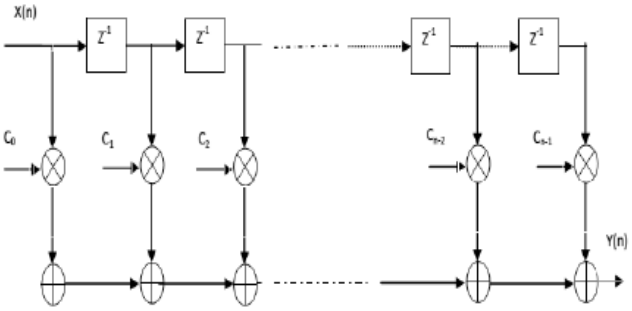

Fig. 1 FIR Filter Structure

Structure of FIR filter is shown in Figure 1. Normally the filter structure has one delay element, one multiplier and an adder for each number of stages. This complete element is known as tap. The number of stages is depending upon the length of the filter. And also this is directly proportional to the tap [4].

III. WALLACE TREE MULTIPLIER

A Wallace tree multiplier is an efficient hardware implementation of a digital circuit that multiplies two integers. Wallace tree reduces the number of partial products and use carry select adder for the addition of partial products. Wallace tree is known for their favorable computation time, when adding multiple operands to two outputs using 3:2 or 4:2 compressors or both. Wallace tree guarantees the lowest whole delay [5].

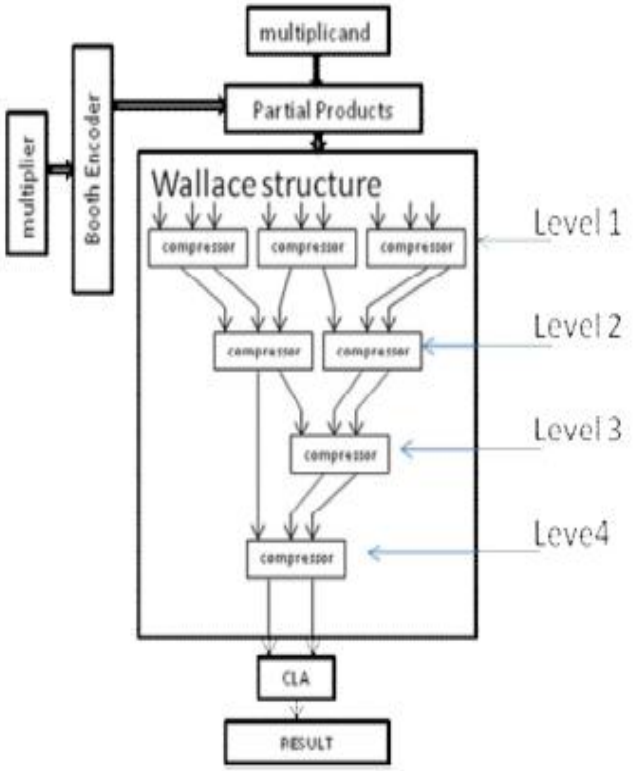

Fig. 2 Wallace Structure Multiplier.

Fig. 2 shows nine operands Wallace structure, where 3:2 compressors compress the data having three multi-bit inputs and two multi-bit outputs. 4:2 compressors compress the data having four multi-bit inputs and two multi-bit outputs.

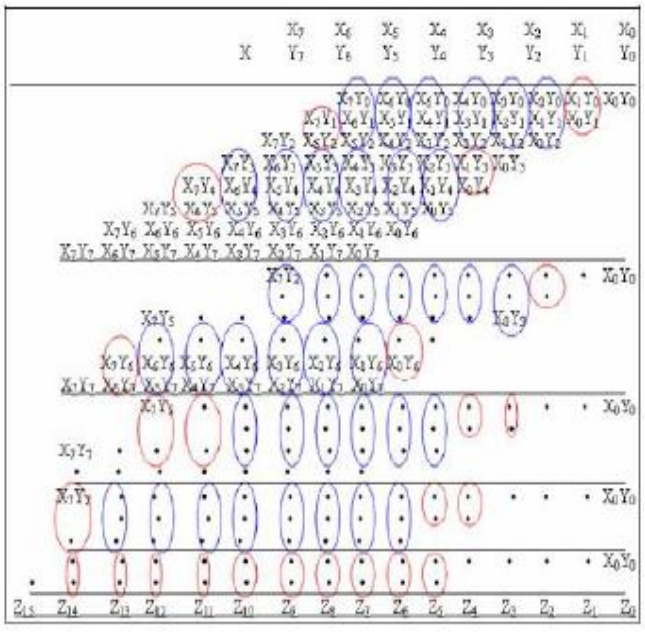

Fig. 3 8 bit*8 bit Wallace tree multiplier

In fig. 3 blue circles represent full adder and red circle represent the half adder.
Wallace tree has three steps [6]:-
1. Multiply each bit of multiplier with same bit position of multiplicand. Depending on the position of the multiplier bits generated partial products have different weights.
2. Reduce the number of partial products to two by using layers of full and half adders.
3. After second step we get two rows of sum and carry, add these rows with conventional adders.

IV. RESULTS

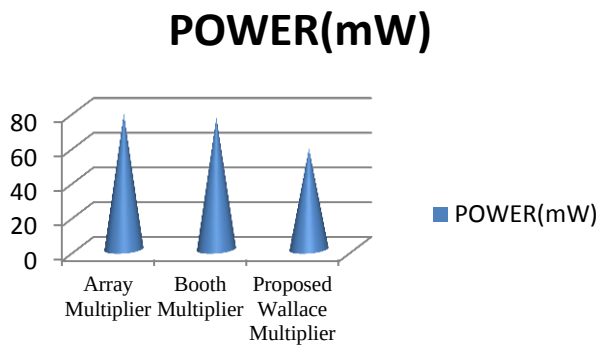

Fig. 4 Graphical Comparison of Power

The graph shows that the power of the previous FIR Filter design is more as compared to proposed design, hence we can say that the proposed FIR filter design using Wallace multiplier is less power consuming than the previous design which is our desired result and it will increase the efficiency.

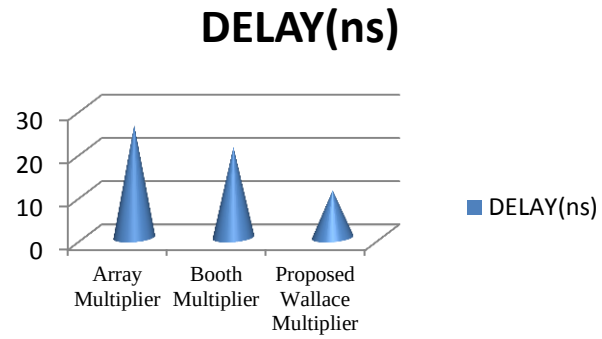

Fig. 5 Graphical Comparison of Delay

The graph shows that the delay of the previous FIR filter designs is more as compared to proposed design, hence we can say that the proposed FIR filter design using Wallace multiplier is faster than the previous designs which is our desired result and it will increase the efficiency by decreasing time complexity.

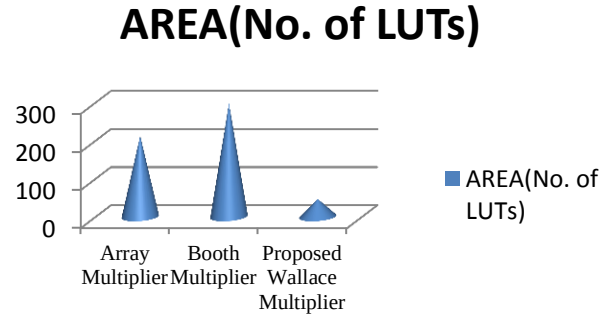

Fig. 6 Graphical Comparison of Area

The graph shows that the no. of LUT's used in the previous designs are more as compared to proposed FIR filter design using Wallace multiplier, hence we can say that the

proposed FIR filter design using Wallace multiplier use less no. of LUTs as compared to the previous design which is our desired result and it will increase the efficiency by decreasing the complexity of circuit and also the cost of manufacturing of a chip.

Table 1 Comparison

Multiplier	Power(mW)	Area(No. of LUT's)	Delay(ns)
Array	78	213	26.082
Booth	76	298	20.974
Wallace	58	47	10.92

The above table indicates the overall comparison of all parameters of the system i.e., it is clear from the table that proposed design is better in all the fields.

V. CONCLUSION

Table 1 shows the Comparison of Previous Designs and Proposed Wallace Multiplier Design. It was clear that there is a decrease in circuitry, power consumption, time consumption as compared to the previous designs. The code is written in VHDL. It is simulated by using ModelSim 6.3c. Synthesis is done in Xilinx ISE 9.2i. It is implemented in Spartan XC3s400. The proposed design is efficient to use in DSP applications.

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