Multilevel Inverters: A Survey of Different Topologies and Controls

Yasmeen Fatima, Renu Yadav, Rameshwar Singh

***Abstract*— Multilevel inverter (voltage source converter) is emerging as a new methodology of power electronics converter; provide options for medium and high-power voltages. Multi level inverter produce typically the staircase voltage wave, from several dc voltage source, this DC voltage source received form different renewal energy source as solar cell, fuel cell etc. one of the major limitations is higher the complexity due to gate driver circuit. This paper presents and analysis of different basic multi level inverter topology used currently as 1) diode-clamp, 2) cascaded- hybrid multi level inverters (CHB MLI), and 3) flying- capacitors (FC-MLI). This paper is also present different type of switching scheme used in multi level topology such as Sinusoidal pulse width of modulation scheme.**

***Index Terms*— Multilevel inverters, MLI, hybrid topologies, asymmetric and symmetric voltage source configuration, CHB, THD, phase shift pulse width modulation, PWM, sinusoidal pulse width modulation, phase opposition disposition.**

I. INTRODUCTION

In the beginning there was available only two level of inverter that has two level voltages i.e. +V and –V, these two level of voltage switched from Pulse width modulation technique and this methodology create effective harmonics distortion, EMI and dv/dt stress [1-3]. The main problem is present higher ratio of Total harmonics distortion (THD) in wave form, and another problem it is hard to connect directly power electronics switch to high voltage and medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV)[6]. Solution of all these problems, the new multi level inverter methodology was invented, multi level inverter working with higher number of voltage levels, as a result the multi-level inverter output voltages have reduced harmonic distortions profile and smooth sinusoidal wave form and power electronics switch working with different voltages stress[9 11].
Multilevel inverters have received more attention in industrial application such as static VAR compensators,

renewable energy systems and motor driver etc[16]. A number of multilevel inverter topologies have been invented during the last few decades, major multi-level inverter topologies are cascaded H-bridges multi-level inverter (CHB-MLI) with separate dc sources, diode clamped multi level inverter (DC-MLI), and flying capacitors multi-level inverter (FC-MLI)[2 3].

Yasmeen Fatima, Electrical Engineering Department, NITM/RGTU, Bhopal, M.P, India
Renu Yadav, Electrical Engineering Department, NITM/RGTU, Bhopal, M.P, India
Rameshwar Singh, Electrical Engineering Department, NITM/RGTU, Bhopal, M.P, India

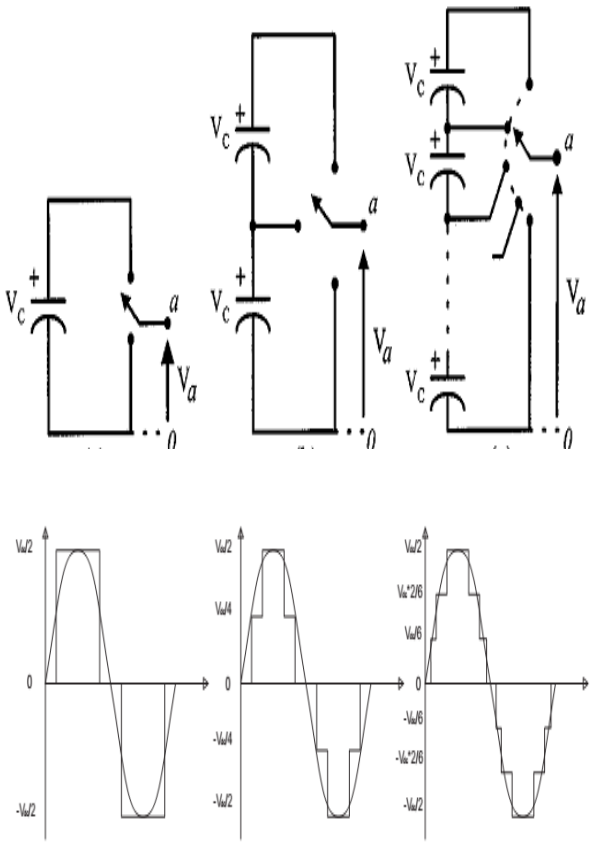

Fig. 1. single phase of an inverter with (a) two levels, (b) three levels, and(c)nlevels.

Multi level inverter includes number of ideal power switch: capacitor and flying diode are connected to get higher number of stepped waveform; the term introduced multilevel starts with the three-level inverter [4]. By increasing the number of voltage levels in the inverter, the output voltages have more steps producing as a staircase waveform, which has a reduced total harmonic distortion and dv/dt stress. However, a high number of levels create the control complexity and introduces voltage imbalance problems.

II. DIODE-CLAMP MULTILEVEL CONVERTER

In this circuit, the dc-bus voltage is split into five levels by four series-connected bulk capacitors and middle point of the four capacitors can be defined as the neutral point. The output voltage has five voltage level: $V_{dc}/2$, $V_{dc}/4$, 0, - $V_{dc}/2$ and -$V_{dc}/4$. Voltage level $V_{dc}/2$ Switch $\mathbf{S_1}$, $\mathbf{S_2}$, $\mathbf{S_3}$, $\mathbf{S_4}$ need to be turned ON and for - $V_{dc}/2$ voltage switch $\mathbf{S_4}$, $\boldsymbol{S_1'}$, $\boldsymbol{S_2'}$, $\boldsymbol{S_3'}$, need to be turned ON. The voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes[3 4].

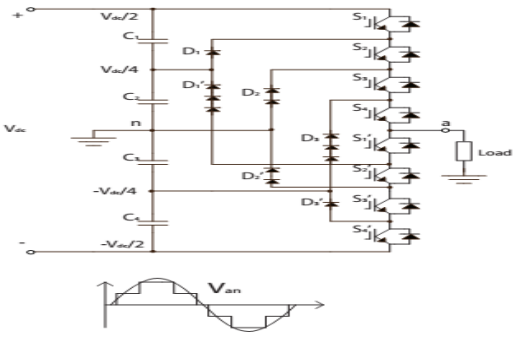

Fig. 2. Diode-clamped multilevel inverter circuit topologies of Five-level.

To explain how the staircase voltage is synthesized, the point (neutral) "n" is considered as the output phase voltage reference point. There are some switch combinations to synthesize five level voltages across a and n. which explain shown below in table

Table.1: Switch states for five level capacitor clamped inverter, "1" means turned ON and "0" means turn OFF switches

Output voltage	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/2$	0	0	0	1	1	1	1	0
$-V_{dc}/4$	0	0	0	0	1	1	1	1

2.1. Advantages

1. When the numbers of voltage levels are high enough, total harmonic content will be low enough to avoid the use of filters.
2. Working efficiency is high because all working devices are switched at the fundamental switching frequency.
3. Reactive power flow can be controlled by this technique.
4. The control method is simple for a back-to-back system.

2.2. Disadvantages

1. Higher numbers of clamping diodes are required when the numbers of levels are high.
2. It's difficult to do real power flow control.

III. Flying-Capacitor Multilevel Converter

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility and efficient than the diode-clamped converter as shown in figure 3. The voltage of a five-level phase-leg output with respect to the neutral point n, five level voltages can be synthesized by the following voltages combinations: $V_{dc}/2$, $V_{dc}/4$, 0, - $V_{dc}/2$, $-V_{dc}/4$, For voltage level $V_{dc}/2$ switches need to turned ON as $\mathbf{S_1}$, $\mathbf{S_2}'$, $\mathbf{S_3}'$, $\mathbf{S_4}'$ and - $V_{dc}/2$ voltage switch for $\mathbf{S_1}$, $\mathbf{S_2}$, $\mathbf{S_3}$, $\mathbf{S_4}$ need to be turned ON.

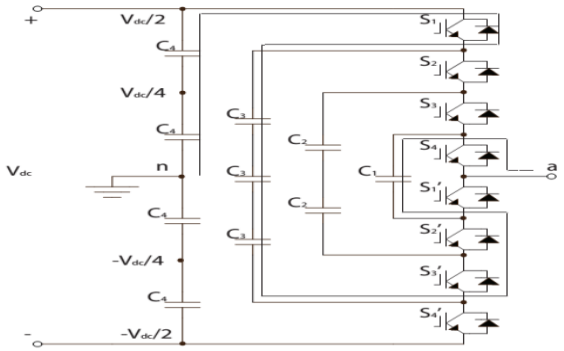

Fig.3. Capacitor-clamped multilevel inverter circuit topologies of Five-level.

Shown in figure 3 using fundamental building block of capacitor clamp, the circuit has been called the flying capacitor inverter. The inverter in shown in figure produce five voltage levels.

Table.2: Switch stats for five level capacitor clamped inverter, "1" means turned ON and "0" means turn OFF switches

Output voltage	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-V_{dc}/2$	1	0	0	0	1	1	1	0
$-V_{dc}/4$	0	0	0	0	1	1	1	1

The capacitors with positive signs (+v) are in discharging mode, while those with negative sign (-v) are in charging mode. By Suitable selection of capacitor combinations, it is possible to balance the capacitor charge. Similarly in case of diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Noted that the voltage rating of each and every capacitor used is the same as that of the main power electronics switch [11-13].

3.1. Advantages:

1. Large number of storage capacitors provides extra ride through capabilities during power outage.
2. Provides switch combination redundancy for balancing different voltage levels.
3. When the numbers of levels are higher, total harmonic content will be low enough to avoid the use for filters.
4. Both reactive and real power flow can be controlled, making a possible voltage source converter candidate for high voltage dc transmission.

3.2. Disadvantage:

1. Higher number of storage capacitors required when the number of converter voltage levels are high. Higher voltage level systems are more difficult to package and much expensive with the required bulky capacitors.
2. The multi-inverter control will be very complicated and the switching frequency and switching losses will be high for real power transmission.

IV. CASCADED MULTI LEVEL CONVERTER

Cascaded hybrid multi inverters with separate dc voltage source efficient to use in comparison to the other two topology as there is no need of capacitors and diodes for clamping and there are used different asymmetric voltage source from renewal energy source as fuel cell, solar cell wind energy etc[16 17]. Higher number of voltage level can be achieved by adding inverter cell, produces smooth sinusoidal wave and lower THD ratio.
One of disadvantage is higher number of power electronics switches due to use of higher number of power switch controlling complexity increases[3].

Table.3: Switch stats for five level capacitor clamped inverter, "1" means turned on and "0" means turn off switches

Output voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{dc}/2$	1	1	0	0	1	1	0	0
$V_{dc}/4$	1	1	0	0	0	1	1	0
0	1	0	0	1	1	0	0	1
$-V_{dc}/2$	0	1	1	0	0	1	1	0
$-V_{dc}/4$	1	1	0	0	0	0	1	1

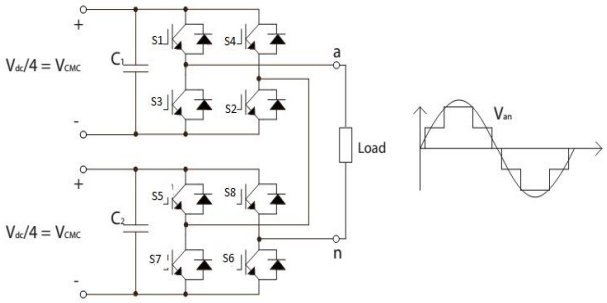

Fig. 4. Cascaded Hybrid multi-level-inverters with separate dc source.

4.1. Advantages:

1. Required least number of components among all multilevel converters to get the same number of voltage levels.
2. There is no need of clamping diodes and voltage balancing capacitors.
3. Soft-switching can be used in this structure to avoid bulky and less resistor-capacitor-diode snubber circuit.

4.2. Disadvantage:

1. Here needs separate dc voltage sources for real power conversions and so its applications are some time limited.

V. SWITCHING SCHEME

The switching scheme is dividing in two methods 1. High frequency switching scheme and 2. Fundamental frequency switching scheme for both cases stepped output wave form is achieved

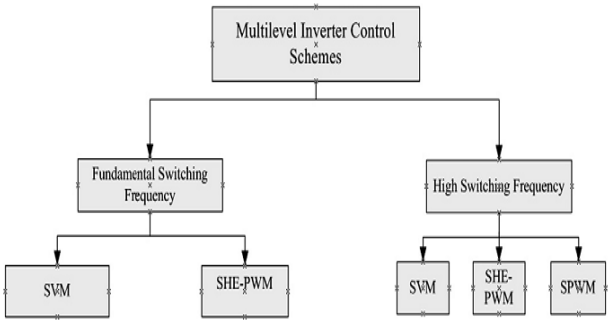

Fig. 5. Different PWM Techniques

Multi level inverter methods use high frequency carrier waves in comparison to reference wave that produce switch gate pulses and this modulation technique is help to reduce total harmonics profile[10].
There are some different PWM techniques as

1. Phase disposition (PD)
2. Phase opposite Disposition (POD)
3. Alternation Phase Disposition (APOD)
4. Phase shift (PS)

This technique shown in figure

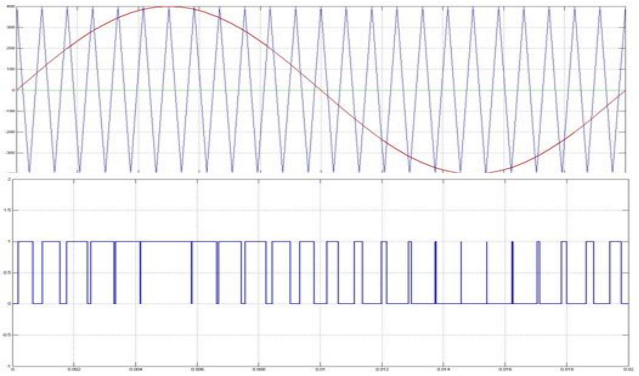

Fig. 6. PWM carrier triangular and reference sinusoidal wave and pulses.

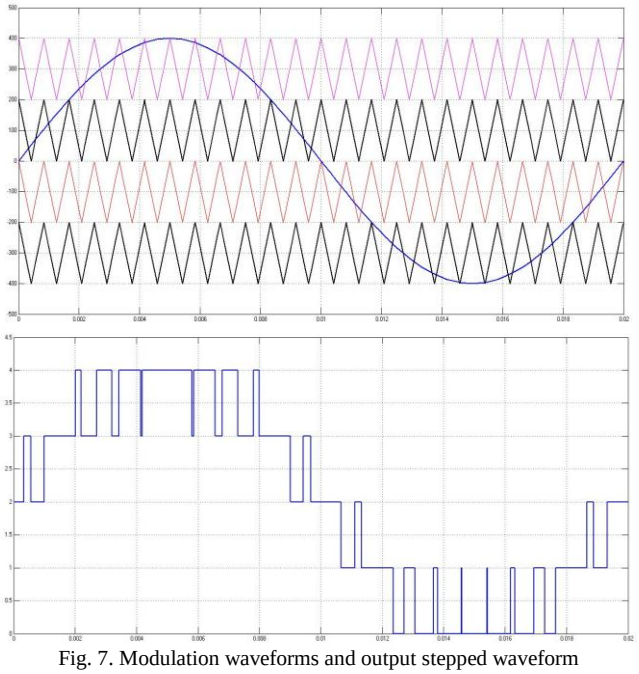

Fig. 7. Modulation waveforms and output stepped waveform

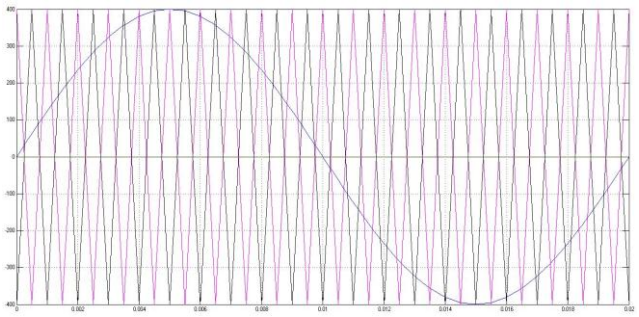

Fig. 8. Phase Shift (PS)

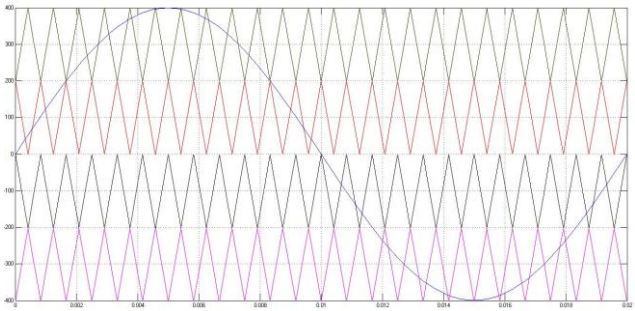

Fig.9. Alternate Phase opposite Disposition (APOD)

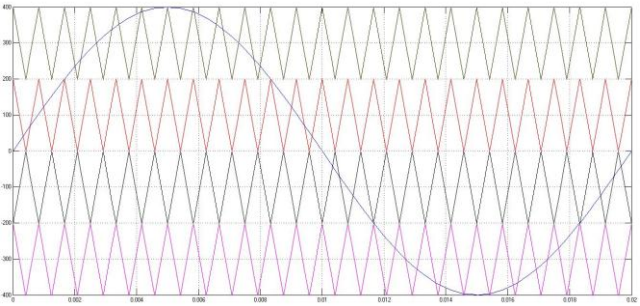

Fig.10. Phase opposite Disposition (POD)

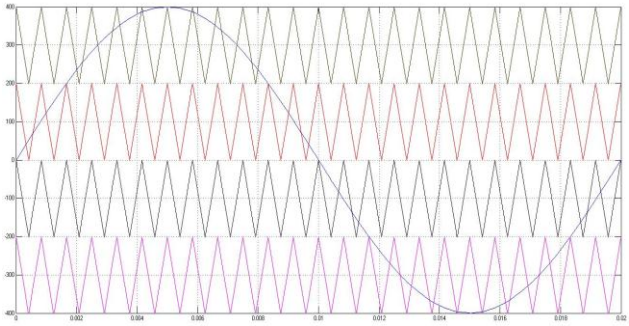

Fig.11. Phase Disposition (PD)

VI. Conclusion

This paper presents brief discussion on some basic multi-level inverter and control strategies. Multi-level inverter family help to solves problems of total harmonics distortion, EMI, and dv/dt stress on switch.Today more and more product commercial available which depends on the multi-level inverter topologies so that's why research work going on to reduces the power electronics components and improve total harmonics profile and total effective cost of the system.
Comparison is shown below in table

Table.4: Comparison of power component requirement

Inverter Configuration	Diode-Clamp	Flying-Capacitors	Cascaded inverter
Switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1)(m-1)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1)(m-2)/2	0

Where m is power components

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