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Optimization of Power Consumption in Bi-CMOS-OPAMP

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***Abstract*— BiCMOS integrated circuit for both digital and mixed-signal applications. Further reduced, making it very useful in all multimedia/communication signal processing ICs. Multimedia, electronics and communication devices have experienced explosive growth recently.In this thesis, the design and performance comparison of a two stage both the op amp circuits were designed and simulated, analyzed and performance parameters are compared Finally, we conclude the suitability of CMOS technology over BiCMOS technology for low power circuit design. A optimize power dissipation of different types of OP-AMP power calculation is specified, analyzed and implemented using the Tanner Tool software. In this project, we presented a calculation of the different types of parameter of CMOS OP-AMP and Bi-CMOS OP-AMP which adopts several innovative techniques to reduce power consumption. The CMOS OP-AMP with pmos and nmos can effectively eliminate power consumption in device. The Bi-CMOS technique used for the reducing slew rate increasing gain in the circuit , it can eliminate the power wasted on analog circuit.**

***Index Terms*— BiCMOS integrated circuit, OP-AMP power calculation, CMOS OP-AMP and Bi-CMOS OP-AMP.**

I. INTRODUCTION

The evolution and adaptation of the microelectronics industry to the BiCMOS technology and its extended families provide a paradigm shift in the development of high-speed, low-power digital and analog integrated circuits. It has been proven in most literatures (see references) that the integration of bipolar and CMOS technologies are advantageous when used in optimized Micro-electronic circuitry in different applications such as telecommunications, mixed-signal, and radio-frequency microelectronics. The operation of both MOS and bipolar logic circuits has been well characterized over the years.Circuit designers with such knowledge allow themselves to make optimization and compromise at the process, device, and circuit design levels. is a comparable understanding for the BiCMOS logic circuits.

In this thesis, the design and performance comparison of a two stage both the op amp circuits were designed and simulated, analyzed and performance parameters are compared. The performance parameters such as gain, phase margin, CMRR, PSRR, power consumption etc achieved are compared. A optimize power dissipation of different types of OP-AMP power calculation is specified, analyzed and implemented using the Tanner Tool software.

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II. TOOL

T-Spice is in many ways like the industry-standard SPICE simulation program:

- Input language. T-Spice uses an extended version of SPICE's input language.
- Analysis modes. T-Spice performs the same basic analyses as does SPICE (DC, AC, transient, and noise).
- Device models. T-Spice incorporates all of SPICE's device models, and semiconductor device models for p-n diodes, BJTs, JFETs, MESFETs, and MOSFETs. Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow you to enter schematics.

Important of the Tool:

1. To develop an understanding of design and simulation of analog and digital logic circuits.
2. To get a basic understanding of layout of electronic circuits.
3. We will use Tanner tools for design and simulation.
4. This presentation introduces us to Tanner tools.
5. Analog and Transient Waveforms can be easily understood.

III. PARAMETER ANALYSIS

A optimize power dissipation of different types of OP-AMP power calculation is specified, analyzed and implemented using the Tanner Tool software. In this project, we presented a calculation of the different types of parameter of CMOS OP-AMP and Bi-CMOS OP-AMP which adopts several innovative techniques to reduce power consumption.

The Analysis and performance parameters such as:-
1. Input and Output resistance
2. gain,
3. phase margin
4. Slew rate
5. power consumption etc

IV. CIRCUIT DESCRIPTION AND RESULTS

A complete study of the CMOS op-amp circuit:

OP-AMPs are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc.

Here we show a two stage CMOS op-amp circuit with the transistor geometries shown in the below table:

S.NO	Transistor	W / L Ratio
1.	M1	110 / 8
2.	M2	110 / 8
3.	M3	40 / 8
4.	M4	40 / 10
5.	M5	140 / 10
6.	M6	90 / 10
7.	M7	140 / 10
8.	M8	140 / 10

Table 1- Transistor geometries for the CMOS Op-Amp circuit.

A detailed circuit schematic of the 5µm CMOS op amp which I have used in all my analysis is shown in figure 1

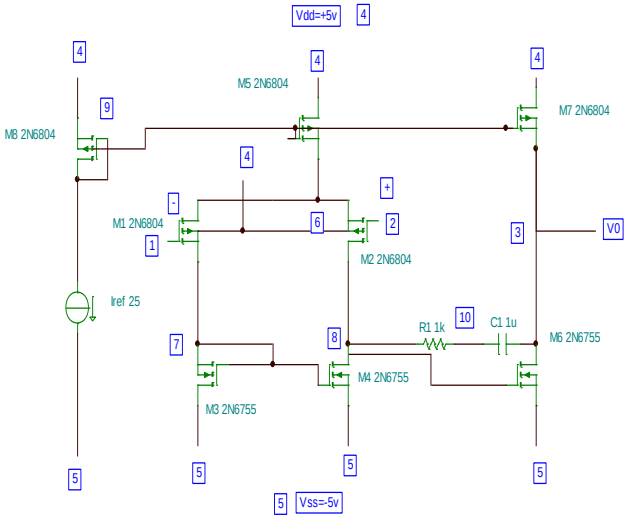


Figure 2- Cicuit of 5um C-MOS op-amp

Now we will find out parameters of the CMOS Op-amp In particular, we consider that each MOSFET is modeled after the transistors found in the 5µm CMOS process at Bell Northern Research (BNR).

Parameter analysis

Output voltage swing

Linear region is from -0.9 mV to +1.2 mV this corresponds to maximum output voltage swing bounded from -4.40V to +4.54V.

DC gain = output voltage swing / input voltage swing
= 4.54 volts - (-4.40 volts) / 1.2mV – (0.9 mV)
= 8.94 volts / 21.0 mV
= +4.257 kv/v

Input bias current

the remaining transistors are operating in their active regions. Other DC information, such as input bias current, static power dissipation, and so on, was calculated through **.OP** command. We can then repeat the DC analysis with the following element statement.

Vd 101 0 DC -220.0uv

Simulation

Gain and frequency response of the 5µm C-MOS Op-amp . First the input differential excitation should be changed to include an AC voltage component. 1v amplitude is commonly chosen for the input signal because the output voltage then directly represents the transfer function of the circuit. Thus the input excitation statement should be changed to read:

Vd 101 0 DC 220.0uv AC 1v

We also request the Spice compute the frequency response of the amplifier over a frequency interval beginning at 0.1 Hz and ending at 100 MHz using the following statement:

.AC DEC 10 0.1Hz 100MegHz

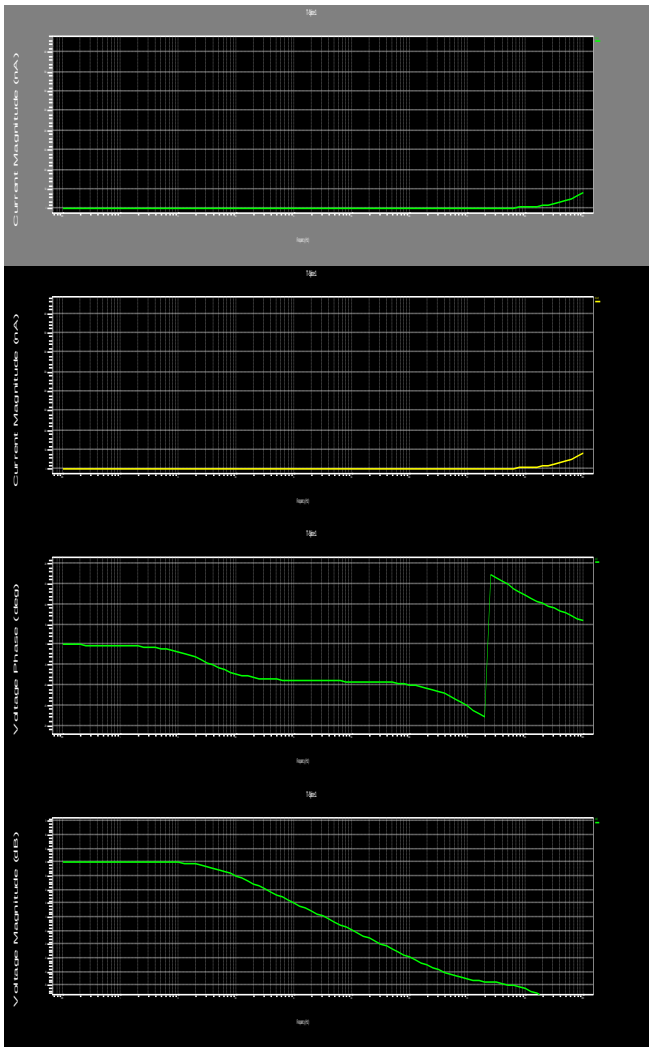


Figure 4.4 Frequency and phase response of the 5µm CMOS op-amp. Slew rate of the 5um C-MOS op-amp

A**.PLOT** statement can be included to request graphical display of the frequency response analyses output voltage:

.PLOT AC Vdb(3) Vp(3)

We will also include a **.PRINT** statement for the magnitude of

the small-signal current flowing through the two VCVSs in series with the op-amp input terminals. The command line for this is

.PRINT AC Im(EV+) Im(EV-)

The Spice input deck for computing the frequency response of CMOS op-amp. On the completion of the above mentioned program we will get the waveforms which shown in the page.

Slew rate of the 5um C-MOS op-amp

Slew rate limiting is an important attribute of op-amp behavior and usually limits the high-frequency operation of op-amp circuits.

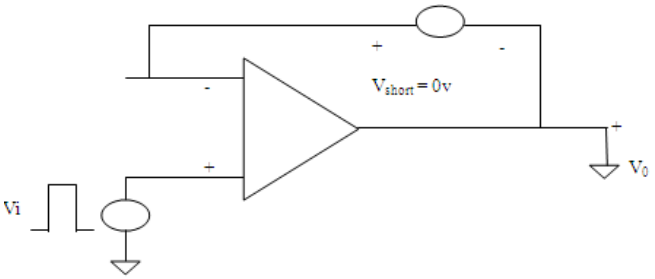


Figure 4.5 Circuit arrangement for computing op-amp positive and negative going slew-rate limits.

Figure 4.4 shows that how we can connect the op-amp in a unity gain configuration and apply a large voltage pulse to its input so as to revel both its positive going and negative going slew rates.

Here a zero-valued voltage source described by

Vshort 2 22 0

is used to form a direct connection between the op-amp output and its negative input terminal. Another voltage source is used to create the input pulse:

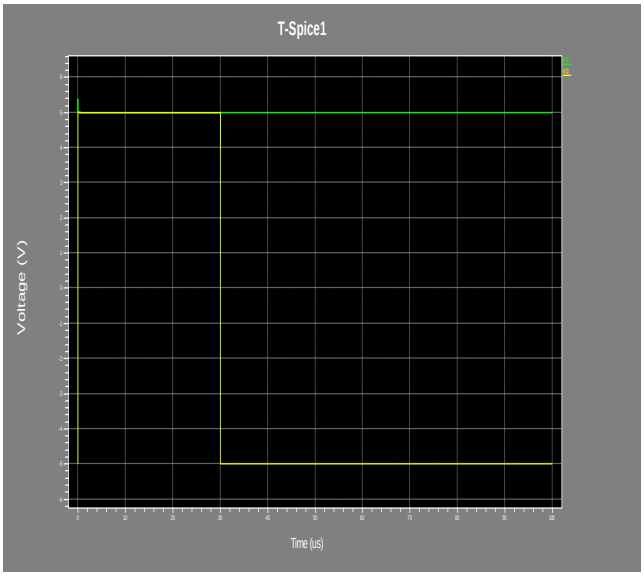


Figure 4.6 Input and Output transient voltage waveforms of the 5µm CMOS op-amp circuit connected in a unity-gain configuration. Both the positive-going and negative-going slew rate limits of the op-amp are evident from these results.

Vd 1 0 PWL (0, -5v, 1ns, +5v 30000ns, +5v 30001ns, -5v 1s, -5v)

On the completion of the above Spice input deck the waveform editor will show the following results:

The above figure shown for the slew rate of 5µm CMOS can be split in two separate part for both input and output transient voltage waveform as:

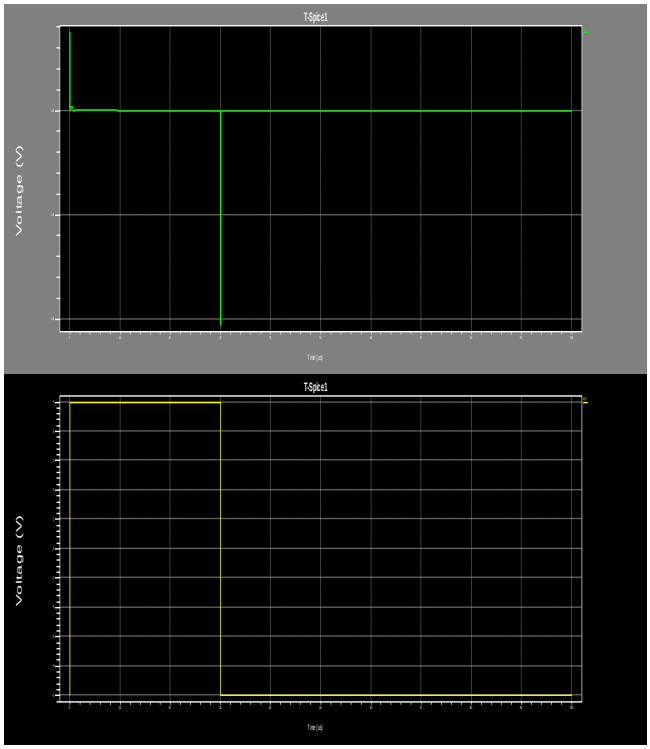


Figure 4.7 The transient voltage waveform which is shown above for output and the waveform which is shown below is for input.

BI-CMOS Op-Amp AC Analysis (1KHz frequency)

Parameter Analysis

Calculation for voltage gain

Vm(8) = 1.000E+00 Vp(8) = 0.000E+00

Vm(4) = 14.5790E+00 Vp(4) = -19.292E-06

So we find that this amplifier has a mid-band voltage gain

$$Av = \frac{Vm(4)}{Vm(8)} = 14.58$$

Calculation for input resistance

Vm(8) = 1.000E+00 Vp(8) = 0.000E+00

Im(vin) = 16.400E-12 Ip(vin) = -90.000E+00

So we find that this amplifier has a mid-band voltage gain

$$Ri = \frac{Vm(8)}{Im(Vin)} = 60.976\ G\Omega$$

Calculation for current gain

Im(vin) = 16.400E-12 Ip(vin) = -90.000E+00

Im(vo) = 19.8710E-03 Ip(vo) = 180.000E+00

So we find that this amplifier has a mid-band voltage gain

$$Ai = \frac{Im(Vo)}{Im(Vin)} = 1.211x10^9$$

Calculation for Output resistance

Vm(4) = 14.5790E+00 Vp(4) = -19.292E-06

Im(vo) = 19.8710E-03 Ip(vo) = 180.000E+00

So we find that this amplifier has a mid-band voltage gain

$$Ro = \frac{Vm(4)}{Im(Vo)} = 733.68\Omega$$

Simulation

Current Gain

To determine the output resistance of this amplifier we repeat this same process but set the level of the input voltage source to 0V and increase the level of the voltage source in series with the load resistance to 1V AC.

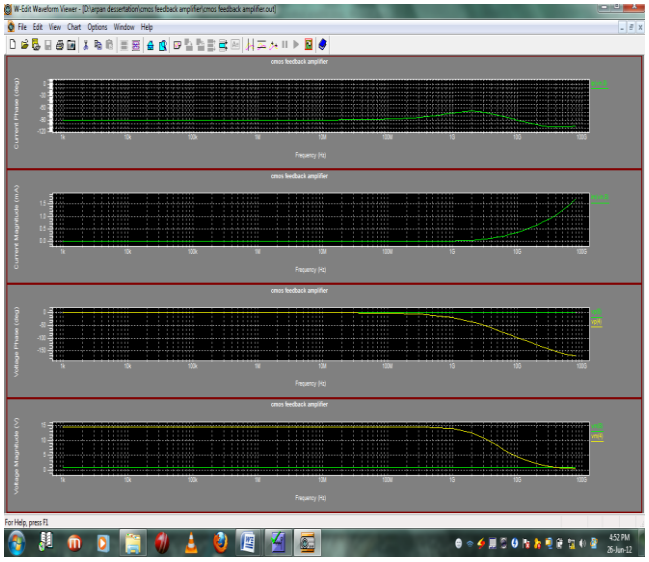


Figure 4.12 BI-CMOS Op-Amp Input output Current

BI-CMOS Op-Amp slew rate analysis

Slew rate of Bi-CMOS Op-Amp can be calculated from the formula dv/dt

V2 – V1 / T2 – T1 = 3.66 v / 80.02 * 10^{-12} = 0.0457 V/ pico-second

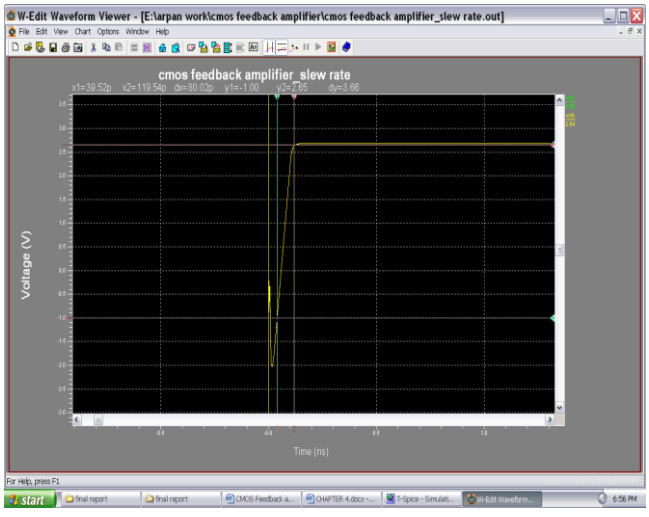
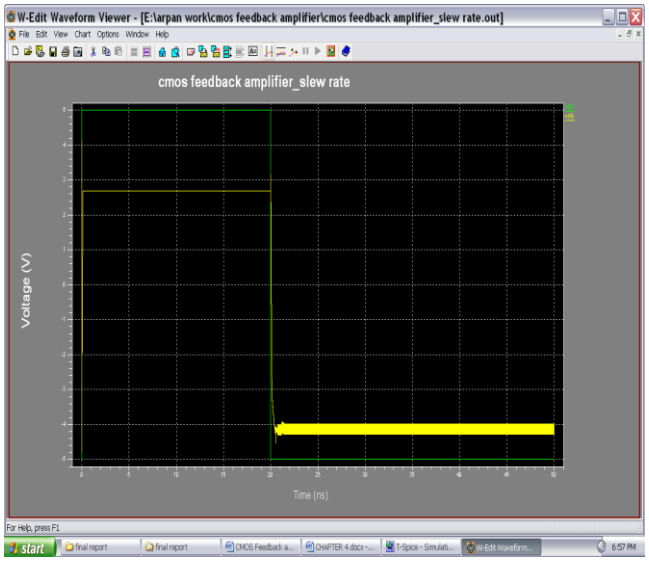


Figure 4.13 Slew rate of BI-CMOS Op-Amp (zoom of rising edge)

The total power dissipation can be calculated by **P=V*I**. Here current at Power supply is from +5 volts to -5 volts that is equal to 10 volts and current at Vcc is 5.9408E-04 so power can be calculated as:

Power dissipation = 10 * .59408 * 10^{-3} = 5.9408 mW



4.14 BI-CMOS Op-Amp power consumption analysis

We find that spice produces the magnitude and the phase of the output voltage and output current of the Op-Amp as above.

V. RESULT

Under following table shows the mathematical comparison between the CMOS and Bi-CMOS OPAMP with the different types of parameter:-

S.NO	PARAMETERS	CMOS OP-AMP	Bi-CMOS OPAMP
1.	Voltage Gain	10.33	14.58
2.	Input Resistance (R_I)	74.34	60.97 Ω
3.	Output Resistance (Ro)	687.64	733.68 Ω
4.	Current Gain (A_i)	0.8211 × 10^9	01.211 × 10^9
5.	Slew Rate (SR)	0.0335	0.0457 V/ Pico Sec
6.	Power Dissipation	07.8769	05.9408 mW

Table 2- Mathematical comparison of parameter between OP-AMP

VI. CONCLUSION

In this thesis, a optimize power dissipation of different types of OP-AMP power calculation is specified, analyzed and implemented using the Tanner Tool software. In this project, we presented a calculation of the different types of parameter of CMOS OP-AMP and Bi-CMOS OP-AMP which adopts several innovative techniques to reduce power

consumption. The CMOS OP-AMP with pmos and nmos can effectively eliminate power consumption in device. The Bi-CMOS technique used for the reducing slew rate increasing gain in the circuit , it can eliminate the power wasted on analog circuit.

Further reduced, making it very useful in all multimedia/communication signal processing ICs. Multimedia, electronics and communication devices have experienced explosive growth recently. Longer battery life is one of the crucial factors in the extensive success of these products. As such, low-power circuit design for multimedia and wireless communication applications has become very important and it circuit for applications has increased life. In order to achieve low power memory, our proposed design saves 12.5 % of power than a conventional design.

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