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Optimization of speed and power of BIST compatible UART

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Abstract— **The rising development of Integrated Circuits or sub-micron technology has resulted in the complexity of testing very complex circuits. Design and test engineers have no other alternative but to admit new tasks that they have to design systems with full testability, consistency and the functionality to evade the opportunity of product failures, errors and missed intent opportunities of market, that had been performed by groups of design and testing engineers in the previous years. BIST is the most general design method that allows self testability to evade the product failures. UART allows full duplex serial communication link, and is used in data communication and control system. There is a need for realizing the UART function in a single or a very few chips. A Universal Asynchronous Receive/Transmit (UART) with BIST capability has the objectives of testing the UART on chip itself and no external devices are essential to perform the test. The design is synthesized in Verilog HDL and consistency of the Verilog HDL implementation of UART is confirmed by simulated waveforms. The consequences indicates that this model eliminates the need for higher end, costly testers and thus it can decrease the development time and cost.**

Index Terms— **UART, FIFO, High speed, Transmitter, Receiver, Baud Rate Generator.**

I. INTRODUCTION

There is a vast establishment of the system takes place in the surroundings of the communication related to the phase of the serial phenomena plays a essential role in its ambassador study of the transmission of the data in a concurrent fashion respectively [1]. There is a communication of the data takes place in the successive way respectively. Asynchronous serial communication has merits of high consistency, less transmission line and long transmission distance, therefore is usually used to swap data between a computer and external devices [2]. UART implements asynchronous serial communication. It provides full-duplex communication in serial link; this has been widely used in the data communications. UART includes a transmitter and a receiver. Transmitter controls transmission by taking a data word in parallel layout and directing the UART to transmit it in a sequence. Similarly, the receiver must spot transmission, receive the data in sequence, and accumulate the data word in a parallel layout[3]-[4]. UART handles the conversion of serial to parallel data. Serial communication decreases the deformation of a signal; thus data transport is feasible between two systems estranged by large distance. The UART serial section is separated into three sub-sections: The baud rate generator, receiver module and transmitter module. The baud rate generator is used to generate a local clock signal. Once the baud-rate has been established, both the transmitter and the receiver's inner clock are set to the similar frequency in data transmission through the UART [4].

The sluggish and the speedy secondary devices for example: computer and printer or in between the controller and LCD. Since, UART is used frequently for the small distance, low speed and is of low cost. UART becomes more firm, consistent and compact for serial data communication [5]. Owing to which, the using up of LUTs, flip flops or in short the area consumption of the chip becomes reduces. A Universal Asynchronous Receiver Transmitter (UART), generally used for little distance, low speed, low cost data swap between processor and peripherals [5]-[6].

TRANSMITTER

Transmission function is simpler because it is beneath the control of the transmitting system. Although transmission of a single character may take a long time relative to CPU speeds, the UART will sustain a flag showing busy status. Full - duplex action needs characters to be sent and received simultaneously, two different shift registers for transmitted characters and received characters are used by practical UARTs [7].

RECEIVER

Every action of the UART hardware is controlled by a clock signal which runs at a multiple (say, 16) of the data rate - each data bit is as long as 16 clock pulses. The receiver tests the position of the incoming signal on each clock pulse, looking for the starting of the start bit. After waiting a further bit time, the state of the line is again sampled and the consequential level clocked into a shift register [7]. After the requisite number of bit periods for the character length (5 to 8 bits, typically) have gone, the contents of the shift register is made accessible (in parallel fashion) to the receiving system [7]-[8]. The UART will set a flag representing new data is available, and may also produce a processor interrupt to appeal that the host processor to transport the received data. In some general types of UART, a small first-in, first-out FIFO buffer memory is inserted between the receiver shift register and the host system boundary [8].

BIST

Built-in Self Test, or BIST, is the method of designing extra hardware and software features into integrated circuits to

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agree to them to perform self-testing, i.e., testing of their personal action using their own circuits, thereby falling dependence on external Automated Test Equipment (ATE) [9]. BlST is a method of self-testing on a system on chip due to the complication to verify caught at logic error using conventional methods such as bed of nails. In this paper, internal diagnostic capabilities are built into UART by the introduction of Built-In-Self-Test (BIST) and error simulation of data at receiver for any data corruption and thereby setting status flags. The UART with status register and BIST section is coded in Verilog HDL and simulated using Xilinx tool ISESIM. The entire execution and validation is done on Spartan 3A FPGA [10]. A properly designed BIST is able to offset the cost of added test hardware while at the same time ensuring the consistency, testability and reduces maintenance cost. BIST solution consists of a Test Pattern Generator (TPG), the circuit to be tested, a way to evaluate the results, and a way to condense those results for simplicity and handling.

II. SIMULATION

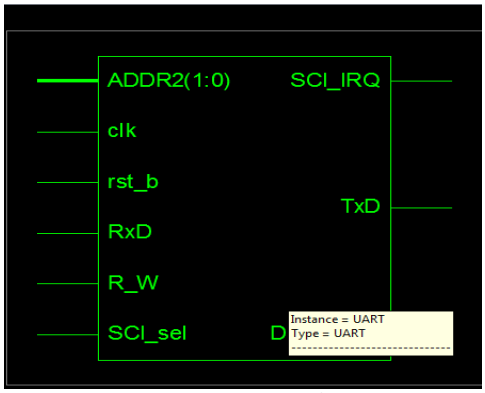

Fig. 1 Block Diagram of RTL

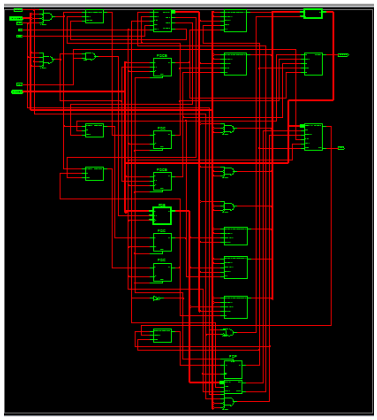

Fig. 2 Technology schematic

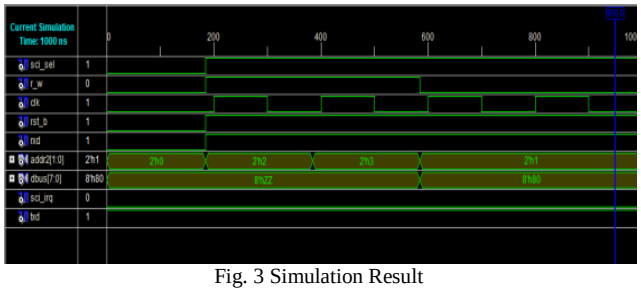

Fig. 3 Simulation Result

III. RESULTS

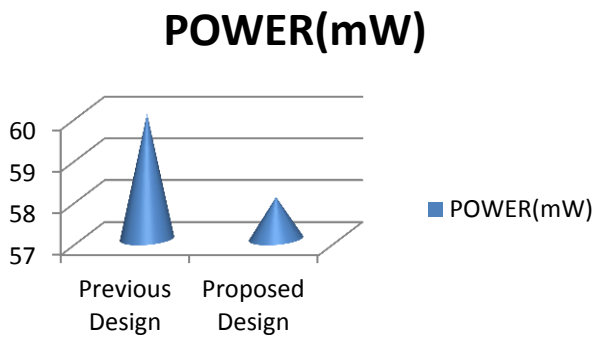

Fig 1 Graphical Comparison of Power

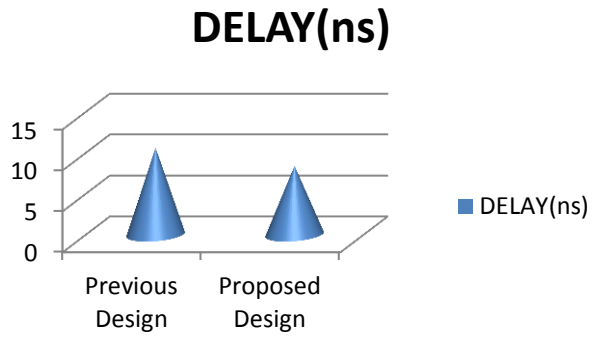

Fig 2 Graphical Comparison of Delay

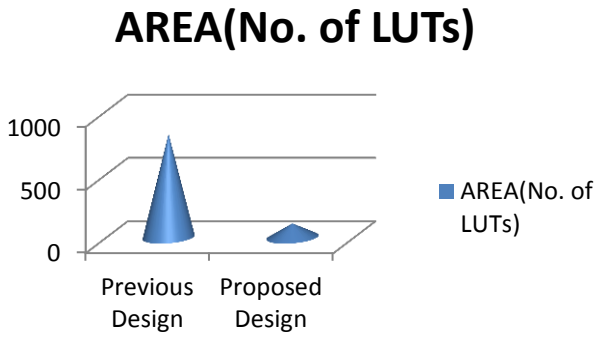

Fig 3 Graphical Comparison of Area

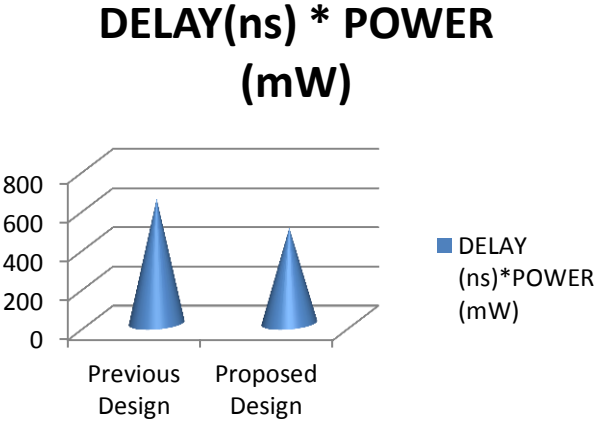

Fig 4 Graphical Comparison of Delay * Power

	POWER (mW)	DELAY (ns)	AREA (No. of LUTs)	DELAY(ns)* POWER (mW)
PREVIOUS DESIGN	60	10.592	819	635.52
PROPOSED DESIGN	58	8.39	110	486.62

Table 1 Overall Comparison of Previous Design and Proposed Design

IV. CONCLUSION

Table 1 shows the Overall Comparison of Previous Design and Proposed Design. It was clear that there is a decrease in circuitry, power consumption, time consumption as compared to the previous design, also the overall performance (delay (ns) *power (mW)) is reduced by 23.42%.

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