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Modelling and Design solutions for NANO- CMOS using Predictive Technology

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***Abstract*-The advances of CMOS technology have driven the exponential growth of IC design for the past decades. Although many technical problems have been resolved along the way, many new physical challenges emerge as CMOS is scaling into the nano-scale regime. Particular examples include power consumption, process variations, signal integrity, and reliability degradation. In this work an advanced compact modeling, circuit design techniques, and EDA tools for submicron CMOS technology by using predictive technology are discussed. Based on the HSPICE simulation software, emphasis is on the behavior of CMOS Inverter, NAND and NOR are processed. Modeling and design for silicon on insulator (SOI) and metal-gate transistors will be generated for future applications. The comprehensive understanding of transistors will provide a solid ground to analysis and design for nano-CMOS technology. The total memory required and power dissipation are the major observed parameters with reference to high speed (HP) and low stand by power (LSTP). The present work analysis the low power and high performance models of PTM with Hi-K metal gate CMOS technology by using them in an CMOS inverter, CMOS NAND and CMOS NOR at 16nm, 22nm, 32nm technology nodes. The aim of Hi-K metal gate technology is to reduce the leakage and it is a good alternative to CMOS bulk technology having high leakage and power dissipation. All the simulation is done with HSPICE simulator at 16nm, 22nm, 32nm technology nodes with PTM models. A comparison table was made between HP and LSTP by using three technology nodes 16nm, 22nm and 32nm for CMOS Inverter, NAND and NOR respectively. Finally, it is proposed to understand nano-scale CMOS design methodologies at present day scenario.**

***Index terms*-16nm, 22nm, 32nm CMOS inverter, NAND and NOR gates, Hi K metal gate strained Si, PTM HP and LSTP models, HSPICE.**

I. INTRODUCTION

Silicon CMOS has emerged over the last 25 years as the predominant technology of the microelectronics industry. The concept of device scaling has been consistently applied over many technology generations, resulting in consistent improvement in both device density and performance. Device dimensions are now well below the micrometer scale and into the nanometer regime [1]. With scaling, the heterogeneous components continue to be on a single chip. Analog, Digital and mixed signal devices continues to be on a single die for optimum cost and optimum performance. The present work analysis the low power and high performance models of PTM with Hi-K metal gate CMOS technology by using them in an CMOS inverter, CMOS NAND and CMOS NOR at 16nm, 22nm, 32nm Technology nodes. This work presents the high speed Inverter, NAND and NOR gates

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where substrate biasing is utilized to achieve the high speed but at the cost of higher power consumption. Hence this circuit is useful where speed is the first priority. So the PTM HP models are used where speed is the first priority and the PTM LSTP models to be used for low leakage applications. In my project work, the basic predictive technology models of CMOS INVERTER,NAND and NOR designed in the NANO regime especially for 16nm, 22nm and 32nm technology nodes. In predictive modeling, the Berkeley Predictive Technology Model (BPTM) [2] and the Arizona State University (ASU) PTM [3] were developed for planar CMOS technology nodes beyond22nm based on the BSIM4 model [4]. A new generation of Predictive Technology Model for Multi-gate (PTM-MG) devices has been developed for early-stage design-technology exploration.

The organization of this work shows as the PTM models of CMOS with high k metal gate technology is discussed in section II. In section III simulation results are shown and finally concluded in section IV.

II. PTM MODELS OF CMOS WITH HI-K METAL GATE TECHNOLOGY

PTM is developed by the Nano-scale Integration and Modelling (NIMO).Thepresent work analysis the low power and high performance models of PTM with Hi-K metal gate CMOS technology.This analysis gives an insight into leakages when the input voltage is sweeping from minimum to maximum voltage.The aim of Hi-K metal gate technology is to reduce the leakage at sub 32nm and sub 22nm nodes and is a good alternative to CMOS bulk technology having high leakage and power dissipation. All the simulation is done with HSPICE simulator at 16nm, 22nm, 32nm technology nodes with PTM models of Arizona state university.Miniaturization is a way of having highperformance

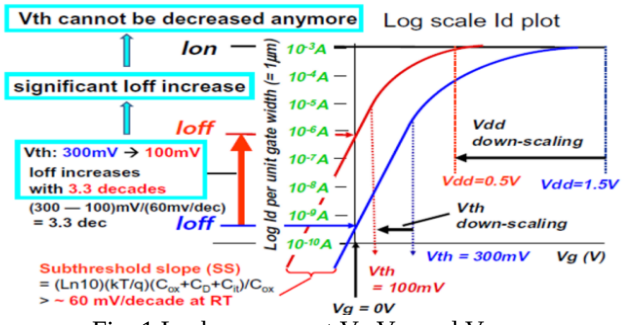

Fig. 1 Leakage current Vs,V_{dd} and V_{gate}

and low power CMOS circuits. So with scaling, power consumption as well as the cost of production decreases, with the decrease in supply voltage, the power consumption also decreases, and to decrease the supply voltage, the threshold voltage has to be reduced. With decrease in threshold voltage, the sub-threshold off leakage current

increases. Then Fig.1 shows the trend of Ids with Vg, with drain to source voltage and threshold voltage [5].The improper down scaling results in off stage leakage current and results in threshold voltage variations due to short channel effect. Thevariation in the device parameters in general is another hurdle with advanced technology node. And the trend is to opt for better alternative with respect totechnology such as insulator, metal gate high k technology etc.

The major issues as we go for low-stand by power (LSTP) technology is the leakage and power dissipation in the high performance technology is more. When the technology node is further reduced proportionally power dissipation is increased in the PTM HP model but proportionally the speed is also increased. So PTM HP model is used where speed is the first priority and the LSTP model is used where power reduction is necessary compare to higher speed. And it is necessary to analyze these technology models at a targeted technology, 16nm in this case, to know the extent of leakage, power dissipation and or reductions on these while using other technology. In the below section the two predictive technology low power and high performance models at High-K metal gate CMOS technology is done at 16nm, 22nm,32nm technology nodes. The comparative analysis shows result that the low power models to be used for low leakage applications and for faster performance the HP models are the best. The Static power dissipation is due to three major factors as leakage current, sub threshold current of transistors and tunneling effect of current. So optimization can be achieved by concentrating all these design issues.

$$P_{D_{STATIC}} = P(t) = i_{DD}(t)V_{DD} \qquad (1)$$

Here $i_{DD}(t)$ is the leakage current or static current and V_{DD} is supply voltage. From this it is clear that if leakage current increases, then static power increases. Hence threshold voltage represents a trade-off between performance and static power dissipation.

III. SIMULATION RESULTS

The CMOS Inverter, NAND and NOR (universal gates) are simulated using HSPICE and results are noted down and shown in fig (2),(3) and (4). The PTM high performance (HP) and low-stand by power (LSTP) models for CMOS inverter, NAND and NOR are simulated by using the HSPICE simulator. The simulation results is shown below. The HSPICE is an analog circuit simulator capable of performing transient, steady state and frequency domain analysis. Here these circuits are simulated in transient analysis. The simulation results is similar for all of the scaling technology nodes because the same inputs has to be taken here. The supply voltage is 1V. The below tables shown the comparison of the HP and LSTP models for three technology nodes 16nm,22nm,32nm for CMOS inverter, NAND and NOR (universal gates) for different parameters like total voltage source power dissipation, total memory used and the threshold voltage and drain current for both PMOS and NMOS (for inverter). From the tables we can observe that the power dissipation is increased when the scaling technology in further reduced in the PTM HP model. So the PTM HP models are used where speed is the first priority and the PTM LSTP models to be used for low leakage applications because the total voltage source power dissipation is decreased when compared to the PTM HP models.

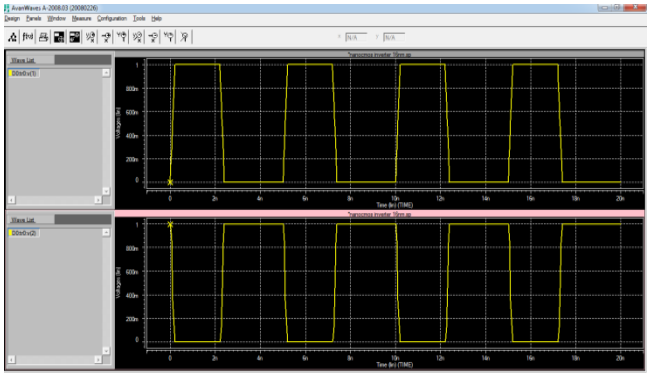

Fig2.Nano CMOS inverter output using HSPICE

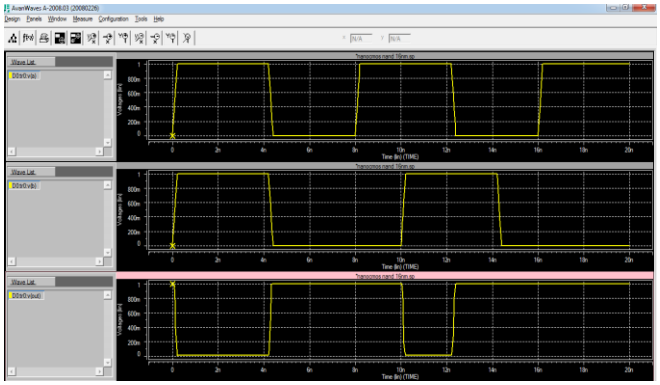

Fig3.Nano CMOS NAND output using HSPICE

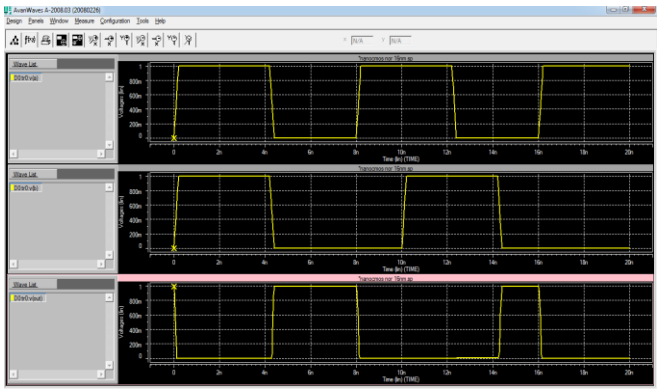

Fig4.Nano CMOS NOR output using HSPICE

IV. CONCLUSION

This paper presents the high speed and low power PTM models for an CMOS INVERTER, NAND and NOR gates. The HP models are used where substrate biasing is utilized to achieve the high speed but at the cost of higher power consumption. Hence this circuit is useful where speed is the first priority, and the LSTP models are used for low leakage applications. Analysis of the two predictive technologies low power and high performance models at High-K metal gate CMOS technology is done at 16nm, 22nm, 32nm technology nodes. The comparative analysis shows result that the Low power models to be used for low leakage applications and for faster performance the HP models are the best. So depending on the application one of these model is used.

Table I. Comparison of various parameters for technology nodes (16nm, 22nm, 32nm) of High-K metal gate CMOS Inverter with HP and LSTP PTM models.

Parameter\PTM models	HI-K_MG HP inverter (for 16nm)	HI-K_MG LSTP inverter (for 16nm)	HI-K_MG HP inverter (for 22nm)	HI-K_MG LSTP inverter (for 22nm)	HI-K_MG HP inverter (for32nm)	HI-K_MG LSTP inverter (for 32nm)
Supply Voltage	1V	1V	1V	1V	1V	1V
Temparature	25°C	25°C	25°C	25°C	25°C	25°C
Memory used	238 Kb	159 Kb	238 Kb	158 Kb	238 Kb	159 Kb
Voltage source Power dissipation	887.2056 n Watts	570.6208 p Watts	96.8043 n Watts	183.0833 p Watts	25.8075 n Watts	49.2006 p Watts
V_{th} (nmos) Cutoff	179.0278m	507.6454m	259.9582m	556.1218m	311.4548m	540.7670m
V_{th}(pmos) Linear	-394.1075m	-681.8345m	-440.3887m	-631.8459m	-481.2574m	-581.2745m
I_d (nmos) Cutoff	886.5840n	12.9377p	96.5928n	5.0240p	25.5906n	9.8769p
I_d (pmos) Linear	-886.9004n	-292.1291p	-96.7217n	-94.4763p	-25.7824n	-30.0096p

Table II. Comparison of various parameters for technology nodes (16nm, 22nm, 32nm) of High-K metal gate CMOS NAND with HP and LSTP PTM models.

Parameter\PTM models	HI-K_MG HP NAND (for 16nm)	HI-K_MG LSTP NAND (for 16nm)	HI-K_MG HP NAND (for 22nm)	HI-K_MG LSTP NAND (for 22nm)	HI-K_MG HP NAND (for32nm)	HI-K_MG LSTP NAND (for 32nm)
Supply voltage	1V	1V	1V	1V	1V	1V
temp	25°C	25°C	25°C	25°C	25°C	25°C
Total memory used	242 Kb	161 Kb	242 Kb	161 Kb	241 Kb	161 Kb
Total voltage source power dissipation	2.2997n Watts	1.1140n Watts	705.5837p Watts	354.7911p Watts	613.8527p Watts	77.7716p Watts

Table III. Comparison of various parameters for technology nodes (16nm, 22nm, 32nm) of High-K metal gate CMOS NOR with HP and LSTP PTM models.

Parameter\PTM models	HI-K_MG HP NOR (for 16nm)	HI-K_MG LSTP NOR (for 16nm)	HI-K_MG HP NOR (for 22nm)	HI-K_MG LSTP NOR (for 22nm)	HI-K_MG HP NOR (for32nm)	HI-K_MG LSTP NOR (for 32nm)
Supply voltage	1V	1V	1V	1V	1V	1V
Temp	25°C	25°C	25°C	25°C	25°C	25°C
Total memory used	241 Kb	161 Kb	241 Kb	161 Kb	241 Kb	161 Kb
Total voltage source power dissipation	1.6892u Watts	1.1412n Watts	192.9507n Watts	366.1652p Watts	51.5902n Watts	98.4010p Watts

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