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Dynamic Power Reduction In Energy Efficient Synchronous Circuits Using Clock Gating

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***Abstract*—Major source of dynamic power consumption in synchronous circuits is clock. Clock in synchronous circuits controls the functioning of circuit by providing signal which operates in two levels – high and low. Clock power can be reduced with commonly used technique of clock gating. This work proposes circuit design of a low-power Memory. The proposed circuit uses clock gating—a well known technique to reduce dynamic power consumption which is mainly due to switching activity when circuit is operational, clock gating works by disabling power supply to the portion of circuit which is not in use. This Gated Clock is implemented using AND gates, OR gates and a D latch. Instead of normal clock the memory is given a gated clock.**

***Index Terms*— Clock gating, dynamic power, low power design, synchronous circuits**

I. INTRODUCTION

With the recent developments in battery driven portable devices such as smart phones, laptops, Personal Digital Assistants etc. which requires higher performance, more functionality and long battery life [1]-[2]; there arises a need to design low power Very Large Scale Integrated (VLSI) circuits.

In digital circuits clock is used for synchronization of various components. The power consumed by clock in synchronous circuits is a major source of dynamic power consumption.

Dynamic power consumption can be checked using clock gating technique. By clock gating technique, clock to an inoperative section is deactivated, thus preventing power dissipation due to unnecessary charging and discharging of the idle circuit. In clock gating, clock is selectively blocked for a portion of circuit which is not performing any active computation [2].

In this paper, the work is carried on Memory for dynamic power reduction. Clock Gating is a method which decreases clock power but increases Logic Power due to additional logic in design. However, there is a substantial decrease in Input / Output Power and Signal Power due to decrease in frequency of operation of device. The increase in Logic and Signal power is comparatively small in magnitude than decrease in clock power [3]. Register Transfer Level (RTL) Clock Gating is the most commonly used optimization technique for reducing dynamic power. RTL provides early power estimation which helps the designer to rapidly explore different architectures and find power bugs early in the design before it is found too late at the gate-level where synthesis and place and route steps will take place recursively to meet the essential power budget for the design [4]. There are three ways to construct a clock gated circuit, these are (1) Gate based clock gating (2) Latch based clock gating (3) Flip Flop based clock gating [5]. Of all these, we are using latch based clock gating. In latch based clock gating technique, a level sensitive latch is used as the controlling factor, to control the Enable pin, that is fed to the "AND" or "OR" gate for gating the clock signal. This latch is allowed to reflect the change of Enable pin. The latch holds the value of enable signal from the active edge of the clock till the inactive edge of the clock. In this technique glitch problem is eradicated which is present in a latch free based design, since latch holds the state of enable till complete pulse is done [4] - [6] - [7].

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II. MEMORY WITHOUT CLOCK GATING

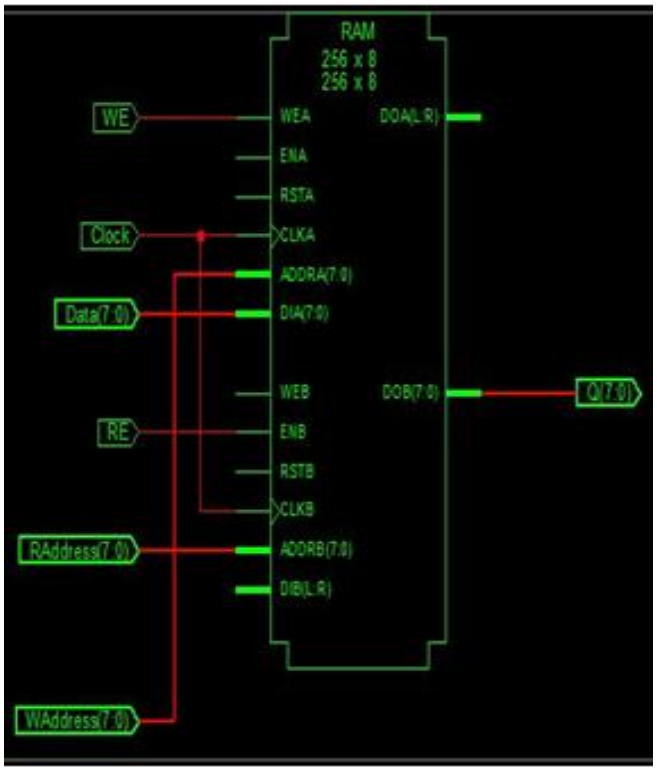

Figure 1: RTL Schematic of Memory

The figure 1 shows the RTL Schematic of RAM with detailed information having size of 256 bytes with input lines read, write, clock, data, enable, reset and address line and output line as data output bus.

III. CLOCK GATED MEMORY

The figure 2 shows the RTL Schematic of Gated Clock Memory with the use of an extra logic circuit implementing

the Gated Clock signal. This Gated Clock is implemented using AND gates, OR gates and a D latch. Instead of normal clock the memory is given a gated clock.

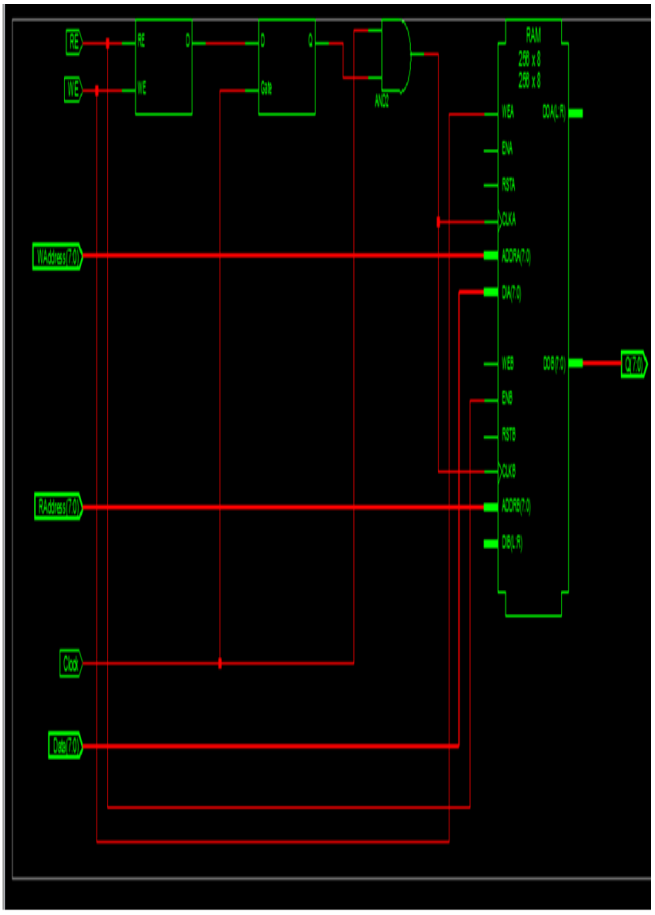

Figure 2 RTL Schematic of Clock Gated Memory

IV. RESULTS

The table shows the comparison between the Memory without Gated Clock and Clock Gated Memory. The result clearly shows that the power consumption of Clock Gated Memory is lower than the one without Gated Clock. Power is calculated using SPARTAN-3 XPE-11.1, power estimating tool from Xilinx.

Table 1: Comparison between Memory and Gated Memory

Name of Device	Number of Slices	Number of Slice Flip Flops	Number of 4 input LUTs	Execution Time (ns)	Power (W)
Memory	0	0	0	1.817	0.066
Gated Memory	1	1	2	1.881	0.059

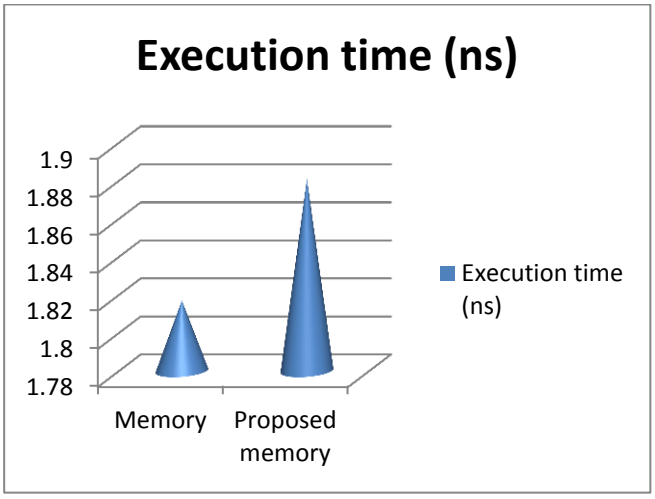

Figure 3: Graph shows comparison of memory and proposed memory in terms of time of execution in (ns)

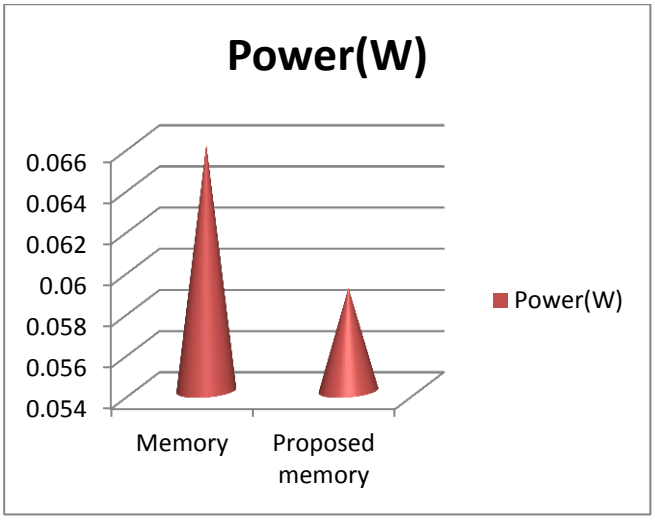

Figure 4: Graph shows comparison of Power (W) consumption of memory and proposed memory

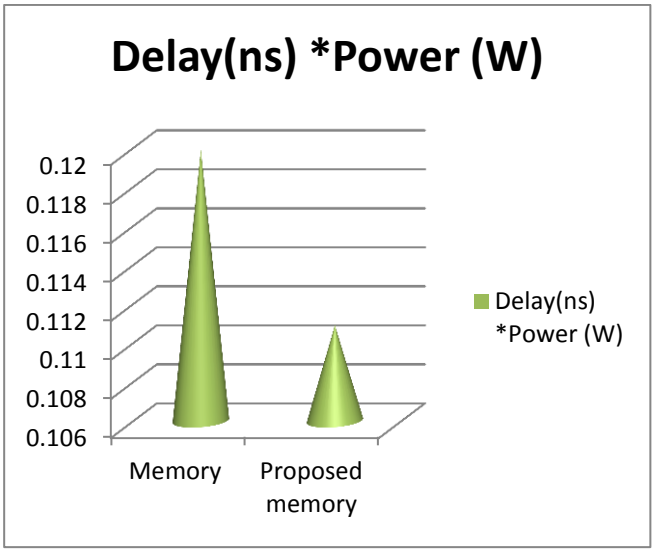

Figure 5: Graph shows comparison of overall performance of memory and proposed memory

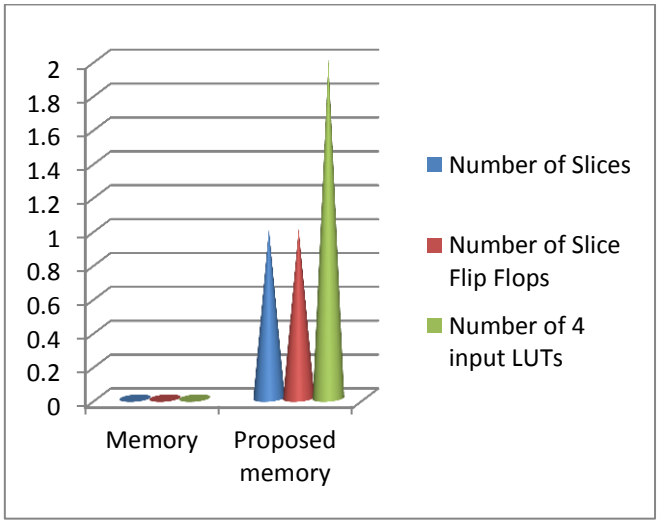

Figure 6: Graph shows comparison of circuit area of memory and proposed memory

From the above graphs we can clearly make out that overall power consumption of proposed memory is reduced than the previous one. The dynamic power consumed by clock gated memory is 10.60 % lesser than the one without clock gating.

In case of overall performance there is 7.506% of dynamic power reduction in clock gated memory.

V. CONCLUSION

The table shows the comparison between memory without clock gating and the memory after clock gating.

Though there is a increase in circuitry in case of gated clock memory due to added logic, and also the time of execution increases, still the overall product of delay (ns) and power (W) is reduced , which shows the improvement in results after implementation of clock gating. There is a power reduction of 7.506% in the circuit of memory with clock gating.

Table 2: Comparison of overall power consumption of memory with proposed memory

Name of Device	Execution Time (ns)	Power (W)	Delay(ns)*Power (W)
Memory	**1.817**	**0.066**	**0.119**
Gated Memory	**1.881**	**0.059**	**0.110**

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