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Design and Modeling of I2C Bus Controller Using Verilog

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***Abstract*— The name I2C stands for "Inter - Integrated Circuit Bus"It allows easy communication between components which reside on the same circuit board and to connect components which are linked via cable. It is a multi-master, multi-slave, single-ended, serial computer bus invented by Philips-Semiconductor in 1980's.It is used for attaching low-speed peripherals to computer motherboards and embedded systems. I2C enabled microcontrollers like PIC18F452 from Atmel and TMS470 from Texas Instruments require a lot of programming and knowledge of the register structures for configuring it. Hence they are not portable. We here present a model of I2C bus controller. The I2C controller is designed using verilog in xilink 11.1 and targeted in virtex 4 and virtex 5.**

***Index Terms*— I2C Bus , Master , Slave , Verilog, Finite State Machine.**

I. INTRODUCTION

The EEPROM, ADC and RTC will require an interface for communication between them. So I2C bus is used as an interface between them. It is used to minimize system-level interconnect. This simplifies the system level design and the design of the motherboard and associate chip-board.Moreover transmitting information over the I2C bus will improve system performance since the transmission of digital data is much less susceptible to interference from environmental noise sources.

II. I2C BUS SPECIFICATIONS

The I2C Controller Bus is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. I2C provides good support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resources master resource needs. It is a simple, low-bandwidth, short distance protocol.

I2C is easy to use to link multiple devices together since it has a built-in address [1][2].The two I2C signals are serial data (SDA) and serial Clock (SCL) as shown in Figure 1.The device that initiates a transaction on the I2C bus is termed the master. The master normally controls the clock signal. A device being addressed by the master is called a slave [1][2]. The I2C protocol supports multiple masters, but most system designs include only one. There may be one or more slaves on the bus. Both masters and slaves can receive and transmit data bytes. Standard I2C devices operate up to 100Kbps, while fast-mode devices operate at up to 400Kbps. Most of the I2C devices available today support 400Kbps operation. Higher speed operation may allow I2C to keep up with the rising demand for bandwidth in multimedia and other applications[2].

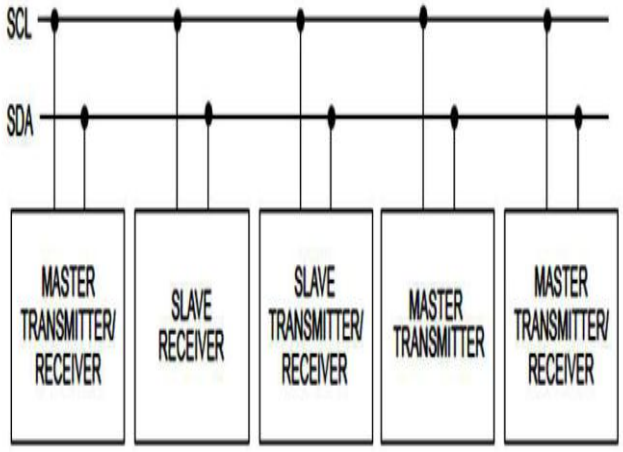

Fig. 1 I2C bus configuration using masters and slaves

III. I2C CHARACTERISTICS

The SDA and SCL lines are bi-directional lines connected to a positive voltage supply through a pull up resistor. The bus is free when these lines are 'high'. The data on the SDA line is valid only when the SCL line is 'high'. Change of data is allowed when SCL line becomes 'low'. During data transfer, the master generates the START and STOP conditions, which are unique conditions and are shown in Figure[2].

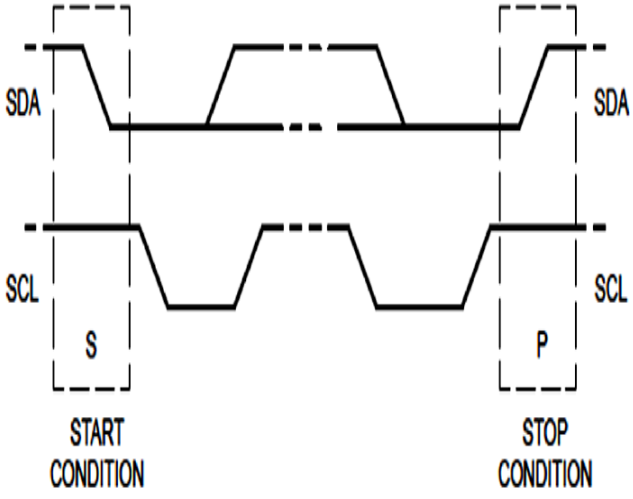

Fig. 3 Data transfer on the I2C bus

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IV. I2C BUS CONTROLLER DESIGN

I2C protocol consists of four parts 1) START signal generation,2) Slave address transfer,3) Data transfer,4) STOP signal generation[12].

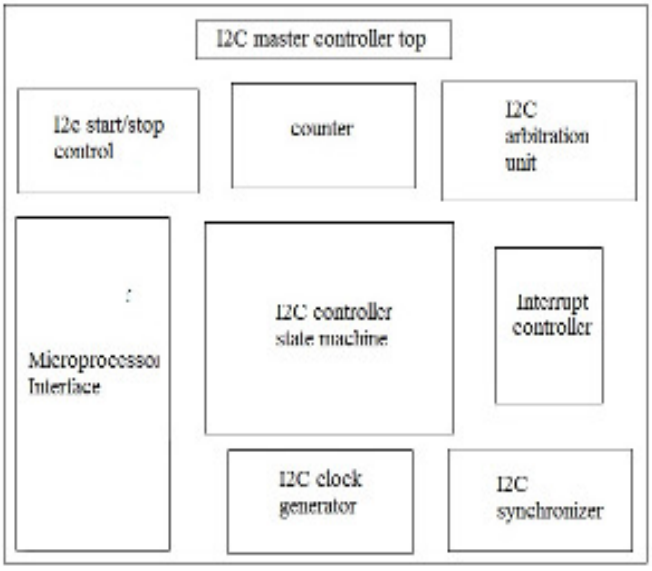

Fig. 4 The I2C Master Controller Block Diagram

V. I2C BUS ARCHITECTURE

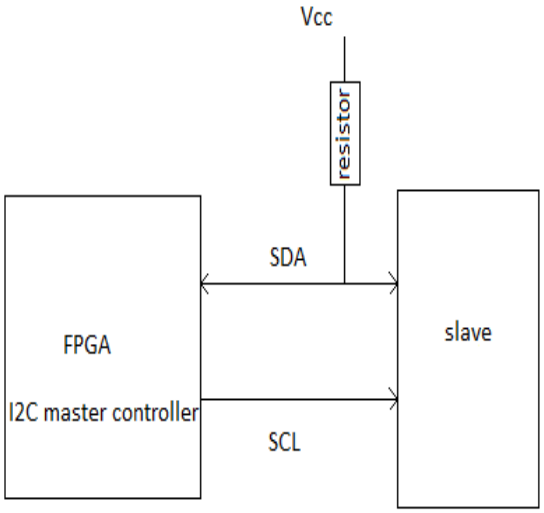

Fig. 5.1 I2C bus architecture

It consists of a master and a slave connected using I2C bus. The SDA line is connected to a positive supply voltage through a pull up resistor. The SCL line is not connected to a pull up resistor as there is only one master.

Designing the I2C master controller

For designing the I2C master controller is to use a finite state machine (FSM). We can easily implement finite state machine by writing VHDL or verilog code [15].

Finite State machine

A finite state machine is a sequential circuit that uses a finite number of states to keep track of its history of operations, and based on this history and its current inputs, determine what to do next.

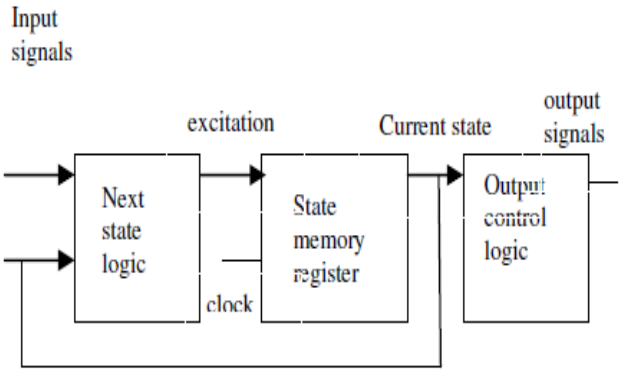

Figure 5.2 Block diagram of finite state machine

A sequential circuit is one where its outputs are dependent on its history of operation and its current inputs

VI. RESULT ANALYSIS

Here the I2C bus controller is designed using verilog and implemented in virtex 4 xc4vlx15-12sf363 using xilink 11.1.The device utilization summary is given below:

Device utilization summary (virtex 4)			
Logic utilization	Used	Available	Utilization
Number of slice	44	6144	0%
Number of slice filpflop	52	12288	0%
Number of 4 input LUTS	81	12288	0%
Number of bonded IOBs	18	240	7%
Number Of GCLKS	1	32	3%

Here the I2C bus controller is designed using verilog and implemented in virtex 5 xc4vlx15-12sf363 using xilink 11.1. The device utilization summary is given below:

Device utilization summary (virtex 4)			
Logic utilization	Used	Available	Utilization
Number of slice	52	19200	0%
Number of slice filpflop	63	19200	0%
Number of 4 input LUTS	46	69	66%
Number of bonded IOBs	18	220	8%
Number Of GCLKS	1	32	3%

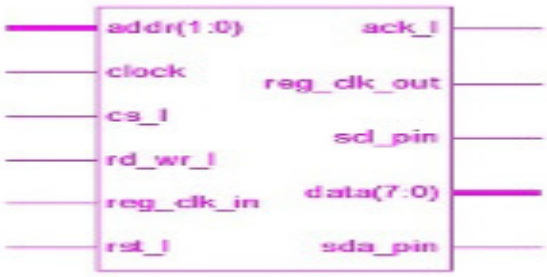

Figure 6.1 RTL view

VII. CONCLUSION

The result shows that minimal resources are utilized in virtex 4. The design process is simplified using verilog HDL to design the I2C bus controller. The designer can write his design description without choosing any specific fabrication technology. If a new technology emerges, designers do not need to redesign the circuit. He simply input the design program to the logic synthesis tool and creates a new gate level netlist using the new fabrication technology. The logic synthesis tool will optimize the circuit in area and timing for the new technology.

REFERENCES:

[1] The I2C Bus specifications version 2.1 January 2000
[2] UM10204 I2C -bus specification and user manual Rev. 4 — 13 February 2012
[3] I2C bus Inter Integrated Circuits bus by Philips Semiconductors
[4] Embedded Platform Excalibur Altera, http://www.altera.com
[5]PCF 8584, I2C bus controller datasheet, http://www.semiconductor.philips.com
[6] Muhammed Ali Mazidi, Janice Gillispie Mazidi & Rolin D. Mckinlay,The 8051 Microcontroller and Embedded Systems, using Assembly and C , second Edition, Pearson Education.
[7] Samir Palnitkar, Verilog HDL, second Edition
[8] SAA1064, 4-digit Led-driver with I2C bus interface datasheet, http://www.semicondutors.philips.com
[9] IEEE Computer Society. IEEE Standard Verilog® Hardware Description Language, IEEE Std 1364- 2001, The Institute of Electrical and Electronics Engineers, Inc, 28 September 2001
[10] R. Herveille. I2C-Master Core Specification, Rev. 0.9, 2003.7
[11]http://www.engineersgarage.com/microcontroller/ 8051projects/interfaceserial-eeprom-24c02-T89C51- circuit.
[12] Arvind Sahu,Ravi Shankar Mishra,Puran Gour , Design and Interfacing of High speed model of FPGA using I2C protocol, , Int. J. Comp. Tech. Appl., Vol 2 (3), 531-536
[13] P.Venkateswaran, Madhumita Mukherjee, Arindam Sanyal, Snehasish Das and R.Nandi, Design and Implementation of FPGA Based Interface Model for Scale-Free Network using I2C Bus Protocol on Quartus II 6.0
[14] http://en.wikipedia.org/wiki/I2C
[15] A Novel Architecture of I2C Slave using One- Hot Encoding Technique, Devashree Mahato, Sulipta Das, Durga Prasad Dash
[16] A.R.M. Khan, A.P.Thakare, A.R.M. Khan, FPGA based design and implementation of serial data transmission controller, et. al. / International Journal of Engineering Science and Technology Vol. 2(10), 2010, 5526-5533
[17] Prof. Jai Karan Singh, Design and Implementation of I2C master controller on FPGA using VHDL, et al. / International Journal of Engineering and Technology (IJET), Vol 4 No 4 Aug- Sep 2012
[18] A Novel Opto-isolation Technique for the I2C Bus for Glitch Elimination in an Industrial Environment, review paper, International Journal of Recent Trends in Engineering, Vol 2, No. 8, November 2009
[19] Arvind Sahu, An Implementation of I2C using VHDL for DATA surveillance, et al. / International Journal on Computer Science and Engineering (IJCSE)
[20] M.Jyothi, L.Ravi Chandra, M.Sahithi, S.Daya Sagar Chowdary, K.Rajasekhar, K.Purnima, Implementation of SPI Communication Protocol for Multipurpose Applications with I2C Power and Area Reduction, International Journal of Engineering Research and Applications (IJERA) , Vol. 2, Issue 2, Mar-Apr 2012, pp.875-883
[21] O. Romain, T.Cuenin & P.Garda:"*Design and verification of mixed-signal I/O IPS: an I2C Bus Controller*". ISBN0:78 0383040.
[22] O. Romain, T.Cuenin & P.Garda: *"Design & modeling of an I2c Bus Controller*", FDL 0'3, Frankfurt, Deutschland, Sept 23-26,2003.
[23] Feng Lin, Haili Wang, Jinian Bian:" HW/SW Interface Synthesis based on Avalon Bus Specification for Nios-oriented SoC Design" 2005 IEEE.
[24] IEEE Computer Society. IEEE Standard Verilog® HD Language, IEEE Std 1364-2001, The Institute of Electrical and Electronics Engineers, Inc,28 September 2001.
[25] Philips Semiconductors: I2C Controller datasheet,http://www.semiconductors.philips.com/acrobat/datasheets/PCF8584_4.