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Implementation Of Selective Harmonic Reduction Approach for Series Cascaded H-bridge Converters Fed By Unequal DC Voltages

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***Abstract*—The problem of harmonics existing in multilevel converters has been tackled in past by various techniques. Optimized PWM techniques for reduction of harmonics have been successful for cascaded H-bridge fed from equal voltages however, this paper presents Selective Harmonic Mitigation technique implemented on series connected cascaded H-bridge converter working on equal as well as unequal voltages. The presented technique is capable of reducing selective harmonics, to an extend acceptable by grid codes, even when converter is fed from unequal voltages. The bulky and costly grid connected tuned filters of power system can be avoided and reduced by implementation of Harmonic Mitigation Techniques. The simulation results are being presented to validate the proposed method.**

***Index Terms*—Harmonic distortion, Multilevel systems, Optimization technique, Pulse width modulation converters.**

I. INTRODUCTION

The Cascaded H-bridge converter topology presented in this paper enables the converter to produce high quality, high voltages waveforms by making use of the low or medium voltage switching devices. It also makes the converter an attractive option for grid connected applications. But the converter working at high power levels generally requires low switching frequency, this is due to the imperfect behavior of the switching devices which reduces the efficiency gets effected hence this results in distorted output[1].Also for such Cascaded H-bridge (CHB) inverter applications, it may be desired that each cell of the converter draws equal energy from the dc source that it is connected to. Though this can be achieved over a single or several fundamental cycles. But it ensures that these sources discharge at the same rate and that each cell of the cascade is utilized evenly.

In applications where the dc sources are not exactly equal, distortion may be present in the converter waveformSelective Harmonic Mitigation – Pulse Width Modulation (SHM-PWM) orSelective HarmonicElimination –Pulse Width Modulation (SHE-PWM) are the methods known to generate waveforms with low switching frequency without making a compromise with the waveforms quality. The waveforms objective includes reduction of particular harmonics in the generated waveform or an optimization of this waveform in order to meet a certain harmonic code for a particular application[2].

Several three-level power cells, formed using full H-bridges, can be series connected to build a converter with a higher number of levels. In general, if npower cells are connected in series to build the converter and all the cells have the same dc voltage, the number of levels that can be achieved is 2n + 1. This topology is named the n-cell CHB converter, and it presents a high level of modularity and redundancy as well as an ability to produce high quality output voltage waveforms [3].

A Cascaded H-bridge converter fed from two unequal dc sources' V_A and V_B has been shown in fig .1. [1]. The SHM-PWM implemented in this paper is based on the dynamic calculation of the switching angles for unequal voltages.

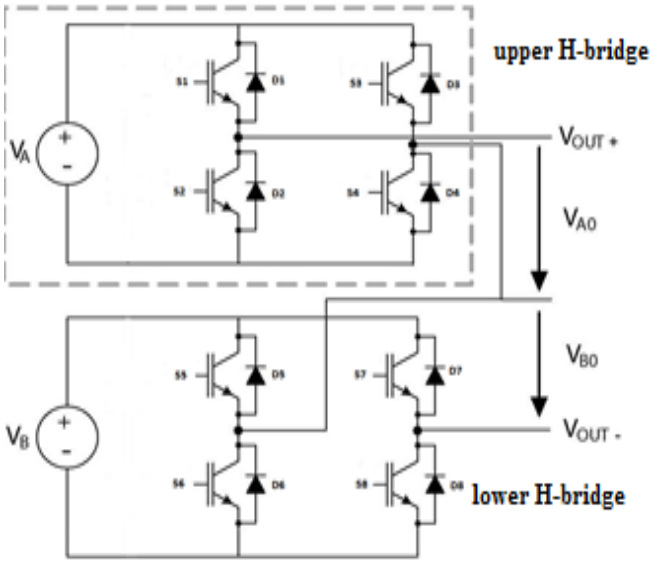

Fig.1. Five- level cascaded H-bridge converter based on the series connection of the two Three- level power cells

II. SHM-PWM PRINCIPLE

The basic principle of SHM reveals that calculating the values of the switching angles according to input DC voltages. The amplitude of fundamental harmonic can be set and hence set of specific harmonics can be cancelled.

Consider the Fourier analysis of a typical waveform shown in Fig.2. With switching angles αi (i = o . . . k − 1)[4]

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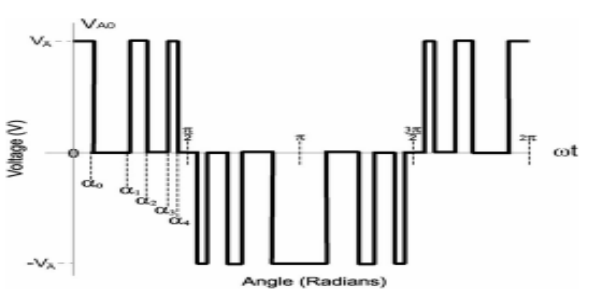

Fig.2. PWM switching pattern with four switching angles.[1].

The amplitude of each harmonic in the figure can be obtained using the following equation where H_J is the amplitude of the J^{th} harmonic [5].

$$H_J = \frac{4}{j\pi}\sum_{i=0}^{k-1}\left[(-1)^i \sin(j\alpha_i)\right] \quad \rightarrow \quad (1)$$

From the use of the above expression we can set a specific value for each harmonic amplitude by making use of switchingangle as the degree of freedom, and hence cancel a set of specific harmonics. The relationship between the dc link voltage of the converter and the amplitude of the generated fundamental component is called the modulation index (Ma) and can be defined as Ma = H1π/4Vdc.

Hence from this calculation of modulation index, we get the value of the particular harmonics, this value is further used for the calculation of the switching angles, applied to the switching device. Even harmonics in such waveforms are cancelled due to symmetric nature of waveform[6] [7].

The presented SHM-PWM technique is very versatile and flexible because it can be applied to any H-bridge circuits operating at unequal voltages, As for any circuits we need to make a simple modification in mathematical description used to obtained the switching angles. By the use of the SHM-PWM technique all the harmonic levels are kept under consideration below the max level imposed by the applied grid code in all the modulation index range. The presented technique has beenformulated with the following system of inequalities [8-9], where Ma is the modulation index and l_j is the maximum limit of j_{th} harmonic.

$$E_{1} = |\text{Ma-H1}| \leq L_1 \quad \rightarrow \quad (2)$$

$$E_j = \frac{1}{|H1|}\frac{4}{j\pi}\sum_{1=0}^{k-1}[(-1)^i \sin(j_{\alpha i})] \quad \rightarrow \quad (3)$$

The equations (2) & (3) can be arranged into an objective function in order to use an optimization method to minimize it. The obtained objective function explained is given in eqn (4) &eqn (5).

$$M_{a=\frac{H\pi}{4vdc}} \quad \rightarrow \quad (4)$$

$$H_{J=\frac{4}{J\pi}}(V_1 \sin(\alpha_0)+\sum_{I=1}^{K-1}[V_1[\sin(J\alpha_i)-\sin(j_{\alpha i-1})]]) \quad \rightarrow (5)$$

OF $(\alpha_0 \ldots\ldots\ldots\alpha_{k-1})=\sum_{i=1,3,5,\ldots\ldots 49} c_{iE_i^2} + C_{thd}$THD → (6)

thec_i coefficients are modeled as non- linear functions.

This SHM principle can be extended to any higher number of voltage levels

Consider a waveform similar to the pattern shown in Fig .3, which shows ten switching angles

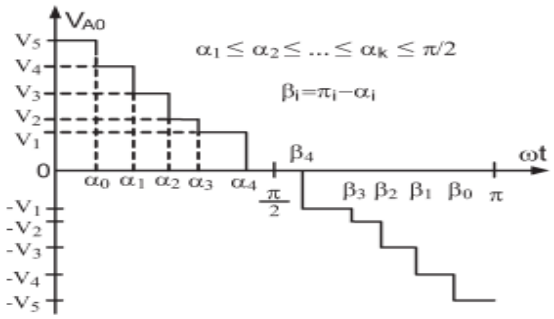

Fig 3. Nine–level PWM switching pattern with ten switching angles. [1].

It can be seen that as the waveform is symmetrical the even harmonics will be eliminated. For N levels, and K switching angles α_i(i= 0,1 ,2 ……..k-1) the Fourier analysis of the waveform is given in equation (7)

$$H_{J=\frac{4}{J\pi}}[\sin\alpha_0 - \sin\alpha_1 + \sin\alpha_2 - \cdots + (-1)^n \sin\alpha_n] \quad \rightarrow \quad (7)$$

III. OPERATION OF THE CONVERTER

The gating circuitry for switching devicesof upper H-bridgeshown in Fig.1,is shown Fig .4. Here the sine wave signal is compared with the repeating sequence and resultant output is obtained as designed in relational operator.The output PWM pulse obtained from Static Switching Angles are given to the switching devices of upper H-bridge cell for all the cases.

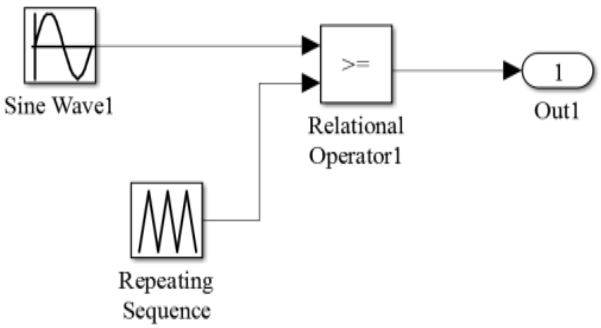

Fig.4. Gating Circuitry for switching Devices of the upper H-Bridge of the Converter. [1].

Fig.5. shows the generation of the pulse width modulated (PWM) signal is obtained from the comparator, where the sinusoidal signal is compared with the output of the logical operator block. Here the input to the logical operator block is the switching angles which are calculated using the equation (4) and equation(5).

The output of the comparator goes high when the output of the logical operator is greater than the sinusoidal wave .The generated output pulses is given to the lower H-bridge for R

load and RL Load both operating under unequal voltages where SHM technique is applied. [10]

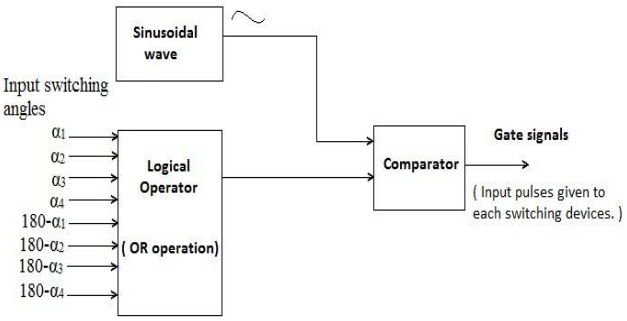

Fig.5. Generation of the pulses as per the SHM.

The presented converter has been operated to obtain 5 voltage levels as shown in Table.1.The switching states are combination of eight switches S1…S7 along with diodes D1…..D8.These switching states generate 5 voltage levels.

Table.1.The switching states conditions and corresponding output voltage levels for the converter

Voltage levels ↓	S1	S2	S3	S4	S5	S6	S7	S8
0	-	-	-	-	-	-	-	-
V_{AB}	ON	ON	-	-	-	ON	-	-
$2V_{AB}$	ON	ON	-	-	ON	ON	-	-
$-V_{AB}$	-	-	ON	ON	-	-	ON	-
$-2V_{AB}$	-	-	ON	ON	-	-	ON	ON
0	-	-	-	-	-	-	-	-

IV. IMPLEMENTATION OF SHM-PWM TO OBTAIN VARIOUS SWITCHING ANGLES.

For the look up table presented in Table.1, values of Switching Angles are first calculated, when CHB is fed from equal voltages.Usingequation (4) and equations (5), using the same switching angles the output waveforms are analyzed when equal voltages to CHB become unequal. Keeping in the view that value of the THD obtained increases in this case, the proposed technique encourages dynamic calculation of Switching Angles for the CHB fed from unequal voltages using equation (4) and equations (5).

The sample values of switching angles thus obtained are as follows

α_1=13.493 α_2=8.042 $\alpha_{3=}$5.73917 $\alpha_{4=}$4.4608

Values for the unequal voltages V_A=150 V and V_B=250V the sample of switching angles of the corresponding switches S5, S6, S7, S8, are follows

α_1=23.1936 α_2=13.1975 $\alpha_{3=}$9.8514 $\alpha_{4=}$7.662

V. SIMULATION DIAGRAM AND RESULTS.

The cascaded H-bridge converter under SHM-PWM technique has been simulated in MATLAB/SIMULINK as shown in Fig.6.The Simulink model has been analyzed for the conditions when both the converters are fed from equal dc link voltages and when the input dc voltages become unequal The various values of the switching angles for equal and unequal voltages are shown in Table II

Study of R load and RL load for different cases has been shown.

5.1 FOR R LOAD (R=360Ω)

CASE1 (for unequal input voltages and Static Switching Angles)

Table II. Shows the various values of Static and Dynamic Switching Angles for equal and unequal voltages.

Switching angles	SA for equal voltages	Static SA for unequal voltages	Dynamic SA for unequal voltages
α_1	13.493	13.493	23.1936
α_2	8.042	8.042	13.1975
α_3	5.73917	5.73917	9.8514
α_4	4.4608	4.4608	7.6622

The switching angles shown in the above table are derived using the equations (4) and (5).the first column shows the switching angles when the tow voltages are equal, whereas the second column presents the switching angles for unequal voltages in the static state. Similarly third column shows the dynamically calculated switching angles

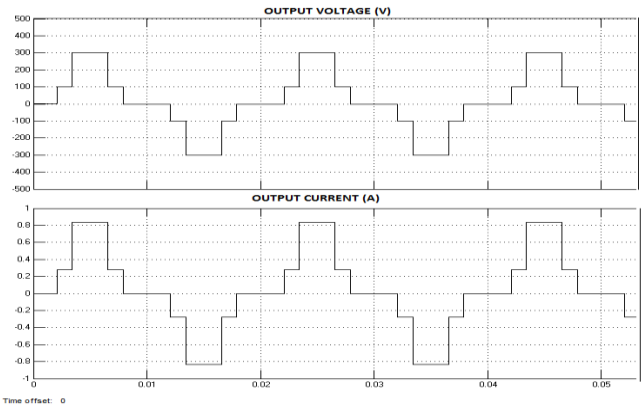

Fig.8. Output voltage and current waveforms for Static switching angles

In the above graph maximum output voltage is 300 V and the minimum output voltage is -300V.the average output current value is 0.8 A.

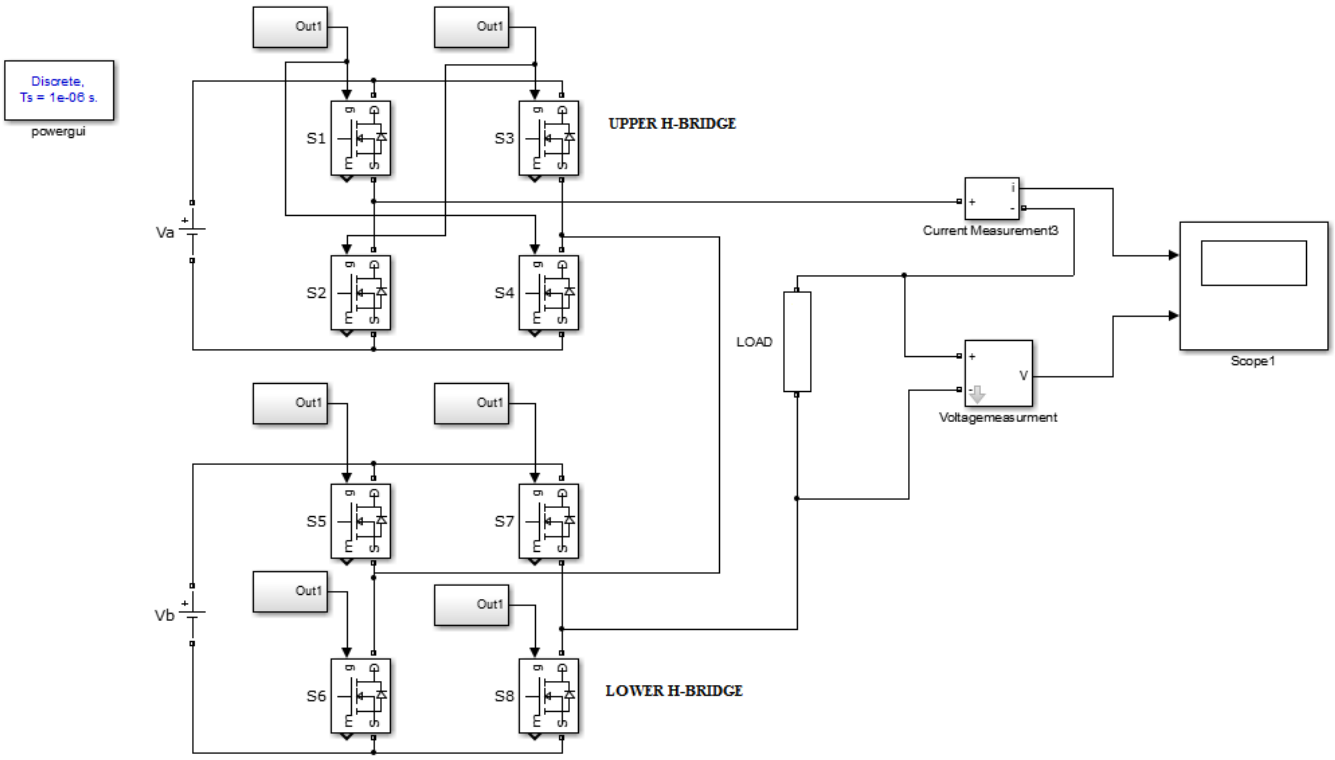

Fig.6. Simulation diagram of the five-level converter

CASE 2 (for unequal voltages and Dynamic Switching Angles)

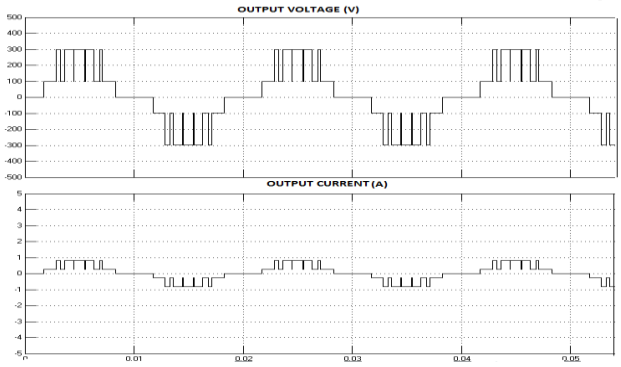

Fig .9.Output voltage and output current waveforms for recalculated Switching angles

By making use the dynamically calculated Switching Angles operating under unequal voltages, the duty cycles of the switching devices is varied and hence by this variation in the duty cycle the required Harmonic Mitigation is being obtained.

Table III shows the value of THD obtained in the respectivecase. It can be seen that switching angles needs to be recalculated dynamically to keep the THD to a acceptable level when input DC voltages becomes unequal.

THD for R Load

TABLE III& Table V. Gives the variation of the THD value for different voltage conditions and also the static and dynamic switching angles

Table .III.

Different cases→	SA for equal voltages	Static SA for unequal voltages	Dynamic SA for unequal voltages
THD values in percentage	38.09	27.82	25.52

5.1.2 FOR RL LOAD (R=360Ω & L=15MH)

TABLE IV.Shows the various values of Static and Dynamic Switching Angles for equal and unequal voltages

Switching angles	SA for equal voltages	Static SA for unequal voltages	Dynamic SA for unequal voltages
α_1	13.493	13.493	23.1936
α_2	8.042	8.042	13.1975
α_3	5.73917	5.73917	9.8514
α_4	4.4608	4.4608	7.6622

The switching angles shown in the above table are derived using the equations (4) and (5).the first column shows the switching angles when the tow voltages are equal, whereas the

second column presents the switching angles for unequal voltages in the static state. Similarly third column shows the dynamically calculated switching angles

CASE3(for unequal voltages and Static Switching Angles)

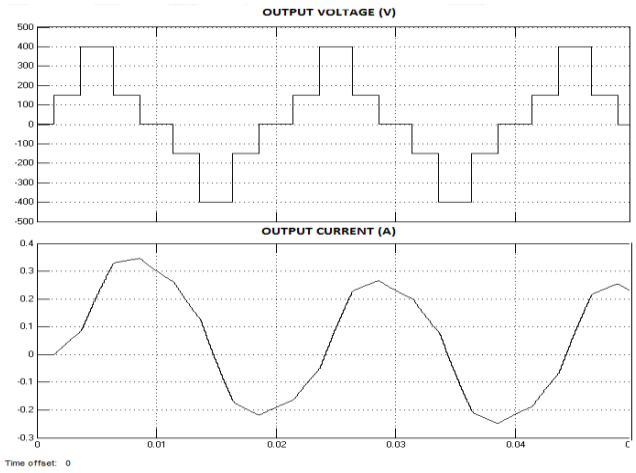

Fig .10. output voltage and current waveformsfor Static switching angles

In the above Fig.10. Maximum output voltage is 400 V and the minimum output voltage is -400V.the average output current value is 0.35 A

CASE4 (for unequal voltages and Dynamic Switching Angles)

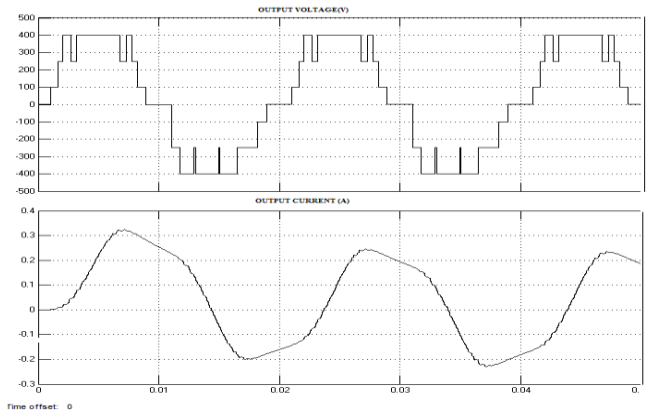

Fig .11.Output voltage and current waveforms for recalculated Switching angles

By making use the dynamically calculated Switching Angles operating under unequal voltages, the duty cycles of the switching devices is varied and hence by this variation in the duty cycle the required Harmonic Mitigation is being obtained. The maximum output voltage 400 V and the minimum -400 V. the average output current is 0.35 A.

TABLE V

Different Cases→	SA For Equal Voltages	Static SA For Unequal Voltages	Dynamic SA For Unequal Voltages
THD values in percentage	60.16	47.82	27.84

VI. CONCLUSION

This paper presents a control strategy based on the SHM-PWM technique, for cascaded H-bridge Converters fed from unequal voltage levels. The technique reveals that dynamic calculation of switching angles is required for significant reduction in Total Harmonic Distortion (THD) when the input voltages feeding a cascaded H-bridge becomes unequal.

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