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Design and Analysis of Low Power 2-bit and 4-bit Digital Comparators in 45nm and 90nm CMOS Technologies

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***Abstract*— Digital Comparator is an important part of ALU for comparison operations. With the miniaturization of technology, it becomes essential for any device to be power efficient. In the research work, a 4-bit Digital Comparator is designed using 2-bit comparator modules[22] with CMOS and low power design techniques viz. AVL, GDI, GDIAVL [2],[7],[9] and the best performing circuit is presented. Then two application of a 4-bit digital comparator are presented to justify the performance of the low power yielding comparator designs. The implementation is done on DSCH 3.5 and simulation on Microwind 3.5 tool on 45nm and 90nm technology. Comparison between different designs is made in terms of the parameters such as power consumption, leakage current, surface area etc.[4]**

***Index Terms*—AVL, Digital Comparator, GDIAVL, Low Power, Microwind 3.5, VLSI**

I. INTRODUCTION

A. Digital Comparator

A digital/magnitude comparator is a logic circuit that is used to compare the magnitude of two binary numbers say A and B. The result of the comparison is specified by three binary variables that indicate whether A<B, A=B or A>B. The XNOR gate (coincidence gate) is a basic comparator because its output is a 1 only if its two input bits are equal [22].

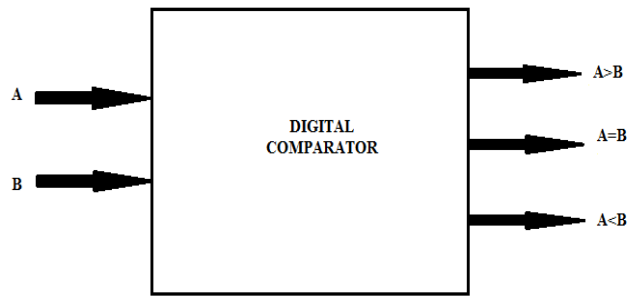

Fig.1 Block Diagram of a Digital Comparator

B. 2-bit Digital Comparator

Configuration 1: By Definition

It compares two 2-bit binary numbers A (A1A0) and B (B1B0). The circuit diagram and truth table of a 2-bit Magnitude Comparator are as shown below:

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Outputs are defined as:
Greater (A>B): $\overline{A1}B1+\overline{A0}B0$ (A1 Θ B1)
Lesser (A<B): $\overline{A1}B1+\overline{A0}B0$ (A1 Θ B1)
Equal (A=B): (A1 Θ B1) (A0 Θ B0)

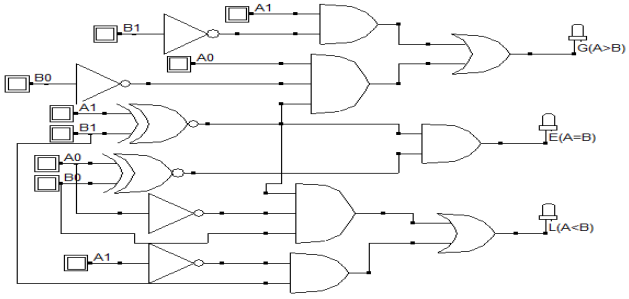

Fig.2 Circuit Diagram of a 2-bit Digital Comparator (Configuration 1)

A 2-bit Digital Comparator can be alternatively designed with the following method.

Configuration 2: Using 1-bit Digital Comparator Modules

A 2- bit Digital Comparator can be designed with two 1- bit comparators each one comparing corresponding bits of both the numbers . [22]

If A (A1A0) and B (B1B0) are two numbers, then G (A>B) if A1 >B1 or A1=B1 and A0>B1.

Thus, G (A>B) =G1+E1.G0,

L (A<B) =L1+E1.L0, and, E (A=B) =E1.E0 where

G1 (A1>B1): A1B1bar,

L1 (A1<B1): A1barB1,

E1 (A1=B1): (A1ΘB1)

Similarly the expressions can be written for A0, B0.

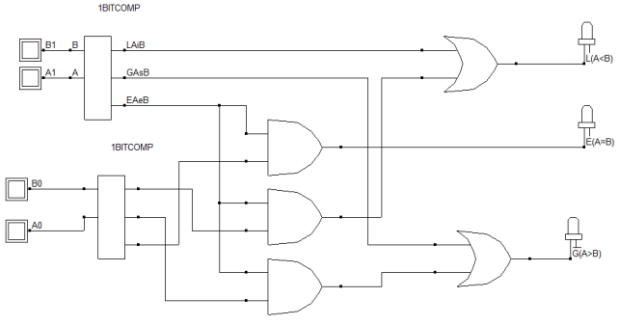

Fig.3 Circuit Diagram of a 2 bit-comparator using two 1-bit modules (Configuration 2)

C. 4-bit Digital Comparator

A 4-bit digital comparator compares two 4-bit numbers viz.

A i.e. (A3A2A1A0) and B i.e. (B3B2B1B0). The circuit has been designed with three 2-bit digital comparator. The circuit diagram of the same is as shown below:

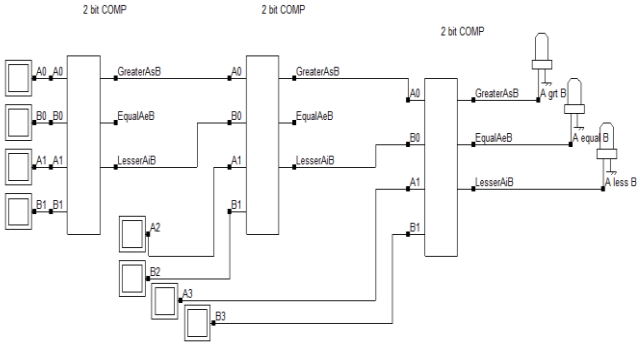

Fig.4 Circuit Diagram of a 4-bit Digital Comparator using 2-bit digital comparator

D. Low Power Techniques

It is essential for any circuit design to consume least power because battery life for portable devices is limited. Some of the techniques taken in this paper are AVL, GDI, and a proposed technique called GDIAVL.CMOS technique is taken as the base case for comparison of results with the other techniques.

1. Conventional CMOS Technique

In this well-known technique, a circuit consists of two networks: NMOS pull-down network to connect the output to '0' (GND) and PMOS pull-up network to connect the output to '1' (Vdd).

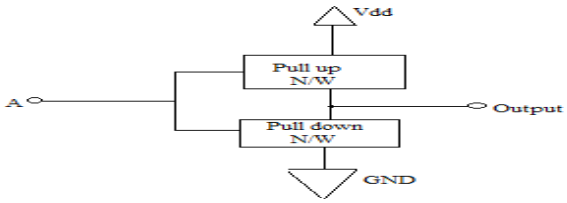

Fig.5 Conventional CMOS Circuit

2. GDI (Gate Diffusion Input) Technique

GDI (or Gate Diffusion Input) is technique based on a simple concept of a cell as shown in Fig. 6. A GDI cell consists of 3 inputs: G (common gate input of PMOS and NMOS), P (input to the source/drain of PMOS), N (input to the source/drain of NMOS) [2]

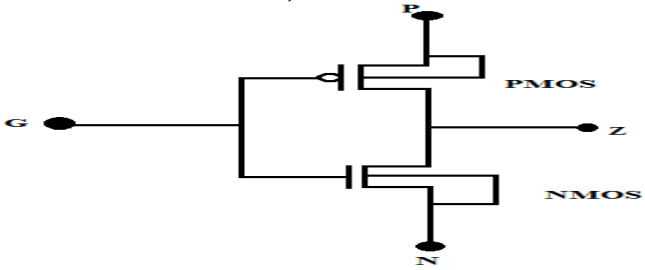

Fig.6 Basic GDI Cell

Table1. GDI Logic Functions

S.No.	P	N	G	Z	Description
1.	'0'	B	A	AB	AND
2.	B	'1'	A	A+B	OR
3.	'1'	'0'	A	Abar	NOT
4.	'1'	B	A	Abar+B	Function 1
5.	B	'0'	A	AbarB	Function 2
6.	B	C	A	AbarB+AC	MUX

3. AVL (Adaptive Voltage Level) Technique

An adaptive voltage level technique as described in [7], [12], [13], [15] is a power gated technique that is fit in the pull down and pull up networks between power rails. It is comprised of AVLG and AVLS schemes.

3.1 AVLG Technique

In this power gated technique, two PMOS transistors and one NMOS transistor are connected in parallel. This circuit combination is fixed between pull down network and GND potential. A sleep signal with alternate states (0 or 1) or a clock is connected to the NMOS transistor. As the PMOS transistors are held in forward biased state, they are always ON. But NMOS transistor is switched between states hence is alternately ON and OFF. The circuit works normally in the active mode since NMOS is ON and is offering low resistance. When the NMOS transistor is OFF i.e. when the circuit is in standby mode, PMOS transistors degrade the ground potential, thus leakage current flowing through NMOS of AVLG circuit is reduced and hence the power consumption is also reduced.

3.1 AVLS Technique

In this power gated technique, two NMOS transistors and one PMOS transistor are connected in parallel. This circuit combination is fixed between pull up network and Vdd potential. A sleep signal with alternate states (0 or 1) or a clock is connected to the PMOS transistor. As the NMOS transistors are held in forward biased state, they are always ON. But PMOS transistor is switched between states hence is alternately ON and OFF. The circuit works normally in the active mode since PMOS is ON and is offering low resistance. When the PMOS transistor is OFF i.e. when the circuit is in standby mode, NMOS transistors degrade the supply node potential, thus leakage current flowing through PMOS of AVLS circuit is reduced and hence the power consumption is also reduced.

The combination of AVLS and AVLG technique is called AVL technique.

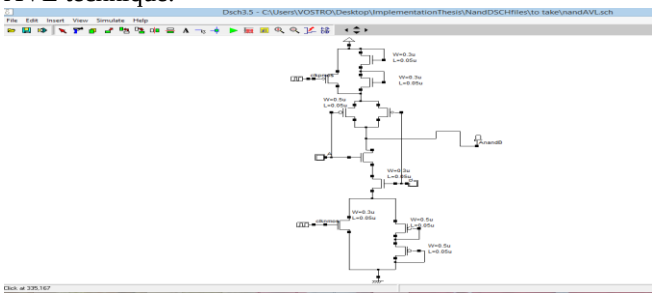

Fig.7 Schematic of NAND gate using AVL Technique

4. GDIAVL Technique

A combination of GDI +AVL i.e. applying the AVL circuit on a GDI circuit design rather than on CMOS circuit design

gives rise to a new technique called GDIAVL, is proposed that gives appreciable power reduction.

II. 2-BIT DIGITAL COMPARATOR

A. *Transistor Implementation*

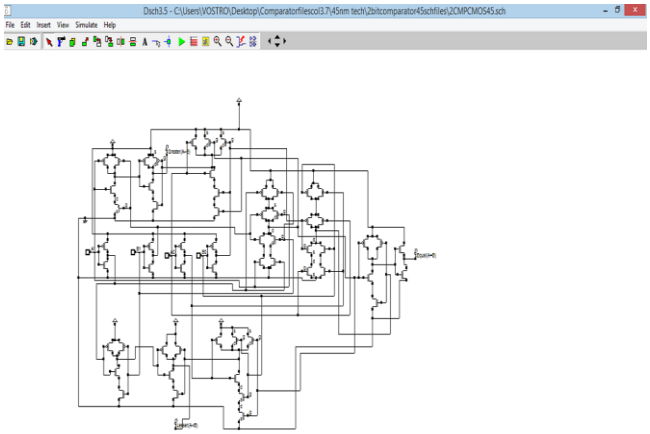

Fig.8 Schematic of 2-bit Comparator (Configuration 1) in 45nm using CMOS Technique

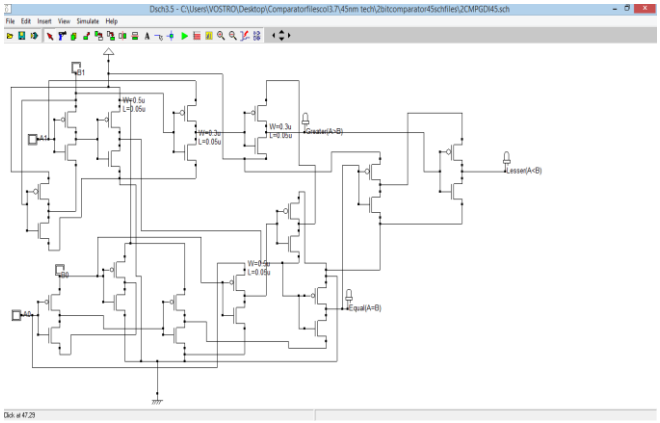

Fig.9 Schematic of 2-bit comparator (Configuration 1) in 45nm using GDI Technique

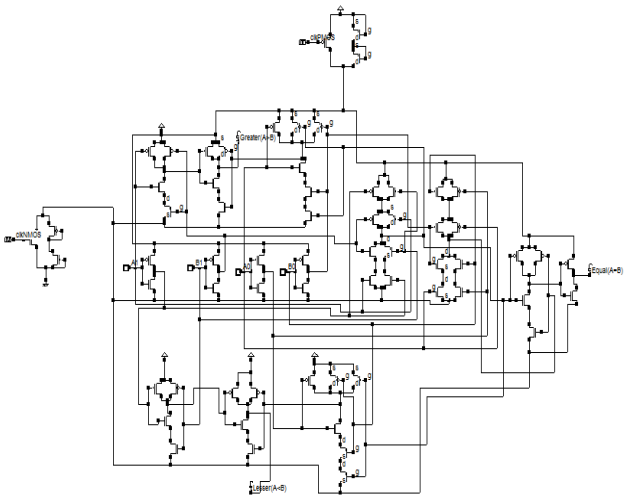

Fig.10 Schematic of 2-bit Comparator (Configuration 1) in 45nm using AVL Technique

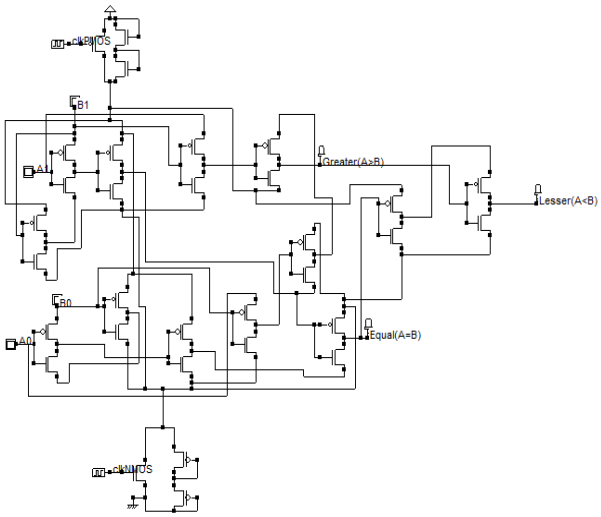

Fig.11 Schematic of 2-bit comparator (Configuration 1) in 45nm using GDIAVL Technique

The schematics are designed for both configuration 1 and 2 of the 2-bit magnitude comparator on both 45nm and 90nm technologies in DSCH 3.5 of Microwind tool.

B. *Layout*

Layout for each design is generated when the VERILOG file generated for the respective design in DSCH 3.5 is compiled in Microwind 3.5 tool.

As an example, the layout for 2-bit comparator designed in Configuration 1 with CMOS technique in 45nm technology is shown below:

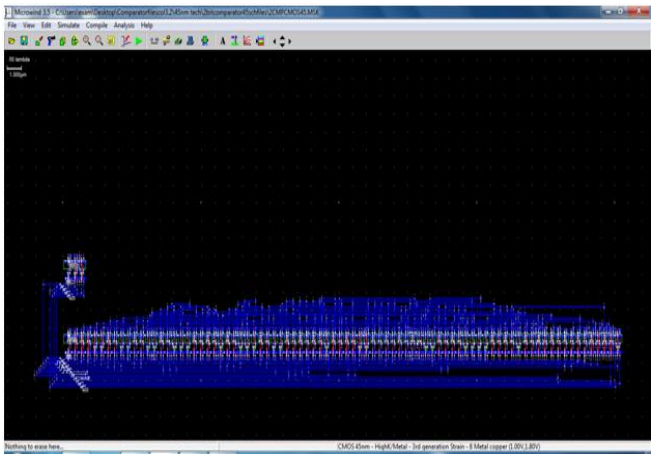

Fig.12 Layout of 2-bit Comparator (Configuration 1) in 45nm using CMOS Technique

III. 4-BIT DIGITAL COMPARATOR

A. *Transistor Implementation*

The schematics for all circuits are designed for both configurations 1 and 2 of 2-bit comparator modules used in the 4-bit magnitude comparator on both 45nm and 90nm technologies in DSCH 3.5 of Microwind tool.

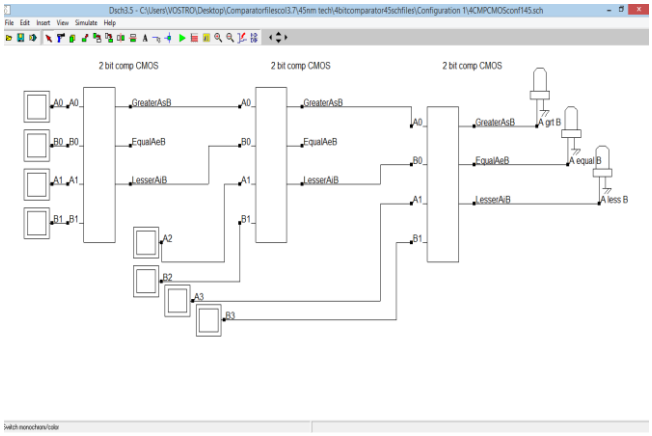

Fig.13 Schematic of 4-bit comparator (Configuration 2) in 45nm using CMOS Technique

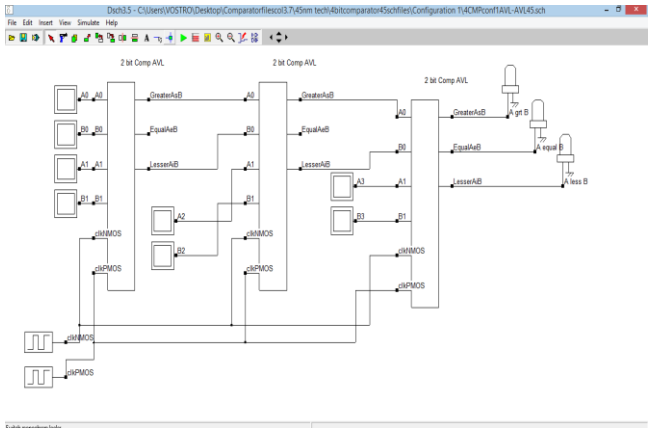

Fig.14 Schematic of 4-bit comparator (Configuration 2) in 45nm using AVL Technique

B. *Layout*

Layout for each design is generated when the VERILOG file generated for the respective design in DSCH 3.5 is compiled in Microwind 3.5 tool.

As an example, the layout for 4-bit comparator designed with 2-bit comparator modules in Configuration 2 with AVL technique in 45nm technology is shown below:

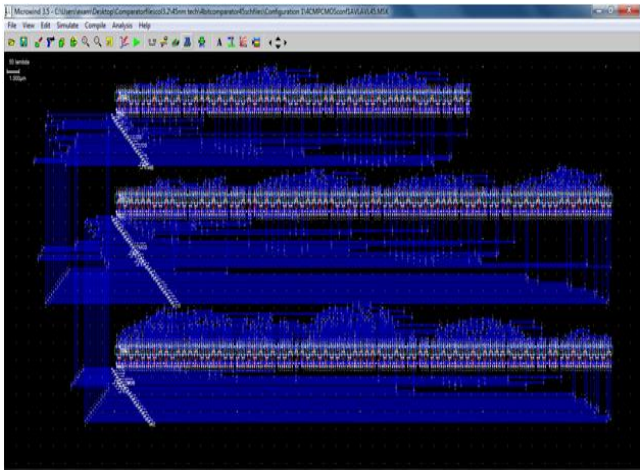

Fig. 15 Layout of 4-bit comparator (Configuration 2) in 45nm using AVL Technique

IV. Simulation Results

A. *Conventional CMOS 2 bit Comparator*

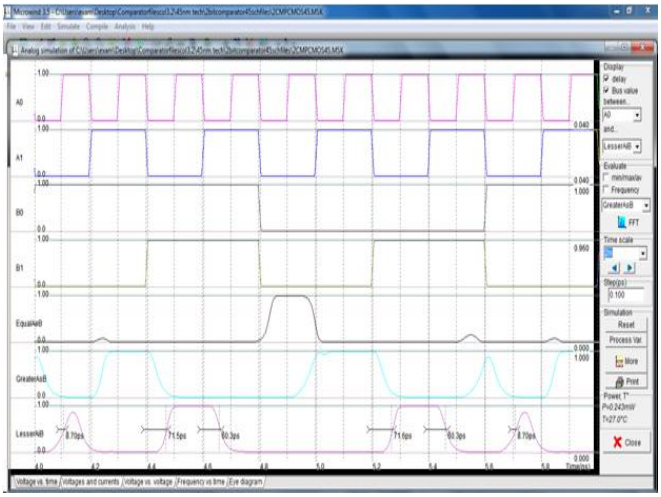

Fig.16 Post-Layout Simulation (Voltage vs. Time) of 2-bit comparator (Configuration 1) in 45nm using CMOS Technique

B. *2-bit Comparator using AVL Technique*

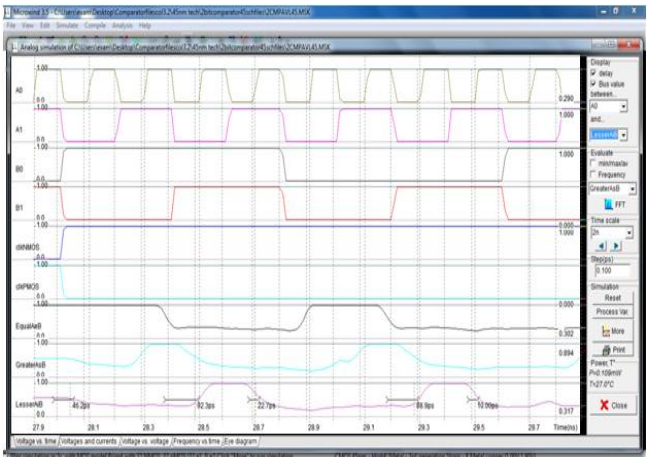

Fig.17 Post-Layout Simulation (Voltage vs. Time) of 2-bit comparator (Configuration 1) in 45nm using AVL Technique

C. *2-bit Comparator using GDI Technique*

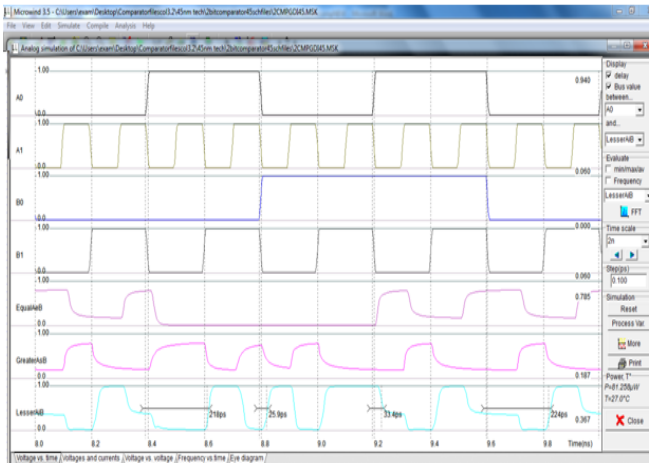

Fig.18 Post-Layout Simulation (Voltage vs. Time) of 2-bit comparator (Configuration 1) in 45nm using GDI Technique

D. 2-bit Comparator using GDIAVL Technique

Fig.19 Post-Layout Simulation (Voltage vs. Time) of 2-bit comparator (Configuration 1) in 45nm using GDIAVL Technique

E. Conventional CMOS 4-bit Comparator

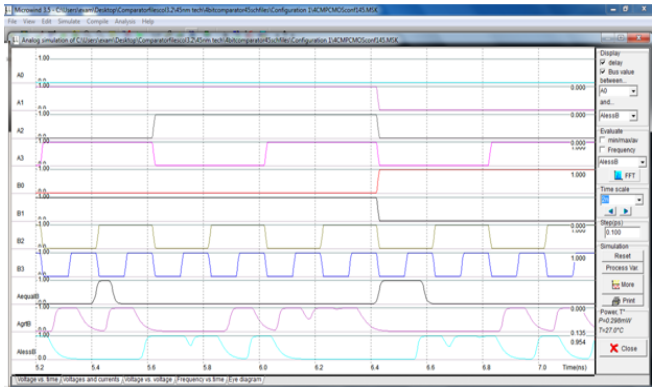

Fig.20 Post-Layout Simulation (Voltage vs. Time) of 4-bit comparator (Configuration 2) in 45nm using CMOS Technique

F. 4-bit Comparator using AVL Technique

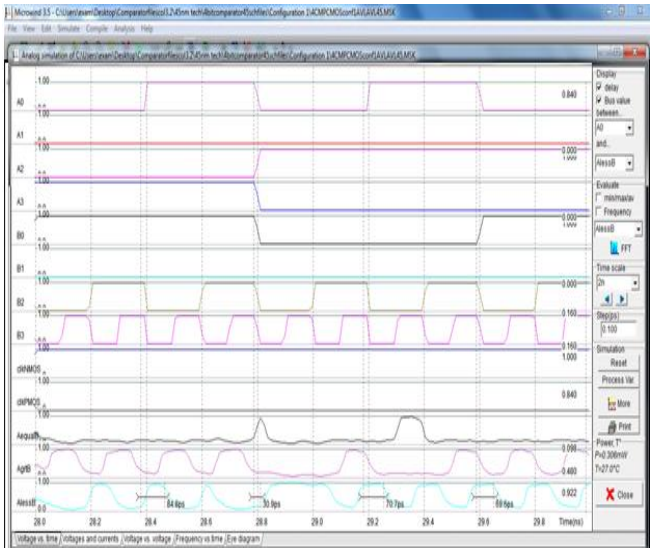

Fig.21 Post-Layout Simulation (Voltage vs. Time) of 4-bit comparator (Configuration 2) in 45nm using AVL Technique

G. 4-bit comparator using GDI Technique

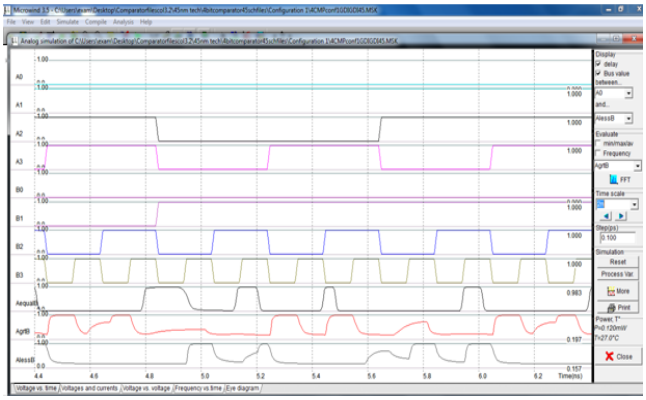

Fig.22 Post-Layout Simulation (Voltage vs. Time) of 4-bit comparator (Configuration 2) in 45nm using GDI Technique

H. 4-bit comparator using GDIAVL Technique

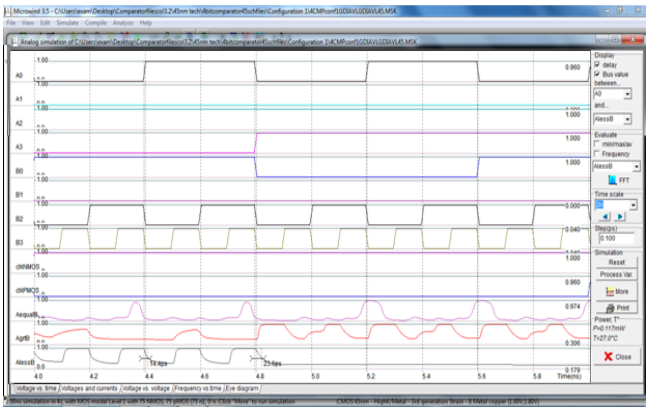

Fig.23 Post-Layout Simulation (Voltage vs. Time) of 4-bit comparator (Configuration 2) in 45nm using proposed GDIAVL Technique

The following tables draw comparison between the low power techniques used to design 4-bit comparator in 45nm and 90nm technologies on the basis of the listed parameters.

Table2. Comparison for 4-bit Digital Comparator -Configuration 1& 2 (45nm)

Tech.	Power (mW)	Leakage I (mA)	Idmax (mA)	Area (μm^2)	Delay (ps)	Xnsistor
Configuration 1 – By definition of 2 bit comparator						
CMOS	0.311	0.103	1.70	769	23	174
AVL	0.248	0.047	3.17	1021	26	189
GDI	0.164	0.074	0.96	187	13	78
GDIAVL	0.13	0.204	0.84	449	8	96
Configuration 2 - 2 bit comparator using 1 bit comparator modules						
CMOS	0.311	0.146	2.53	724	14	174
AVL	0.306	0.021	1.59	969	8	228
GDI	0.12	0	0.44	366	6.5	96
GDIAVL	0.117	0	0.37	467	6.5	150

Table3. Comparison for 4-bit Digital Comparator -Configuration 1& 2 (90nm)

Tech.	Power (mW)	Leakage I (mA)	Idmax (mA)	Area (μm^2)	Delay (ps)	No. of Xnsistor
Configuration 1 – By definition of 2 bit comparator						
CMOS	0.954	0	6.97	4570	5.5	172
AVL	0.273	0.027	3.01	5240	18.5	189
GDI	0.323	0	2.58	1146	4.5	78
GDIAVL	0.242	0.073	1.22	2614	4.5	96
Configuration 2 - 2 bit comparator using 1 bit comparator modules						
CMOS	1.132	0	4.31	3676	8	174
AVL	0.777	0.363	2.62	5485	5	228
GDI	0.185	0	1.06	1711	4.5	150
GDIAVL	0.168	0.346	0.86	2248	4.5	96

V. APPLICATIONS OF 4-BIT COMPARATOR

A. Application in a GCD (Greatest Common Divisor) Calculator

A GCD (Greatest Common Divisor) of two numbers is calculated using Euclidean Algorithm as described in [8]. The schematic of the GCD calculator consists of the following main components:

1) 4-bit 2x1 MUX
2) 4-bit Full Subtractor
3) 4-bit Register
4) 4-bit Digital Comparator (for operation: A<B)
5) Inverter
6) 2 input and 4 input AND gates

All the components have been designed using basic gates except comparator. As found in the simulation results of the 4-bit digital comparator, AVL, GDIAVL techniques show considerable improvement in power consumption with reduced leakage current in Configuration 1 and 2, hence the comparator for the GCD calculator is taken as the 4-bit digital comparator designed with these techniques in 45nm.

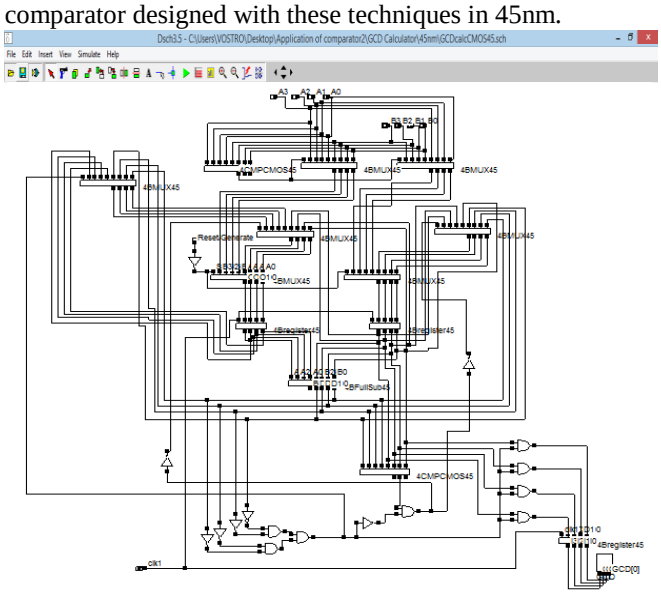

Fig.24 Schematic of GCD Calculator using 4-bit comparator in CMOS Tech. (Configuration1)

Table4. Comparison for GCD Calculator using 4-bit Digital Comparator Configuration 1& 2 (45nm)

S. No.	Tech.	Power (mW)	Leakage Current (mA)	Idmax (mA)
Configuration 1 – By definition of 2 bit comparator				
1.	**CMOS**	1.079	0.074	6.609
2.	**AVL**	0.261	0	0.961
3.	**GDIAVL**	0.73	0	2.829
Configuration 2–2 bit comparator using 1 bit comparator modules				
1.	**CMOS**	1.108	0.096	3.137
2.	**AVL**	0.312	0.01	0.847
3.	**GDIAVL**	0.707	0	5.496

It is seen that the for 45nm technology implementation, *AVL* technique shows considerable reduction in power consumed and leakage current for both configuration 1 and 2 of the 2-bit comparator used for the 4-bit comparator incorporated in a GCD Calculator.

B. Application in a Photocopy Machine Control Circuit

A 4-bit digital comparator is used in a circuit of a Photocopy Machine Control. The schematic of the circuit consists of the following main components:

1) Decimal to BCD Priority Encoder
2) BCD Counter
3) 4-bit Digital Comparator (for operation: A=B)
4) 2 input AND gate, INVERTER
5) 2, 3, 4 input OR gates

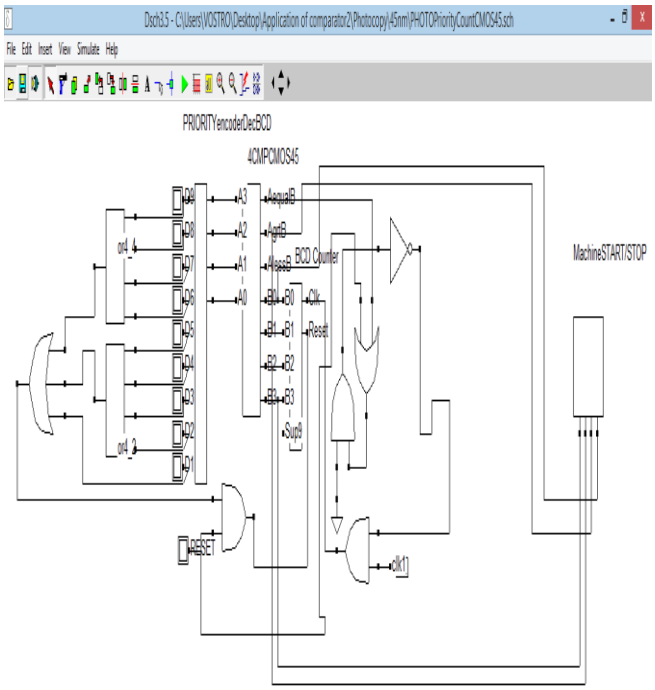

Fig.25 Schematic of Photocopy Machine Control Circuit using 4-bit comparator in CMOS Tech. (Configuration 1)

Table5. Comparison for Photocopy Machine Control Circuit using 4-bit Digital Comparator Configuration 1& 2 (45nm)

S. No.	Tech.	Power (mW)	Leakage Current (mA)	Idmax (mA)
Configuration 1 – By definition of 2 bit comparator				
1.	**CMOS**	0.803	0	2.439
2.	**AVL**	0.693	0.047	3.387
3.	**GDIAVL**	0.556	0	3.178
Configuration 2–2 bit comparator using 1 bit comparator modules				
1.	**CMOS**	0.726	0	3.437
2.	**AVL**	0.512	0	3.166
3.	**GDIAVL**	0.69	0.124	3.119

It is seen that the for 45nm technology implementation, *GDIAVL* technique shows considerable reduction in power consumed and leakage current for configuration 1 while *AVL* technique shows considerable reduction in power consumed and leakage current for configuration 2 of the 4-bit comparator used in Photocopy Machine Control Circuit.

VI. Conclusion

As far as the reduction is power consumption is concerned, a tradeoff between AVL and the proposed technique called GDIAVL can be considered for designing a higher order bit Digital Comparators in 45nm and 90nm technologies.

Acknowledgment

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References

[1] A.P. Chandrakasan, et al.,"Low-power CMOS digital design", *The IEEE Journal of Solid-State Circuits*,Volume: 27, Issue: 4,DOI: 10.1109/4.126534, Page(s): 473 – 484, April 1992.

[2] A. Morgenshtein, and A. Fish, "Gate-diffusion input (GDI) - a technique for low power design of digital circuits: analysis and characterization", *Circuits and Systems, 2002. ISCAS 2002. IEEE*, Volume 1, DOI :10.1109/ISCAS.2002.1009881, Page(s): I 477 - I 480, 2002.

[3] E.R. Menendez; D.K. Maduike; et al, " CMOS Comparators for High-Speed and Low-Power Applications" *IEEE, Computer Design, ICCD 2006. International Conference*, Page(s): 76 – 81, 2006.

[4] Pushpa Saini; Rajesh Mehra," Leakage Power Reduction in CMOS VLSI Circuits**",** *International Journal of Computer Applications* (0975 – 8887) Volume 55– No.8, October 2012

[5] Jaiswal, S.K.; Verma, K.; Singh, G.; Pratihar, N., et al., "Design of 8 bit comparator for Low Power Application*", IEEE, Computational Intelligence and Communication Networks (CICN), 2012* , Page(s): 480-482, Nov. 2012.

[6] A.J. Chowdhury, et.al, "A new leakage reduction method for ultra low power VLSI design for portable devices", *IEEE- Power, Control and Embedded Systems (ICPCES),2nd International Conference*, Page(s): 1- 4 ,Dec 2012.

[7] S.Akashe , G. Sharma, V. Rajak and R.Pandey, "Implementation of high performance and low leakage half subtractor circuit using AVL Technique", *IEEE, Information and Communication Technologies (WICT)*, Page(s): 27-31, 2012.

[8] Darshana Upadhyay and Harshit Patel., "Hardware Implementation of Greatest Common Divisor using subtractor in Euclid Algorithm." *International Journal of Computer Applications* 65(7):24-28, March 2013

[9] Laxmi Kumre; Ajay Somkuwar ; Ganga Agnihotri., et al.,"Design of Low Power 8 bit GDI Magnitude Comparator", *IASIR- IJETCAS*, 4(1), Page(s): 102-108, March-May 2013

[10] Vandana Choudhary, et al., "2 – bit comparator using different logic style of full adder*", IJSCE,* Vol. 3, Issue 2, Page(s): 277-279, May 2013.

[11] S. Ram, and R.R. Ahamed, "Comparison and analysis of combinational circuits using different logic styles", *IEEE, Computing, Communications and Networking Technologies (ICCCNT),*2013 ,Page(s): 1-6, July 2013.

[12] D.K. Gautam, Dr. S.R.P. Sinha, and Er. Y.K. Verma, "Design a low power half subtractor using AVL technique based on 65nm CMOS technology", *IJARCET*, Vol. 2, Issue 2, Nov. 2013.

[13] S.K. Mahammad Akram, et al., "Implementation of low leakage and high performance 8 – bit ALU for low power digital circuits", *IJCA*, Vol. 82, No. 18, Page(s): 24-28, Nov 2013

[14] M. Amala; G.S.S. Prasad, et al., "Design of Low Power 12-Bit Magnitude Comparator", *IJTEL*, Vol. 2, No. 6, Dec. 2013.

[15] T. Sood, and R. Mehra, "Design of low power half subtractor using 90µm CMOS technology", *IOSR-JVSP*, Vol. 2, Issue 3, Page(s): 51-56, 2013.

[16] D.K. Gautam, Dr. S.R.P. Sinha, and Er. Y.K.Verma, "Design of a low power high speed full adder using AVL technique based on CMOS nano-technology", *IOSR-JECE*, Page(s) 19-26, Vol. 8, Issue 1, 2013.

[17] Linet, K., et al., "Modified 4-Bit Comparator Using Sleep Technique", *IJCSET*, Vol. 5, No. 05, May 2014.

[18] Vijaya Shekhawat, Tripti Sharma and K. G. Sharma," Low power magnitude comparator circuit design, *IJCA (0975 – 8887)* Volume 94 – No 1, May 2014.

[19] Narendra Rawat and Rakesh Jain, "Power reduction approach in combinational circuit(half and full subtractor)", *IJSR*, Volume 3, Issue 7, July 2014, Page(s): 1104-1108.

[20] K. Dhar; A.Chatterjee ; S. Chatterjee, et al., "Design of an energy efficient, high speed, low power full subtractor using GDI technique", *Students' Technology Symposium(TechSym*), Page(s): 199-204, 2014.

[21] Neil H. E. Weste, Principal of CMOS VLSI Design, Pearson Education, 2003.

[22] A. Anand Kumar, Fundamentals of Digital Circuits, PHI Learning Pvt. Ltd.,2009.