Impact Of Design And Stability Parameters On Low Power Sram Performance

Prashant Upadhyay, Ajay Kumar Yadav

***Abstract*— Due to the continuous rising demand of handheld devices like iPods, mobile, tablets; specific applications like biomedical applications like pacemakers, hearing aid machines and space applications which require stable digital systems with low power consumptions are required. As a main part in digital system the SRAM (Static Random Access Memory) should have low power consumption and stability. As we are continuously moving towards scaling for the last two decades the effect of this is process variations{1] which have severe effect on stability, performance. Reducing the supply voltage to sub-threshold region, which helps in reducing the power consumption to an extent but side by side it raises the issue of the stability of the memory. Static Noise Margin of SRAM cell enforces great challenges to the sub threshold SRAM design. In this thesis we have analyzed the cell stability of 6T SRAM Cell at various parameters. The cell stability is checked at deep submicron (DSM) technology. SRAM cell is one of the basic storing elements. There is further scope of improving the performance of SRAM cell. This dissertation provides a review of various proposed schemes used to improve the stability of SRAM cell and to reduce its area and power consumption.**

In this paper we have analyzed the effect of temperature [2] and supply voltage (V_{DD}) on the stability parameters of SRAM which is Static Noise Margin (SNM), Write Margin (WM) and Read Margin (RM). The effect has been observed at Cadence software PSpice 16.2 Version . The temperature has a significant effect on stability along with the V_{DD}..

***Index Terms*—SRAM, V_{DD}, SNM, WM, RM**

I. INTRODUCTION

Static random access memories (SRAMs) provide indispensable on-chip data storage and continue to dominate the silicon area in many applications. It is projected that more than 90% of silicon real estate will be occupied by SRAM in the future.

Nowadays Memory is designed by designer in different configuration .For example:

- High speed SRAM memory
- Low Power SRAM memory
- High Density SRAM memory etc.

Design objectives for different memory configuration are different. The memory, for which I describe the parameters, is low power memory. Low power memory technology is achieved by combination of low power chip technology, multi data bit chip configurations in which a large number of data bits are processed simultaneously, small package technology and low voltage chip to chip interfaces. Due to scaling of device we are facing new challenges day by day like oxide thickness fluctuation, intrinsic parameter fluctuation. Working on low threshold voltage[3]and leakage energy also became main concern. SRAM (Static Random Access Memory) is memory used to store data.

Prashant Upadhyay M.Tech, EC Department, Mewar University Chittorgarh, Rajasthan, INDIA.

Ajay Kumar Yadav Asst. Professor in C.E.R.T. Meerut India.

Basic Operations of SRAM and Design Considerations

The various operations of SRAM cell can be understood considering the circuit diagram of conventional SRAM system shown in fig. There are three operations associated with SRAM simulation which is standby mode (Hold), read operation mode and write operation mode. If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply. This operation is called standby operation.

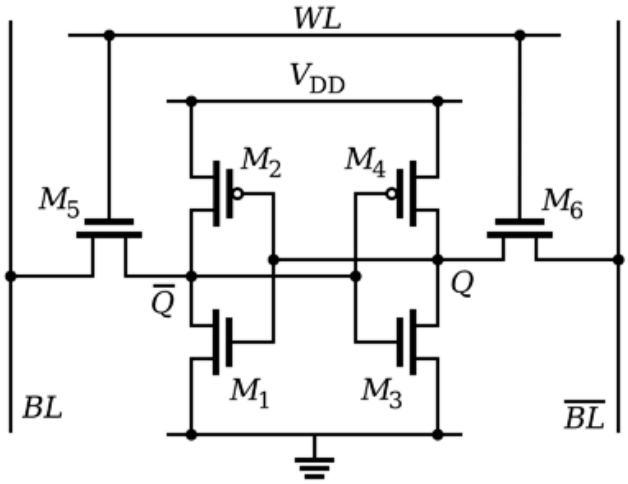

Figure I. Basic 6T SRAM Cell

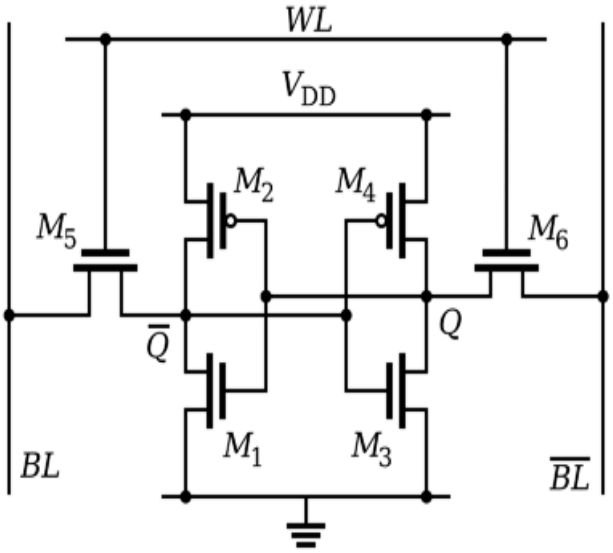

Figure I. Circuit Diagram of Read Operation of SRAM Cell

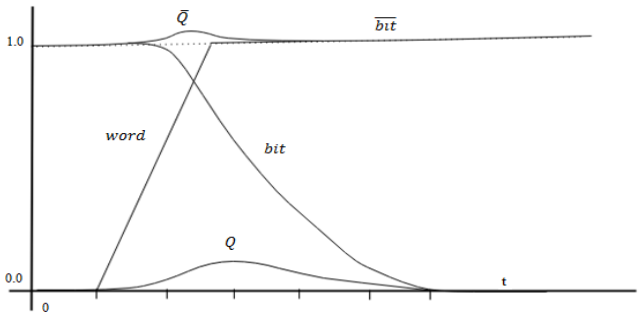

Figure 3 Variation of output in Read Operation of SRAM Cell

II. Low Power Design

In recent years, a rapid development in VLSI fabrication has led to decreased device geometries and decreased transistor densities[4] of integrated circuits and circuits with high complexities and very high frequencies have started to emerge. Such circuits can consume excessive amount of power and generate an increased amount of heat. Circuits with excessive power dissipation are more susceptible to run time failures and present serious reliability problems. Every 100C increase in operating temperature approximately doubles a component's failure rate. Increasingly expensive packaging and cooling strategies are required as a chip power increases. Due to these concerns, circuit designers are realizing the importance of limiting power consumption and improving energy efficiency at all levels of the design.

The second driving force behind the low power design phenomenon is a growing class of personal computing devices such as portable desktops, digital pens, audio and video-based multimedia products and wireless communication and imaging system, such as personal digital assistants, personal communicators and smart cards. These devices and systems demand high speed, high throughput computations[5]

III. SRAM Performance, Figures of Merit and Performance Parameters

SRAM is a volatile memory and its task from the user's point of view is simple: as long as the cell is connected to supply voltage, it must keep data (hold) and enable to read and write data. Ideally, this must be done very fast, on minimum die area, with almost no leakage[6] and great yield. Each core cell has different qualities and strengths, depending on its design. All these different qualities must be measurable to be able to compare various core cells. While some qualities are unambiguous (e.g. area in μ^{m^2}), some others need Figures of Merits (FoMs) when they are not directly measurable (e.g. cell stability

Supply Voltage V_{DD}

This is one of the external factors influencing the SNM. There is no such physical factor that has an impact on the supply voltage assuming that the voltage that is being supplied to SRAM is as constant as coming from a `DC' source. But since we are using the power-up state of SRAM which is a transient event during which the supply voltage is raised from 0 to V_{DD}, the ramp-up speed of the power-up is expected to have an impact on SNM..

Threshold Voltage V_{TH}

The threshold voltage (V_{TH}) is usually defined as the gate voltage where an inversion Layer [4]forms at the interface between the oxide layer and the body of the transistor Threshold voltage for a MOSFET with p-type substrate (NMOS) and n-type substrate (PMOS) can be expressed in terms of various parameters of MOS capacitor as follows

$$V_{TH_{NMOS}} = V_{FB} + 2|\emptyset_F| + \gamma\sqrt{2|\emptyset_F|}$$

$$V_{TH_{PMOS}} = V_{FB} - 2|\emptyset_F| - \gamma\sqrt{2\emptyset_F}$$

The terms involved in the equations are:

Flat band Voltage(V_{FB})

This is affected by the presence of charge in the oxide or at the oxide-semiconductor interface. The Flat band voltage corresponds to the voltage which when applied to the gate electrode yields a at energy band in the semiconductor. The V_{FB} is described as follows:

$$V_{FB} = \emptyset_{ms} - \left(\frac{q.N_{OC}}{C_{ox}}\right)$$

where,

Φms is the difference in the work function of the gate and the substrate,

Measured in V,

q is the charge of an electron, measured in C,

Noc is the oxide charge density, measured in cm^{-3},

Cox is the capacitance of the gate oxide per unit area, measured in $\frac{F}{m^2}$

Here,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Surface Potential $(\emptyset_F)$

This factor depends upon the substrate doping, the intrinsic carrier concentration and the temperature as shown by the equations below

$$\emptyset_{F_{NMOS}} = -\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$$

$$\emptyset_{F_{PMOS}} = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right)$$

where,

k is the Boltzmann constant measured in eV/K

T is the temperature measured in K

q is the charge of an electron measured in C,

N_a is the concentration of acceptors in substrate for NMOS measured in cm^{-3},

N_d is the concentration of donors in substrate for PMOS measured in cm^{-3},

n_i is the intrinsic carrier concentration measured in cm^{-3}.

5-Design Parameters and optimization of SRAM Memory Cells

IV. Standby Leakage Power

Standby leakage power has become an important constraint in today's processor design. According to the figures posted by International Technology Roadmap for Semiconductors (ITRS), the leakage power[7] is set to become a dominant source of power dissipation in sub 90 nm technologies. With the technology node fast approaching the 45 nm mark, the leakage power is expected to dominate the dynamic switching power [8] and account for more than 50% of the total chip power. As a result, Standby leakage[9] power becomes an important constraint to be considered and controlled while designing digital circuits. With decreasing technology node, supply voltage is continually scaled to reduce the dynamic power dissipation. The continued voltage scaling offsets in lowered device speeds. To compensate this decrease, the threshold voltage, V_{TH}, is reduced commensurately.

V. Sub Threshold Leakage

Subthreshold leakage or subthreshold drain conduction refers to the current that flows between the source and drain of a MOSFET when the gate-to-source voltage is below the threshold voltage (V_{TH}). This region of operation of a transistor is also referred to as the subthreshold region of operation. The transistor is essentially considered to be turned "off". The commonly used model of Subthreshold leakage [10]current (I_{Sub}), through a transistor is

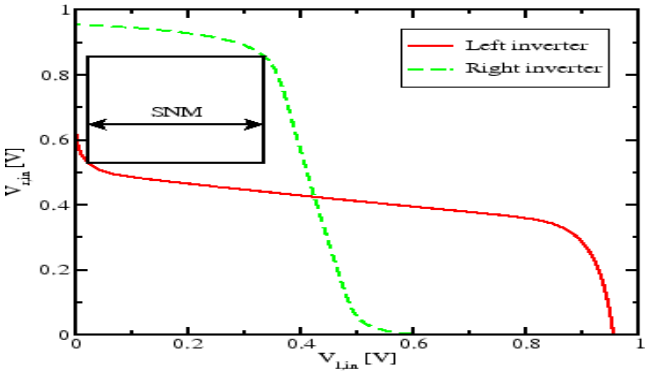

Figure V. SNM for an SRAM cell

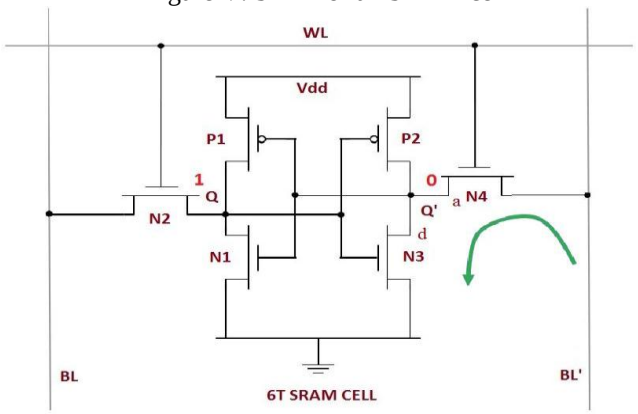

Figure.1 Improving SNM

VI. Analysis

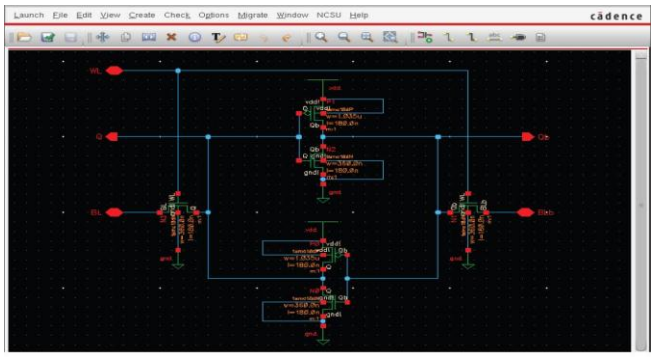

Figure 6 6T SRAM using Cadence

VII. Conclusion

Due to increased demand for high performance as well as low power system design, it is often required to have on-chip memory or embedded memory to support the high data bandwidth application. Among embedded memories, SRAM continues to play a pivotal role in almost all VLSI systems. In sub-100nm technology, the trade-off of SRAM design parameters, such as area, power, speed, and noise stability are so critical to manage that there is no single solution to optimize all of these parameters. The optimum solution lies in designing the SRAM array depending upon the type of target application. It is either a high performance application like a server, or desktop, or it is a low power mobile application like a cell phone or sensor node. To mitigate these critical design issues, this thesis makes several contributions. First, several novel SRAM designs are presented. The design criteria are exclusively based on the target application of the memory array

References

[1] X. Tang D. Neamen, An introduction to semiconductor devices, McGraw-Hill, 2006.
[2] J.M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital integrated circuits, Prentice- Hall, 2002.
[3] A. Pavlov and M. Sachdev, Cmos sram circuit design and parametric test in nano-scaled technologies, Springer, 2008
[4] M. Khellah, Y. Ye, N. S. Kim, D. Somasekhar, G. Pandya, A. Farhang, K. Zhang, C. Webb and V. De, "Wordline & bitline pulsing schemes for improving SRAM cell stability in low-Vcc 65nm CMOS designs," Symp. on VLSI Circuits, pp. 9-10, June 2006.
[5] H. Calhoun, A. Chandrakasan, "A 256kb Sub-threshold SRAM in 65nm CMOS," in Tech. Dig., ISSCC 2006, San Francisco, CA, Feb. 6-9, 2004, pp. 2592-2601.
[6] E. Seevinck, F.J. List, and J. Lohstroh, Static-noise margin analysis of mos sram cells, IEEE Journal of Solid-State Circuits 22 (1987), no. 5, 748-754.
[7] V. De, J. Meindl, "Intrinsic MOSFET parameter placement due to random placement", IEEE Trans on VLSI, 1997, pp. 369-376.
[8] K.Itoh, M.Horiguchi,h.Tanaka Ultra –Low Voltage Nano –Scale Memories, Springer, 2007
[9] Chandrakasan and R. Brodersen. CMOS Low Power Digital Design. Kluwer Academic Pubs., 1996.
[10] C.-T. Chuang, S. Mukhopadhyay, J.-J. Kim, K. Kim, R. Rao, "High-performance SRAM in nanoscale CMOS: Design challenges and techniques," in IEEE Int. Workshop., Memory Technology, Design and Testing, Taipei, Taiwan, Dec. 3-5, 2007, pp. 4-12.
[11] D P. Mazumder and K. Chakraborty, "Testing and Testable Design of Random-Access Memories"'Kluwer Academic Publisher, 1996 (428 pages) design, 2004.

Prashant Upadhyay M.Tech, EC Department, Mewar University, Chittorgarh, Rajasthan, INDIA
Ajay Kumar Yadav Asst. Professor in C.E.R.T. Meerut India