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Transformerless Grid-Connected Inverters for Photovoltaic Modules: A Review

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***Abstract*—Day by day the contribution of renewable energy is increased in total energy consumed in the world due to the fact that they generate energy by keeping the environment clean. Among all these systems Photovoltaic power system becomes popular and consists of isolation transformer in inverter. Due to increase in demand of low cost and high efficiency inverters the transformerless inverters becomes most popular in Photovoltaic (PV) grid connected power system. In transformerless inverter due to removal of transformer the size, weight and cost of solar power conversion system also reduced. But when transformer is eliminated, there is galvanic connection between PV panels and grid which leads flowing of Leakage current due to formation of parasitic capacitance between PV panels and ground which creates some safety issues.**

The paper presents the review on transformerless inverter technologies for connecting photovoltaic (PV) modules to grid with common mode leakage current elimination. The transformerless inverters are H5, H6, HERIC, NPC, using unipolar sinusoidal pulse width modulation (SPWM) control strategy, using double-frequency sinusoidal pulse width modulation (SPWM) control strategy. In this paper Various inverter topologies are studied and compared.

Among these transformerless inverters, unipolar sinusoidal pulse width modulation (SPWM) control strategy and double-frequency sinusoidal pulse width modulation (SPWM) control strategy are the best options for transformerless inverter. In both the strategies common mode leakage current eliminated completely. The higher frequency and lower current ripples are obtained, thus the total harmonic distortion of the grid-connected current are also reduced

by using the double frequency SPWM strategy.

The condition for common mode leakage current elimination also derived. Finally, A 1 kW inverter is simulated in MATLAB/Simulink with both the control strategies.

***Index Terms*— Common-mode leakage current, Parasitic capacitance, H5, H6, HERIC, NPC, Unipolar SPWM, Double-frequency SPWM.**

I. INTRODUCTION

Renewable sources of energy is the solution of today's increasing demand of electrical energy. Among many renewable sources the solar energy is best and reliable way for generation of electricity.

Solar power generation system is mainly consisting of solar array which act as a generator and power conversion unit.

The power conversion unit in most of the commercial PV inverters consists of a low frequency transformer to make galvanic isolation between PV modules and grid which provides personal safety and cope up with the output voltage.

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But use of transformer makes system bulky, increases cost of system and reduces efficiency of system. So as to overcome these drawbacks, transformerless inverter topology is evolved. But in transformerless inverter there are some safety issues because a galvanic connection between the grid and the PV array exists, as a result the leakage current flows between PV panels and ground [1].

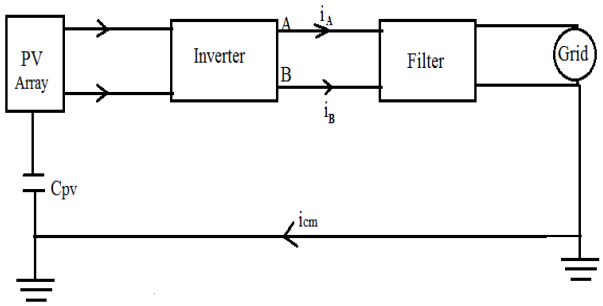


Fig.1.Resonant circuit of common mode leakage current.

Because of the flowing of common mode leakage current the system losses increases, quality of the grid connected current reduces and induces the severe conducted and radiated electromagnetic interference. It also creates personal safety problems.

When PV panels are grounded resonant circuit is created which includes the ground capacitance, filter, inverter and impedance of grid [2] as shown in Fig.1.

Condition for eliminating common mode leakage current

In the transformerless PV grid connected system there is a galvanic connection between the grid and the PV array exists, which may form a common-mode resonant circuit and induce the common-mode leakage current. The simplified equivalent model of the common-mode resonant circuit obtained in [3]–[5] as shown in Fig.2

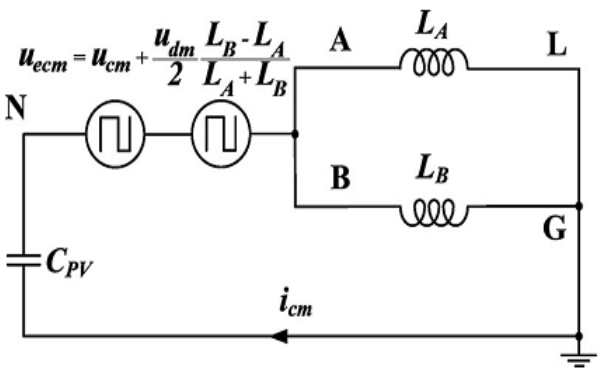


Fig.2 Simplified equivalent model of common-mode resonant circuit.

Where Cpv is the parasitic capacitor, L_A and L_B are the filter inductors, i_{cm} is the common-mode leakage current, and an equivalent common-mode voltage u_{ecm} is defined by,

$$u_{ecm} = u_{cm} + \frac{u_{dm}}{2}\frac{L_B - L_A}{L_{A+}L_B}. \quad (1)$$

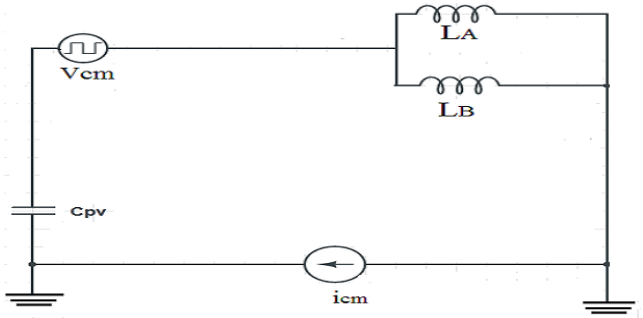


Fig.3 Equivalent circuit for leakage current analysis.

Thus from equivalent circuit for leakage current analysis shown in fig.3, the common mode leakage current i_{cm} is,

$$i_{cm} = Cpv\left(\frac{dV_{cm}}{dt}\right) \quad (2)$$

Thus from (2) it is derived that the common mode leakage current is depend upon variation in common mode voltage. So for eliminating leakage current, it is necessary to keep common mode voltage constant.

II. TRANSFORMERLESS INVERTER TECHNOLOGIES

H6 inverter

H6-type configuration is composed of six power MOSFETs (S1-S6), two freewheeling diodes (D1and D2), and two split inductors (L1and L2) as a low-pass filter shown in Fig.4.This circuit is well suited for non-isolated ac module applications[6].

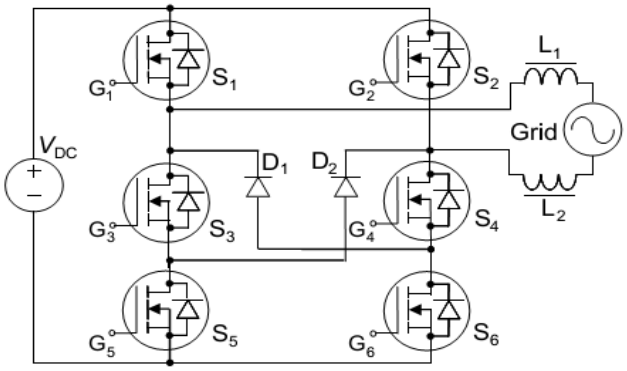


Fig.4 H6 inverter.

PWM scheme for the H6 inverter is illustrated in Fig. 5.In H6 inverter, the top device in one leg and the bottom device in the other leg are switched simultaneously in the PWM cycle and the middle device operates as a polarity selection switch in the grid cycle From Fig.5, if the sinusoidal control voltage $\mathbf{v_{control}}$, which is synchronized with grid voltage, is higher than the triangular carrier voltage $\mathbf{v_{carrier}}$, the gating voltage G1 and G6 are active; otherwise, G1 and G6 are inactive. And if voltage $\mathbf{v_{control}}$ is higher than zero, the gating voltage G4 is active; otherwise, G4 is inactive. Similarly, the comparison of ($-\mathbf{v_{control}}$) with $\mathbf{v_{carrier}}$ or zero results in the logical signals to control G2, G5 and G3, respectively.

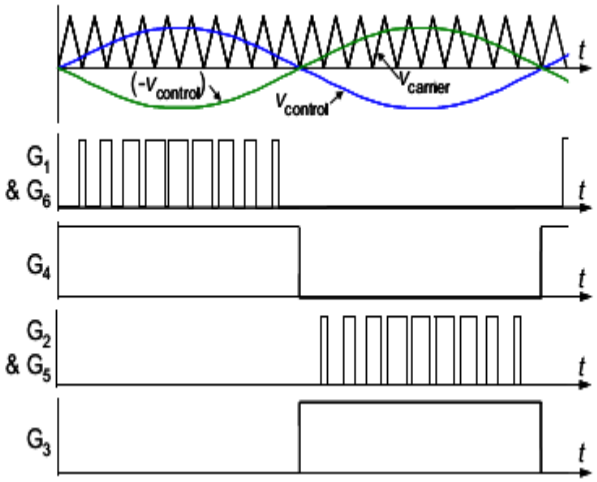


Fig.5 PWM scheme for H6 inverter.

H5 inverter

This inverter provides a disconnection from the DC side in order to get a zero leakage ground current. The disconnection is necessary because in transformerless inverter a galvanic connection can appear between the grid and the inverter, therefore resonant circuits can turn up in the system[7]. The H5 topology structure is given in Fig. 6.

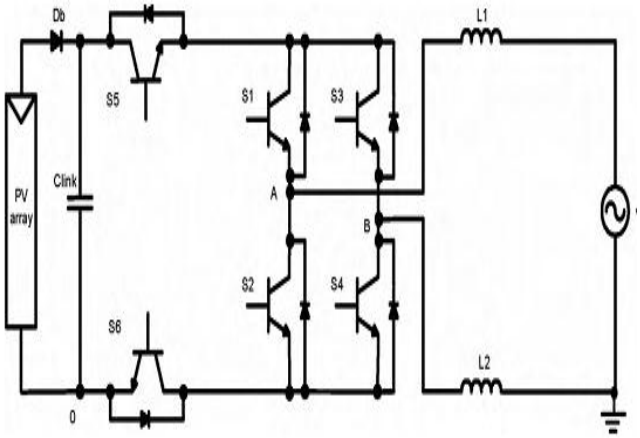


Fig. 6 H5 inverter.

During the positive half cycle, S5 and S6 commutate at switching frequency whereas S1 and S4 are ON in order to modulate the input voltage. On the other hand, when negative half cycle is present, S5 and S6 Commutates switching frequency whereas S3 and S2 are ON. The disadvantages of this topology are the higher conduction losses due to the series association of three switches during the active phase, and operation with reactive power is only possible with modified switching strategy characterized by increased losses.

HERIC (Highly Efficient and Reliable Inverter Concept)

The HERIC (Highly Efficient and Reliable Inverter Concept) inverter avoids a fluctuating potential on the DC terminals of the PV generators by means of disconnecting the converter from the load (utility grid)[8]. In this case the zero voltage level is obtained using a bidirectional switch during freewheeling periods. This inverter is shown in Fig. 7.

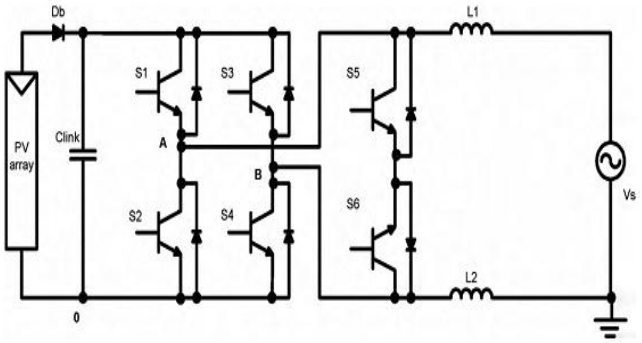


Fig. 7 HERIC inverter.

This inverter works as follow: During the positive half cycle S6 remains connected, whereas S1 and S4 commutate at switching frequency in order to generate both active and zero vectors. When an active vector is present (S1 and S4 are ON), current flows from the PV panels to the load (grid), when a zero vector occurs, S1 and S4 are switched OFF and then, the current flows through S6 and D1, this is the freewheeling situation. On the other hand, when the negative cycle is coming, S6 goes OFF and S5 goes ON, whereas S3 and S2 commutate at switching frequency. It means that an active vector is present when S3 and S2 are ON, therefore the current flows from the PV panel towards the load, thus when S3 and S2 turn off, a zero voltage vector is present in the load, then current flows through S5 and D2. This kind of modulation allows having a freewheeling situation with no connected load (utility grid).This topology reduces the occurrence of leakage currents. The drawbacks are increased amount of semiconductors and the incapability of processing reactive power with default switching strategy.

NPC ((Neutral Point Clamped) :

The NPC inverter has a good Performance regarding the voltage fluctuations present on the DC bus, due to the fact that in this case the middle point of the input capacitors is connected to neutral. This situation avoids capacitive earth current and their negative influence on the Electromagnetic compatibility of the circuit. In order to allow Power transfer into the grid the DC bus voltages have to be always higher than the grid voltage amplitude, due to this, take into account that the output voltage of PV modules is around 24 V, it is necessary to use a large number of modules or in other case, it is possible to use an input converter in order to boost the input voltage. Fig.8 shows the NPC topology[9].

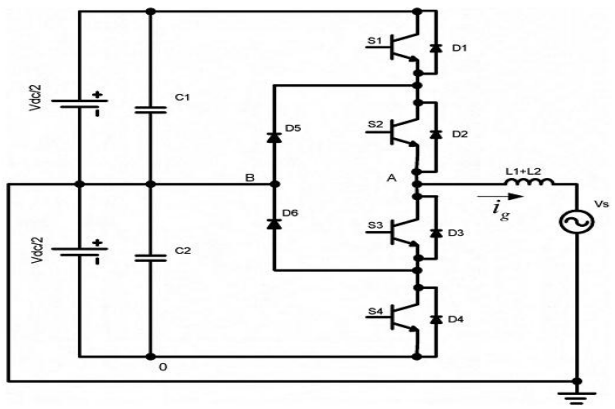


Fig. 8 NPC inverter.

The operation of this topology is as follow: During the positive half cycle, S2 remains ON, S1 commutate at switching frequency and S3 and S4 are OFF. When S1 is ON, and active vector is applied to the load and the current flows through S1 and S2 toward the load (current increasing), also when S1 is OFF, a zero voltage vector is applied to the load, in this case, the current flows through D5 and S2 (current decreasing).On the other hand, during the negative half cycle, S3 remains ON, whereasS4commutateatswitching frequency and S I and S2 are OFF. When S4 is ON an active vector is applied to the load and current flows through S3 and S4 toward the load(current increasing), also when S4 is OFF , a zero voltage vector is applied to the load, in this case, current flows through S3 and D6(current decreasing).

Proposed method

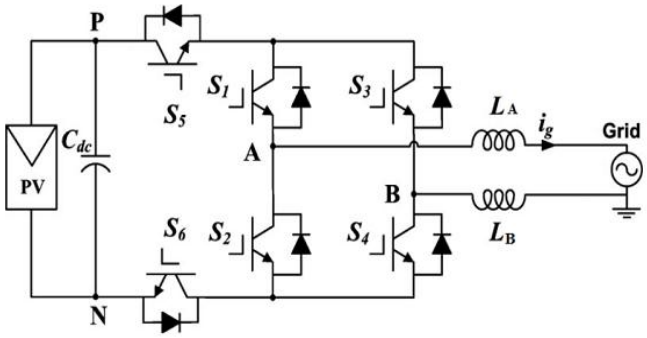


Fig.9 Proposed inverter topology.

The proposed inverter has one phase leg including S1 and S2 operating at the grid frequency, and another phase leg including S3 and S4 commutating at the switching frequency. Two additional switches S5 and S6 commutate alternately at the grid frequency and the switching frequency to achieve the dc-decoupling states.

A. Unipolar SPWM strategy

The four operation modes that generate the voltage states of $+U_{dc}$,0,$-U_{dc}$ are shown in Fig. 10. Fig.11 shows the ideal waveforms of the proposed inverter with unipolar SPWM. In the positive half cycle,S1 and S6 are always ON,S4 and S5 commutate at the switching frequency with the same commutation orders.S2 andS3, respectively, commutate complementarily to S1 and S4. Accordingly, Mode 1 and Mode 2 continuously rotate to generate $+U_{dc}$ and zero states and modulate the output voltage. Likewise, in the negative half cycle, Mode 3 and Mode 4 continuously rotate to generate $-U_{dc}$ and zero states as a result of the symmetrical modulation.

Mode 1: when S4 and S5 are ON,u_{AB}=$+U_{dc}$ and the inductor current increases through the switches S5,S1,S4, and S6. The common-mode voltage is

$$u_{cm}=\frac{1}{2}(u_{AN}+u_{BN})=\frac{1}{2}(U_{dc}+0)=\frac{U_{dc}}{2} \quad (3)$$

Mode 2: when S4 and S5 are turned OFF, the voltage u_{AN}falls and u_{BN} rises until their values are equal, and the antiparallel diode of S3 conducts. Therefore, u_{AB}=0 V and the inductor current decreases through the switchS1 and the antiparallel diode ofS3. The common-mode voltage changes into

$$u_{cm}= \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}\left(\frac{U_{dc}}{2} + \frac{U_{dc}}{2}\right) = \frac{U_{dc}}{2} \quad (4)$$

Mode 3: whenS3 andS6 are ON,u_{AB} =–U_{dc} and the inductor current increases reversely through the switches S5, S3, S2 and S6. The common-mode voltage becomes

$$u_{cm}= \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}(0 + U_{dc}) = \frac{U_{dc}}{2} \quad (5)$$

Mode 4: whenS3 andS6 are turned OFF, the voltage u_{AN} rises and u_{BN} falls until their values are equal, and the antiparallel diode of S4 conducts. Similar as to Mode 2,u_{AB}=0 V and the inductor current decreases through the switch S2 and the antiparallel diode of S4. The common-mode voltage u_{cm} also Keeps U_{dc}/2 referring to (4). From (3) to (5), the common-mode voltage can remain a constant U_{dc}/2 during the four commutation modes in the improved inverter with unipolar SPWM. The switching voltages of all commutating switches are half of the input voltage U_{dc}/2, and thus, the switching losses are reduced. Furthermore, in a grid period, the energies of the switching losses are distributed averagely to the four switches S3, S4, S5, and S6 with high-frequency commutations, and it benefits the thermal design of printed circuit board and the life of the switching components compared with H5 inverter.

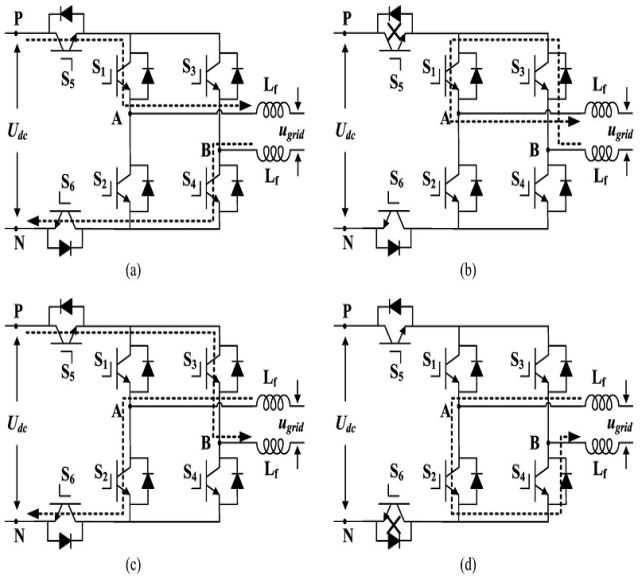


Fig.10 Four operation modes of the improved inverter with unipolar SPWM. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

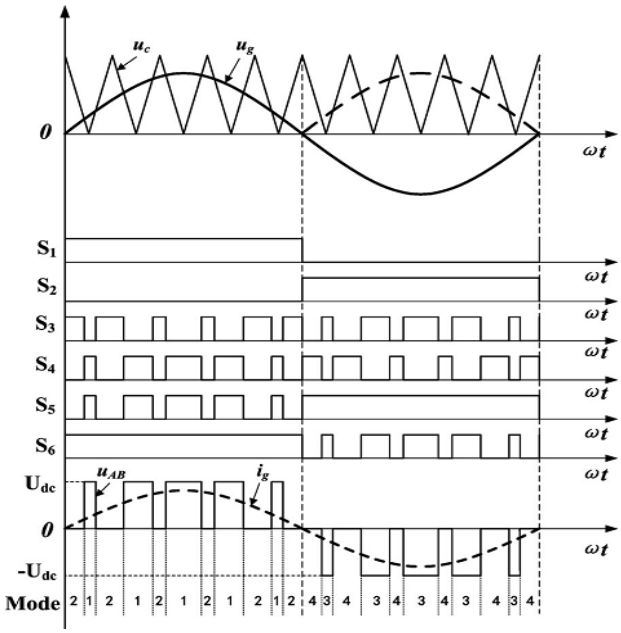


Fig.11 Ideal waveforms of the improved inverter with unipolar SPWM.

B. Double-Frequency SPWM Strategy

The proposed inverter can also operate with the double-frequency SPWM strategy to achieve a lower ripple and higher frequency of the output current[10]. In this situation, both phase legs of the inverter are modulated with 180◦ opposed reference waveforms and the switches S1–S4 all acting at the switching frequency. Two additional switches S5 and S6 also commutate at the switching frequency cooperating with the commutation orders of two phase legs. Accordingly, there are six operation modes to continuously rotate with double frequency and generate +U_{dc} and zero states or –U_{dc} and zero states, as shown in Figs. 10 and 12 Fig. 13 shows the ideal waveforms of the improved inverter with double-frequency SPWM. In the positive half cycle,S6 and S1have the same commutation orders, and S5and S4 have the same orders. S2 andS3, respectively, commutate complementarily to S1 andS4. Accordingly, Mode 1, Mode 2, and Mode 5 continuously rotate to generate +U_{dc} and zero states and modulate the output voltage with double frequency. In the negative half cycle, Mode 3, Mode 4 and Mode 6 continuously rotate to generate –U_{dc} and zero states with double frequency due to the completely symmetrical modulation.

Mode 5: when S1 and S6 are turned OFF, the voltage u_{AN} falls and u_{BN} rises until their values are equal, and the antiparallel diode of S2 conducts. Therefore, u_{AB}=0 V and the inductor current decreases through the switchS4 and the antiparallel diode ofS2. The common-mode voltage u_{cm} keeps a constant U_{dc}/2.

Mode 6: similarly, when S2 and S5 are turned OFF, the voltage u_{AN} rises and u_{BN} falls until their values are equal, and the antiparallel diode ofS1 conducts. Therefore u_{AB}=0 V and the inductor current decreases through the switch S3 and

the antiparallel diode ofS1. The common-mode voltage u_{cm} still is a constant U_{dc} /2 referring to (9). Under the double-frequency SPWM strategy, the common-mode voltage can keep a constant U_{dc}/2 in the whole switching process of six operation modes. Furthermore, the higher frequency and lower current ripples are achieved, and thus, the higher quality and lower THD of the grid-connected current are obtained, or a smaller filter inductor can be employed and the copper losses and core losses are reduced. Thus the proposed method eliminates common mode leakage current by keeping common mode voltage constant for all six modes and also reduces the amount of semiconductors as compared to other methods.

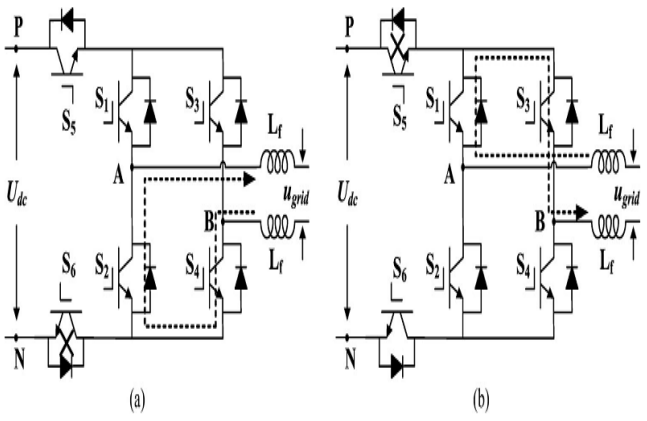


Fig. 12 remaining two of six operation modes under double-frequency SPWM. (a) Mode 5. (b) Mode 6.

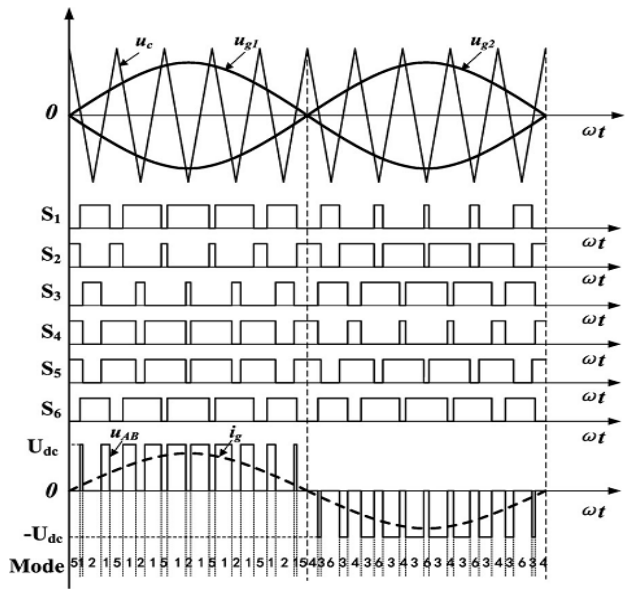
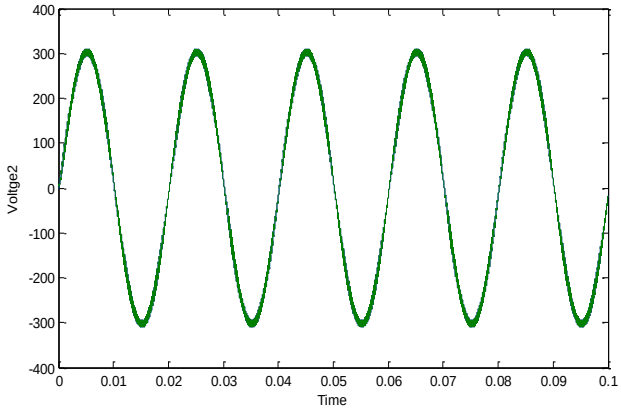


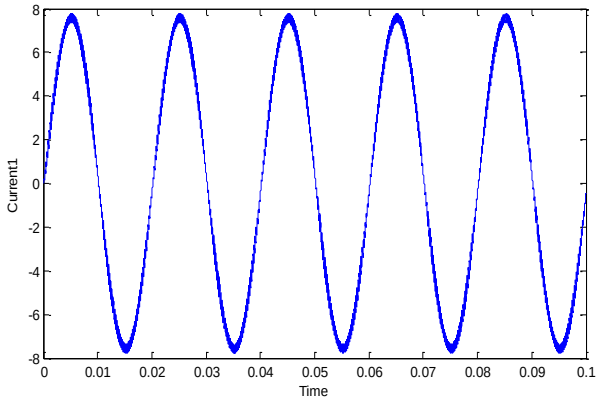
Fig. 13 Ideal waveforms of the improved inverter with double-frequency SPWM.

III. SIMULATED RESULTS

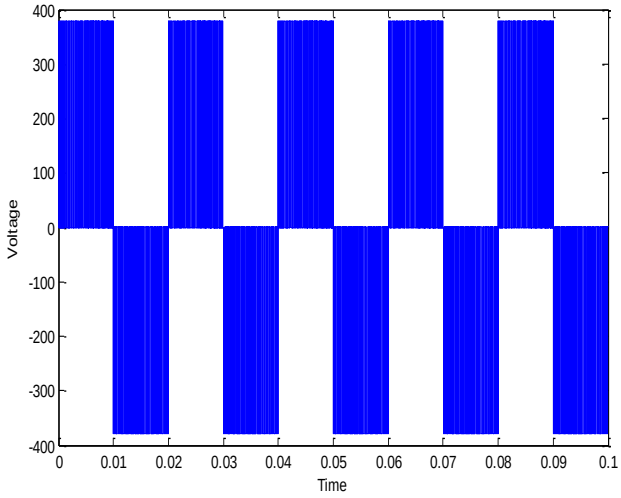
A 1 kW inverter for PV array is simulated with PV panel is connected to ground by parasitic capacitance 75 nF. The details of components and parameters used are as: output power, P_{out} =1 kW; input voltage, U_{dc} =380V; input capacitor, C_{dc} =940μF; grid voltage, U_g =220 V_{ac} ; grid frequency, f_g =50Hz;switch frequency, f_g =20 kHz; filter inductor,L_f =4 mH; parasitic capacitor,C_{pv}=75 nF. Fig. 14 shows the simulated results by using the unipolar SPWM and double frequency SPWM control strategy.



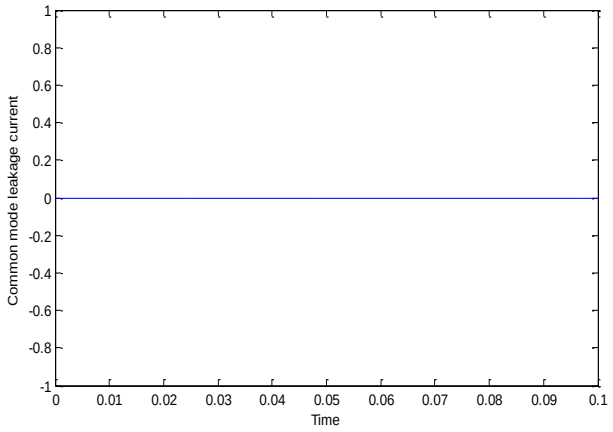
a) Grid voltage U_g



b) Grid current i_g



c) Common mode voltage u_{cm}



d) common mode leakage current i_{cm}

Fig.14 Simulated waveforms with unipolar and double frequency SPWM strategies.

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