Power Quality Enhancement of Diode Clamped Multilevel Inverter Using Different Modulation Schemes

Rahul Kumar Sahu, Govind Pandiya, E Vijay Kumar

Abstract— **Maximum utilization of DC bus voltage with improved Power Quality spectral performance are the highlights of third harmonic current injection modulation scheme for multilevel inverters. In this paper an extensive investigation on third harmonic injection based modulation scheme has been proposed. Thus an improved performance in terms of reduced THD and higher RMS value has been achieved by a control strategy with lesser complexity; thereby preserving the simplicity of carrier based conventional modulation scheme. The proposed switching strategy is investigated through MATLAB simulation.**

Index Terms— **Power Quality, THD, MATLAB/Simulink**

I. INTRODUCTION

The concept of multilevel power conversion has been gaining popularity mainly due to improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. These converters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating. These improvements in power conversion are achieved by using multiple voltage steps strategy which is an essential reason for medium voltage operation to lowering dv/dt and reducing stress on motor winding insulations. Multilevel power conversion has been receiving increasing attention in past few years for high power applications. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literatures.

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels.

Depending on voltage levels of the output voltage, the inverters can be classified as two-level inverters and multilevel inverters. The inverters with voltage level 3 or more are referred as multilevel inverters. Multilevel inverters have become attractiverecently particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage.

Limited fossil fuel reserves and ever increasing population are posing a challenging issue of catering the increasing demand of electrical energy. At the same time, environmental issues such as global warming are also a cause of serious concern to humanity. In response to these problems, most countries have adopted policies which broadly cover two directives:

- Efficient utilization of current energy resources.
- Finding out ways for effective utilization of renewable energy resources.
- The conversion of power from one form to another is a major part of the utilization process. Hence, an efficient and effective conversion process is needed to reduce the waste of energy and improve the power quality.

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the DC bus voltage so as to achieve steps in the output voltage. The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter. A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In a three-level inverter each of the three phases of the inverter shares a common DC bus, which has been subdivided by two capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors. The voltage stress across each switching device is limited to V_{dc} through the clamping diodes . It is assumed that the total DC link voltage is$V_{dc}$and mid-point is regulated at half of the DC link voltage, the voltage across each capacitors is $V_{DC/2}$ .In a three level diode clamped inverter, there are three different possible switching states which apply the stair case voltage on output voltage relating to DC linkcapacitorsvoltage rate. For a three-level inverter, a set of two switches is on at any given time and in a five-level inverter, a set of four switches is on at any given time and so on.

The simplest PWM technique implementation can be done using a triangular carrier signal withfrequency *fc* trying to modulate a reference signal with lower frequency *fs*. A sinusoidal reference signal is modulated using a triangular carrier obtaining a high frequency PWM pulse train

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.Multilevel PWM can be obtained using more than one triangular carrier. For an N-level converter, N-1 carriers are arranged in contiguous bands across the full linear modulation range of the multilevel converter. All the carriers have the same frequency and amplitude and the reference waveform is placed in the middle of the carrier bands. After reviewing the existing literature on various aspects relating to Investigations on Control Strategies of Multilevel Inverters Topology, the focus area of this paper willbe on Pulse Width Modulation Strategies based on third harmonic Performance indices like %THD, Crest Factor (CF) and Form Factor (FF) related to power quality issues will be evaluated, presented and analyzed. The variation of Total Harmonic Distortion (THD) in the inverter output voltage will be observed for various modulation indices.

II. POWER QUALITY

Power quality determines the fitness of electrical power to consumer devices. Synchronization of the voltage frequency and phase allows electrical systems to function in their intended manner without significant loss of performance or life. The term is used to describe electric power that drives an electrical load and the load's ability to function properly. Without the proper power, an electrical device (or load) may malfunction, fail prematurely or not operate at all. There are many ways in which electric power can be of poor quality and many more causes of such poor quality power.

The electric power industry Comprises Electricity generation (AC power), electric power transmission and ultimately electricity distribution to an electricity meter located at the premises of the end user of the electric power. The electricity then moves through the wiring system of the end user until it reaches the load. The complexity of the system to move electric energy from the point of production to the point of consumption combined with variations in weather, generation, demand and other factors provide many opportunities for the quality of supply to be compromised. While "power quality" is a convenient term for many, it is the quality of the voltage rather than power or electric current that is actually described by the term. Power is simply the flow of energy and the current demanded by a load is largely uncontrollable.

III. CONTROL SCHEME

The control scheme for the multilevel can be explained from the waveform shown below in Fig.1and Fig.2. Thewave form shown below shows the carrier and reference current for a nine level diode clamped multilevel inverter. As it can be verified from the figure that a third harmonic waveform has been superimposed on a fundamental reference wave . The resultant reference wave form is a flat topped wave having a modulation index less than 1.

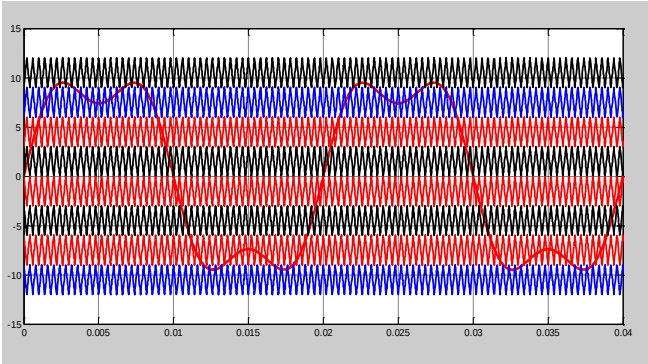

Fig. 1 carrier and reference waveform

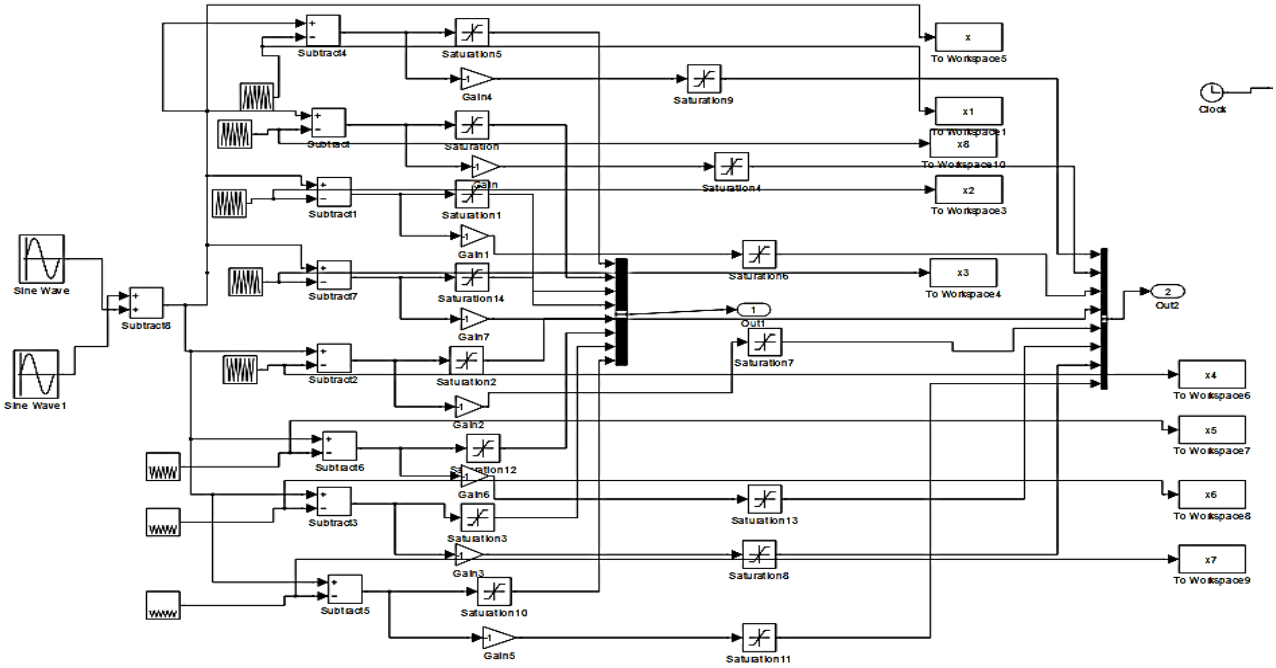

Fig.2 subsystem for the proposed modulation scheme

IV. RESULTS AND DISCUSSION

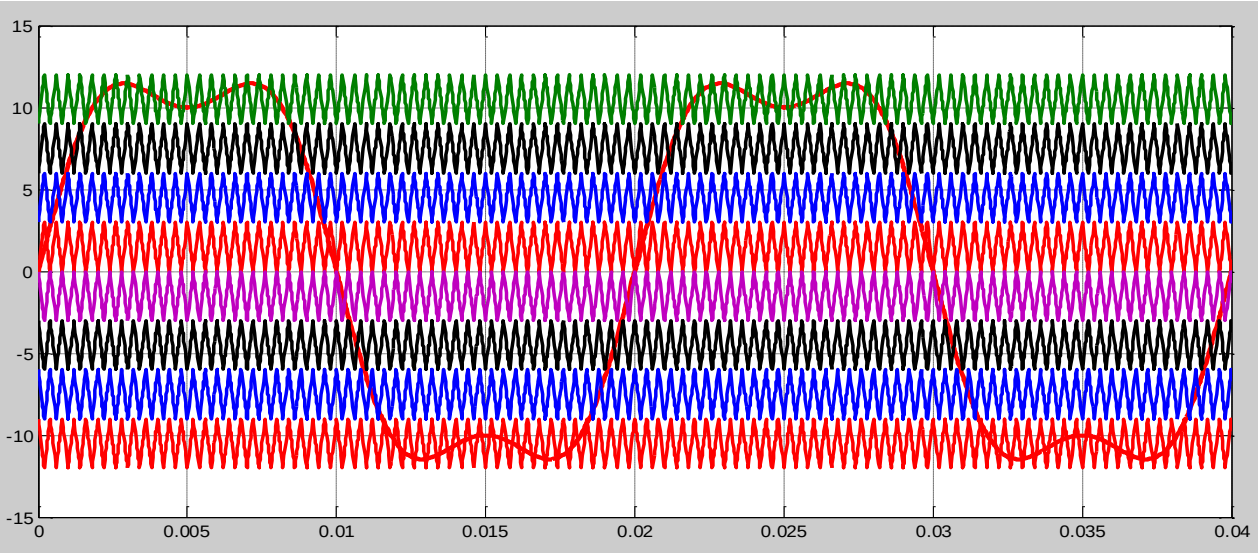

Fig. 3 carrier and refrence wave form for modulation index 1and k=.21

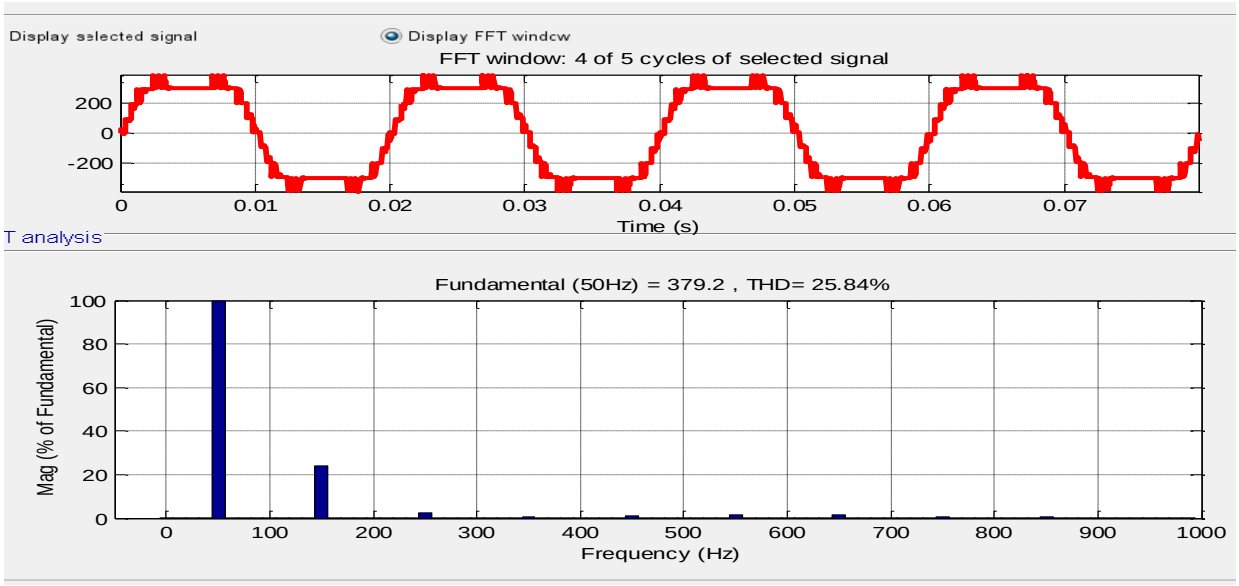

Fig. 4 Voltage wavefom for Ma=0.9,k=0.21

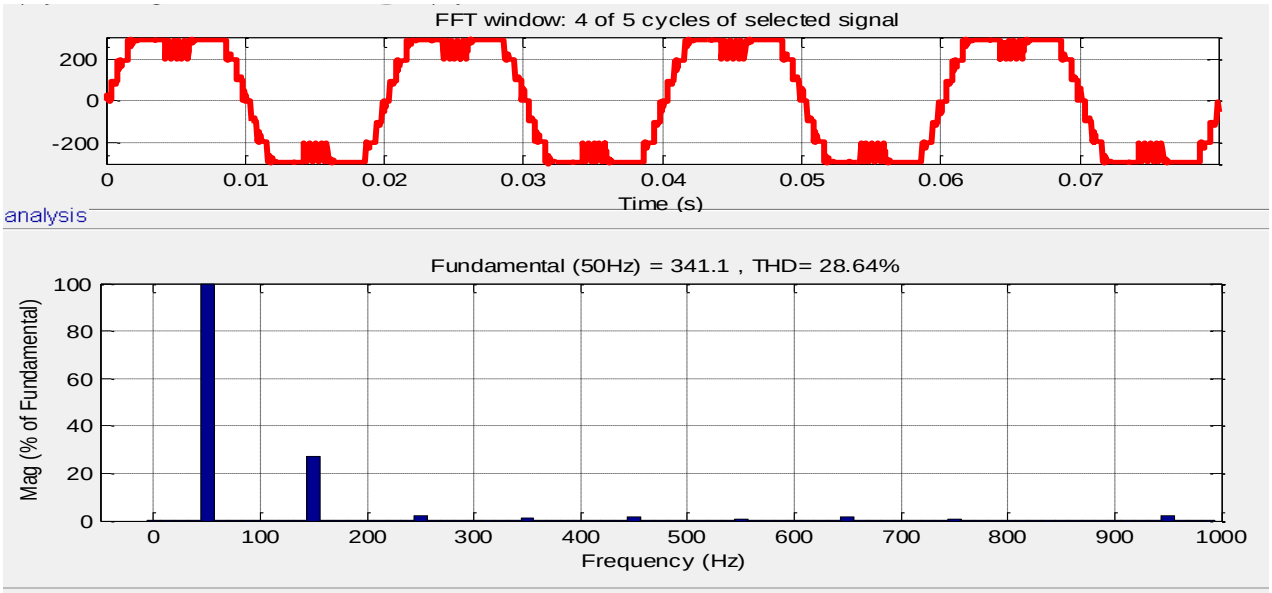

Fig. 5 Voltage wavefom for Ma=0.8,k=0.25

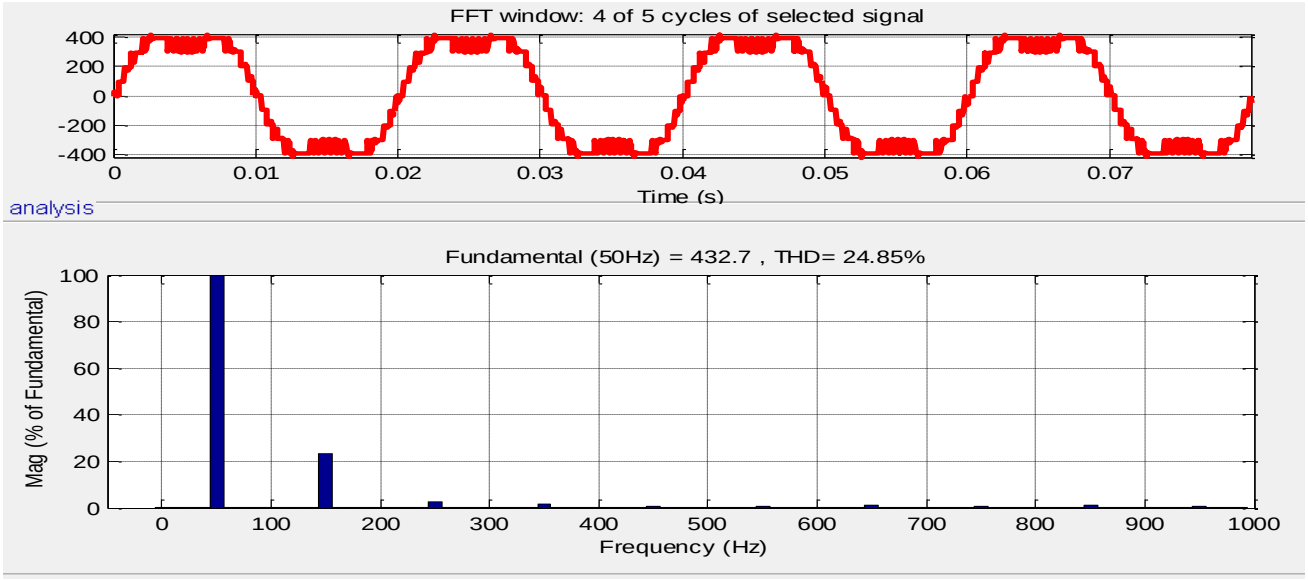

Fig. 6 Voltage wavefom for Ma=1.0,k=0.21

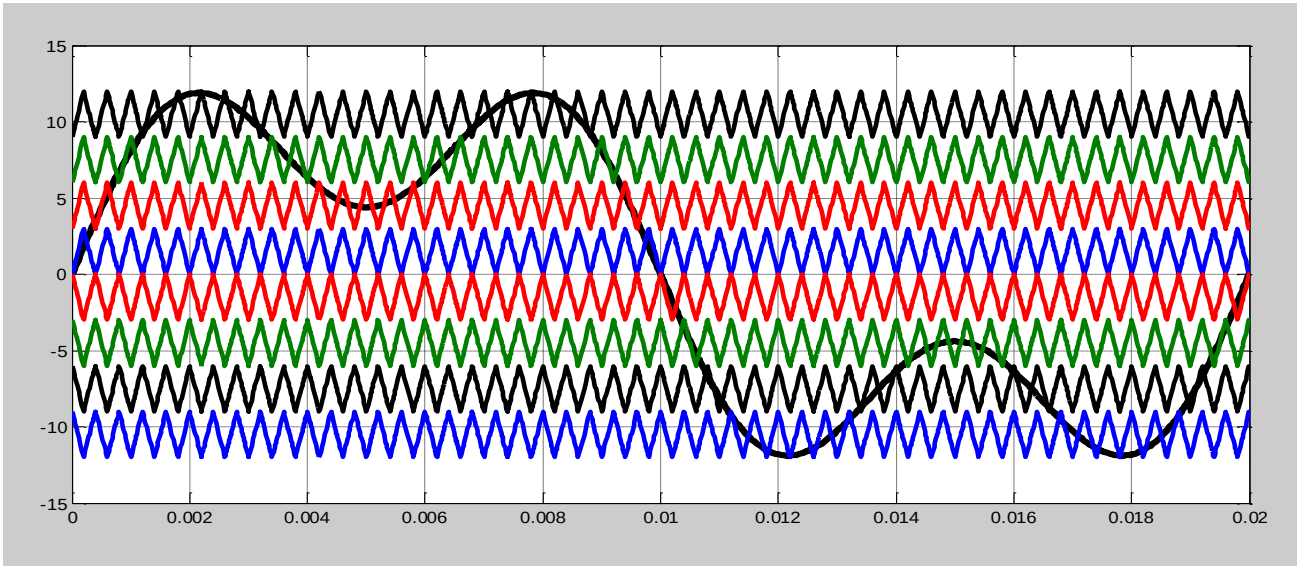

Fig. 7 carrier and refrence wave form for modulation index 1and k=0.5

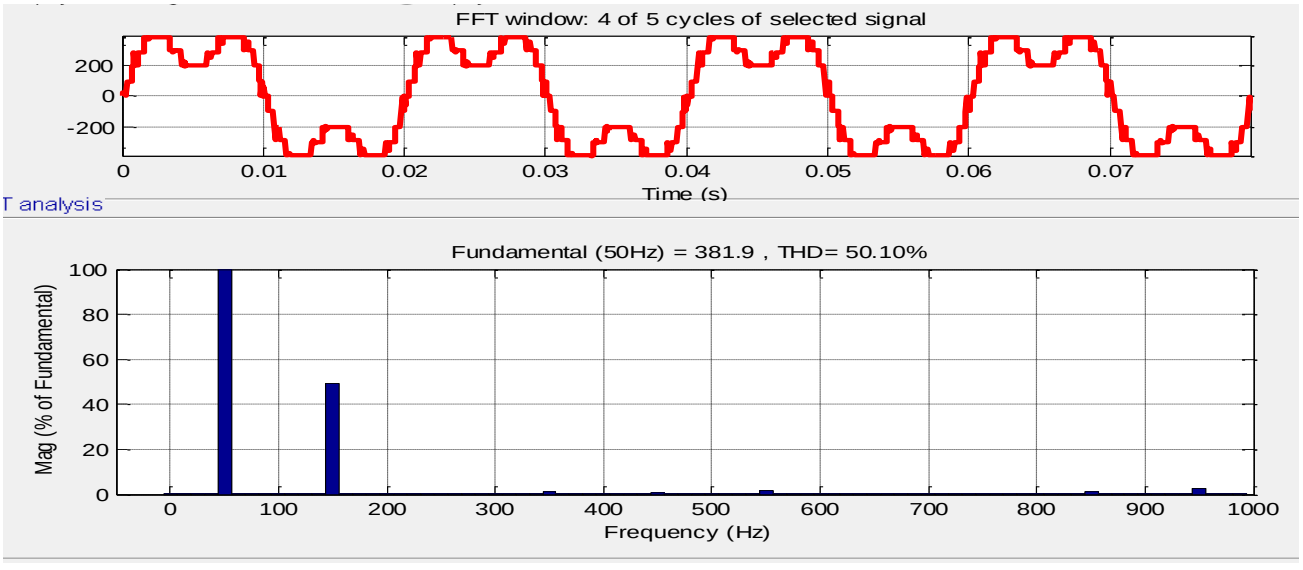

Fig. 8 Voltage wavefom for Ma=0.9,k=0.5

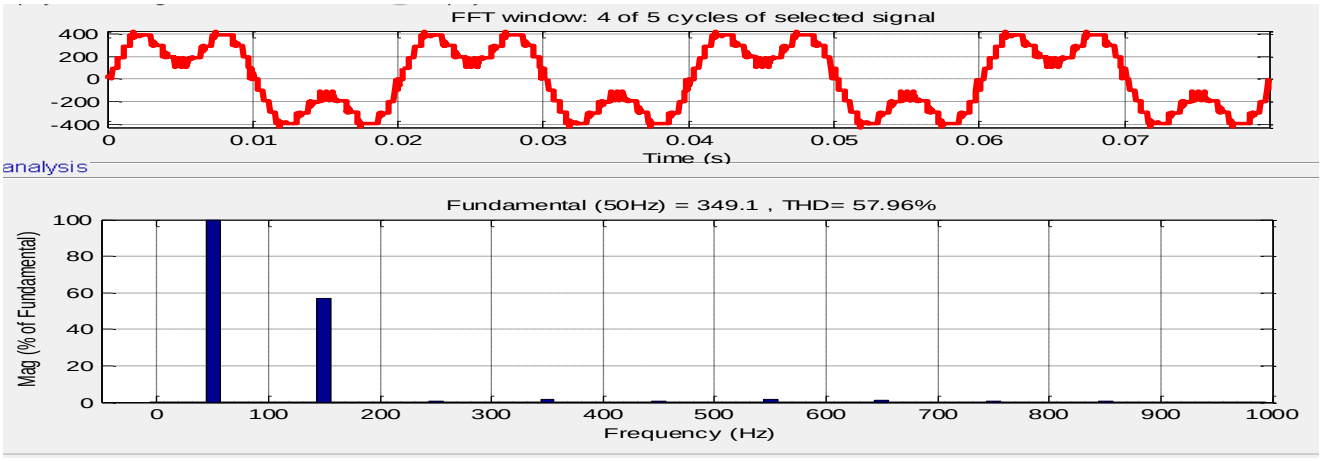

Fig. 9 Voltage wavefom for Ma=0.8, k=0.5

The simulation results for the proposed scheme has been shown for different modulation index Ma, and for different value of harmonic injection constant k. for example k=0.5 means the ratio of the injected harmonic signal to refrence is 0.5. It can be clearly observed from Fig.3 and Fig. 7 that the variation in the value of k results in a sharp dip in the peak value of modulation signal. Furthermore a decrement in rms value of fundamental component is observed at reduced modulation index , on the contrary a slight variation in THD is observed. On the other hand from Fig. 5 and Fig.9 , for ma=0.8 and k=0.25, rms fundamental value is 341.1volts and THD is 28.64%, while for the same Ma and k=0.5, rms value increses to 349.1 while THD is 57.96%. Thus it can be concluded that increase in harmonic injection magnitude k results in maximum utilisation of DC bus but at the same time also deteriotes the spectral propperties of the wave form as shown in table.1

	K=0.5		**K=0.25**	
Modulation index	**THD**	**RMS value**	**THD**	**RMS value**
Ma=0.8	57.96	349.1	28.64	341.1
Ma=0.9	50.10	381.9	25.84	379.2

V. V CONCLUSIONS

From thesimulation results it can be cocluded that harmonic injection in refrence current waveform has a significant influence on the magnitude of outvoltage and spectral properties of output voltage waveform. A proper value of k and modulation index may result in an improved perfomance in terms of THD and DC bus utilisation.

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