Design Of A Novel Energy Efficient Double Tail Dynamic Comparator

Densy T D, Sajitha A S

***Abstract*— Comparator is one of the fundamental building blocks in most Analog to Digital Converters. The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. CMOS dynamic comparator which has dual input, dual output inverter stage is suitable for high speed analog to digital convertors with low voltage and low power. Low voltage and low power consumption are the two most important parameters of the comparator which is to be used in high speed ADCs. Hence the circuit of a conventional double tail comparator is modified for low-power even in small supply voltages. Without complicating the design and by adding a few transistors at the output latch stage and input differential stage, the conventional double tail comparator can be operated with lesser power dissipation. Modification is done on the output latch stage and input differential stage. It will also reduce the delay. These energy efficient double tail comparators are very attractive for many applications such as high speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers.**

***Index Terms*— Double tail dynamic comparator, Energy efficient comparator, High speed analog to digital converters, Low power analog design.**

I. INTRODUCTION

Nowadays, operational amplifiers have great importance in high speed devices like High speed ADCs. Low power methodologies are being thrust for these high speed applications. Power consumption in these devices can be reduced by using smaller feature size processes. However, this will introduce reliability issues and the overall performance of the device will be affected. Now analog-to digital converter requires lesser power dissipation, low noise, better slew rate, high speed and less Offset. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The power consumption and speed takes major roll on performance measurement of ADCs. Dynamic regenerative comparators are being used in today's A/D converters extensively because these comparators are high speed, consume lesser power , having zero static power consumption and provide full-swing digital level output voltage in shorter time duration.

Back-to-back inverters in these dynamic comparators provide positive feedback mechanism. It converts a smaller voltage difference in full scale digital level output. However, the accuracy of such comparators are limited by an input-referred latch offset, resulting from the device mismatches such as threshold voltage, current factor $\beta(=\mu CoxW/L)$ and parasitic node capacitance and output load capacitance mismatches. Hence a new low power, high speed comparator is proposed.

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Densy T D, Electronics & Communication Engineering, Nehru College Of Engineering & Research Centre, Thrissur, India.

Sajitha A S, Electronics & Communication Engineering, Nehru College Of Engineering & Research Centre, Thrissur, India.

II. PREVIOUS WORK

The Comparator is the second most widely used electronic component. One of the fundamental building blocks in most analog-to-digital converters (ADCs) are comparators. Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small feature size. In modern CMOS processes, the threshold voltages of the devices should be scaled at the same pace as the supply voltages[1]. However, High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages. Hence, high-speed comparator design is more challenging if the supply voltage is very low. In other words, to achieve high speed, larger transistors are required in a given technology to compensate the reduction of supply voltage. It means that more area and power is needed. Also, low-voltage operation results in limited range of common-mode input voltage. It is important in many high-speed ADC architectures, such as flash ADC. Many techniques, such as supply boosting methods [2], [3], techniques employing body-driven transistors [4], [5], current-mode design [6] and those using dual-oxide processes, have been developed to meet the challenges in low-voltage design. These are effective techniques, but they introduce reliability issues.

Apart from technological modifications, new circuit structures have been developed which is preferable for low-voltage operation. It avoids stacking of more transistors between the supply rails. But they should not increase the circuit complexity. In [7]-[9], additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The structure of double-tail dynamic comparator first proposed in [10] is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. In [11], a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures.

Based on the double-tail structure proposed a new dynamic comparator is presented, which does not require boosted voltage or stacking of more transistors. By adding two pairs of minimum-sized transistors to the conventional double-tail dynamic comparator results in considerable power savings and less delay when compared to the conventional dynamic comparator and double-tail comparator. Modification is done on the output latch stage and on input differential stage. These energy efficient comparators are very attractive for many applications such as high speed ADCs, memory sense

amplifiers and data receivers.

A. Double Tail Dynamic Comparator

Clocked regenerative comparators have found wide applications in many high-speed ADCs. Due to the strong positive feedback in the regenerative latch they can make fast decisions. Many comprehensive analyses have been done by different authors, which investigate the performance of these comparators from different aspects.

The schematic diagram of the conventional double tail dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1.

The operation of this comparator is as follows. When CLK is zero, the tail transistors Mtail 1 and Mtail 2 are off. M3 and M4 pulls both fn and fp nodes to VDD. Intermediate stage transistors, MR1 and MR2 reset both output nodes to ground. During comparison phase CLK is VDD. Mtail1, and Mtail2 are on, transistors M3 and M4 turn off. Thus, fn and fp start to discharge with different rates according to the input voltages INN & INP. Suppose VINP > VINN, then fn discharges faster than fp, since M2 provides more current than M1.

As soon as the comparator detects that one of the fn/fp nodes is discharging faster, the intermediate stage formed by MR1 and MR2 passes the voltage difference to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

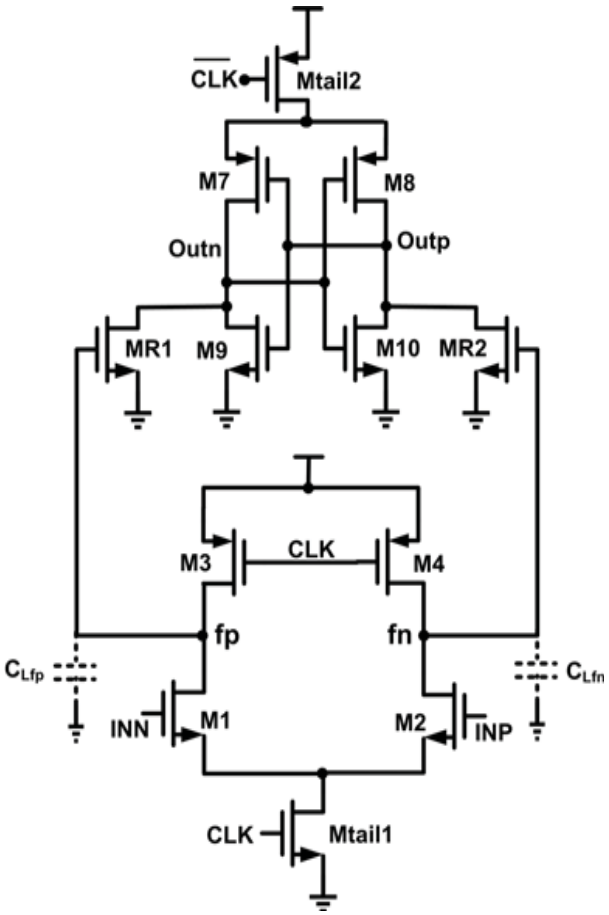

Fig -1. Double tail dynamic comparator

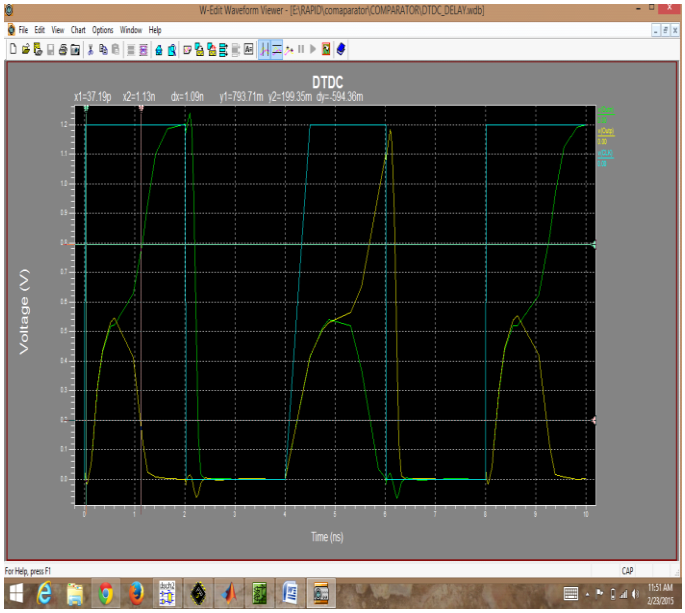

Fig -2. Transient simulation of double tail dynamic comparator

Since here fn discharges faster than fp MR2 will be off while MR1 is on. So Outn goes to low. Hence M8 turns on and Outp goes to VDD. Then M9 will be on and Outn remains low.

Transient simulation of double tail dynamic comparator is shown in Fig. 2. The delay of this comparator is obtained as 1.02nS. The power consumption is obtained as 150 µW.

The main draw back of this comparator is the power consumption. It is obtained as 150 µW .The delay is reduced compared to single tail dynamic comparator, but at the expense of increased area and power consumption. In this comparator, both intermediate stage transistors MR1 & MR2 will be finally turned-off, since fn and fp nodes both discharge to the ground. Hence it will affect the effective transconductance of the latch. Besides, during reset phase, fn & fp nodes have to be charged from ground to supply voltage VDD, which means increased power consumption. The following section describes how the proposed comparator improves the power delay product of the double-tail comparator from the above points of view. Also the dynamic mismatch from the unbalanced parasitic capacitances on the output nodes of the latch causes the additional offset term during evaluation phase. These mismatches such as parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators. A new energy efficient comparator is proposed in order to reduce power consumption and delay.

III. PROPOSED METHOD

The comparator design is largely depends on the target application. The power consumption is the most important issue in the present scenario. Hence the existing system is modified for low power consumption. Due to the better performance of double tail architecture in low voltage applications, the proposed comparator is designed based on the double tail structure.

Without complicating the design and adding few more transistors it can be operated with lesser power dissipation. Based on double tail structure proposed, a new dynamic comparator is presented which does not require stacking of

too many transistors. By adding a few minimum sized transistors to the existing comparator results in considerable power savings.

Modification is done on the output latch stage and on the input differential stage as in Fig 3.

A. *Operation of the Proposed Comparator*

The operation of the proposed comparator is as follows. It has got two operating phases: reset phase and comparison phase. During reset phase, CLK = 0, the tail transistors Mtail1 and Mtail2 are off , and static power consumption is reduced. M3 and M4 pulls both f1 and f2 nodes to VDD. So transistors MI1 and MI2 are on. Intermediate stage transistors, M5 and M6, reset both latch outputs to ground.

During comparison phase, CLK = VDD, Mtail1, and Mtail 2 are on. Transistors M3 and M4 will be turned off. At the beginning of the comparison phase, since f1 and f2 are about VDD, the control transistors are off . Thus, f1 and f2 start to discharge with different rates according to the input voltages. Suppose IN2 > IN1, thus f1 discharges faster than f2. As long as f1 continues falling, the corresponding pMOS control transistor that is MC1 starts to turn on, pulling f2 node back to the VDD. Hence control transistor MC2 remains off, allowing complete discharge of node f1. In conventional double-tail dynamic comparator, ΔVf1/f2 is just a function of input transistor, transconductance and input voltage difference. In this structure as soon as the comparator detects that for instance node f1 discharges faster, a pMOS transistor (MC1) turns on, pulling the other node f2 back to the VDD. Therefore by the time passing, the difference between f1 and f2 increases. It leads to the reduction of latch regeneration time.

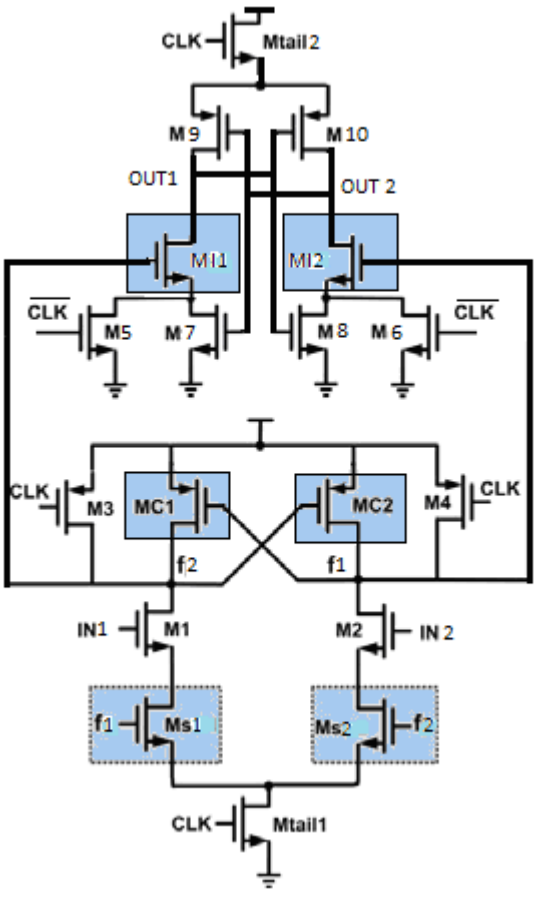

Fig -3. Proposed Energy Efficient Comparator

Since f1 is low, MI2 will be off and therefore out2 remains low. f2 is at VDD. Hence MI1 turrns on. Since out2 is low, M9 will be on and out1 goes to VDD. Two nMOS switches are used below the input transistors to reduce static power consumption.

B. *Control Transistors*

The main idea of the proposed comparator is to reduce the latch regeneration time thereby decreasing delay. So ΔVf1/f2 is to be increased. For this purpose two control transistors (MC1 and MC2) are added to the input stage in parallel with the transistors M3 and M4, but in a cross coupled manner. As soon as the comparator detects that one of the f1/f2 nodes is discharging faster, control transistors will try to increase their voltage difference. Suppose f1 discharges faster than f2. As long as f1 discharges continuously, the corresponding control transistor MC1 starts to turn on, pulling f2 back to VDD. So control transistor MC2 remains off, allowing the complete discharge of f1. After some time the difference between f1 and f2 increases in an exponential manner. As a result, the latch regeneration time decreases. Thus control transistors help in increasing latch regeneration speed and thereby decreasing the delay.

C. *Switching Transistors*

The purpose of the switching transistors MS1 & MS2 is to reduce the static power consumption. When one of the control transistors (Mc1) turns on, a current from VDD is drawn to the ground via input transistor M1 and tail transistor Mtail1. This will result in static power consumption. To compensate this, two nMOS switches MS1 & MS2 are added below the input transistors. Suppose that f2 is pulling up to the VDD and f1 should be discharged completely, hence the switch in the charging path of f2 will be opened. It will reduce any current drawn from supply voltage. The switch connected to f1 will be closed to allow the complete discharge of f1 node. In other words, the operation of the control transistors with the switches emulates the operation of the inverter. The delay and energy per conversion of this comparator is reduced to a great extent in comparison with the conventional dynamic comparator.

D. *Intermediate Stage Transistors*

In order to reduce the dynamic power consumption two transistors (MI1 and MI2) are added in the output stage. These transistors are used to couple the input differential voltage to the output latch stage.

The power consumption is badly affected by the capacitance as per the following equation.

$$P = C_L V^2 dd\ f \quad (1)$$

P is the power consumed, CL is the load capacitance, V dd is the supply voltage and f is the clock frequency. Parasitic capacitance (mainly drain diffusion capacitance) on the output node has a great influence on the load capacitance. If a transistor in the stack is not switched off , that transistor must be considered in determining the total node capacitance. While determining the node capacitances, a transistor that turned on can be viewed as a piece of interconnect. Gate and diffusion capacitances must then be included as a part of the internal node capacitance.

Typically, each internal node consists of the diffusion that is shared by source and drain of the adjacent transistors. Only overlap capacitance is included in the gate to diffusion coupling.

In the conventional comparator, three transistors (M5, M10 & M7) are simultaneously on at the output node if IN2>IN1. So we have to consider the parasitic capacitance of that transistors in determining the total node capacitances. Here in the proposed method, either MI1 or MI2 will be turned off. Since gate of this transistor is capacitively coupled to nodes above and below due to gate overlap capacitance, the voltage of both nodes are pulled down somewhat. Also MI1 isolates M5 and M7 from the output node out1. MI2 isolates M6 and M8 from out2 node. Thus the parasitic capacitance at the output node decreases and the power consumption is reduced to a great extend.

By modifying the output latch stage during reset phase (clk=0V), the drain diffusion capacitance is reduced by a significant amount. Also the switching transistors helps in reducing static power consumption. Therefore, the modified energy efficient comparator can be operated at less power consumption and delay than the previous comparators.

IV. Simulation Results

In order to compare the proposed comparator with the conventional double-tail dynamic comparator, all circuits have been simulated in a 250nm CMOS technology with VDD = 1.2 V. The simulation parameters have been analyzed with the help of the Tanner EDA tool.The schematic is drawn using S-Edit. Pre-layout simulation is performed using T-Spice simulator. Waveform is analysed using W-Edit. Power and delay is calculated using this tool. Transient simulation of proposed energy efficient comparator is shown in Fig 4.

Simulation results are shown in the following table. In the proposed system power consumption is reduced considerably. The power consumption is obtained as 52.2µW. Comparing with the existing system 65.2 % of power reduction can be

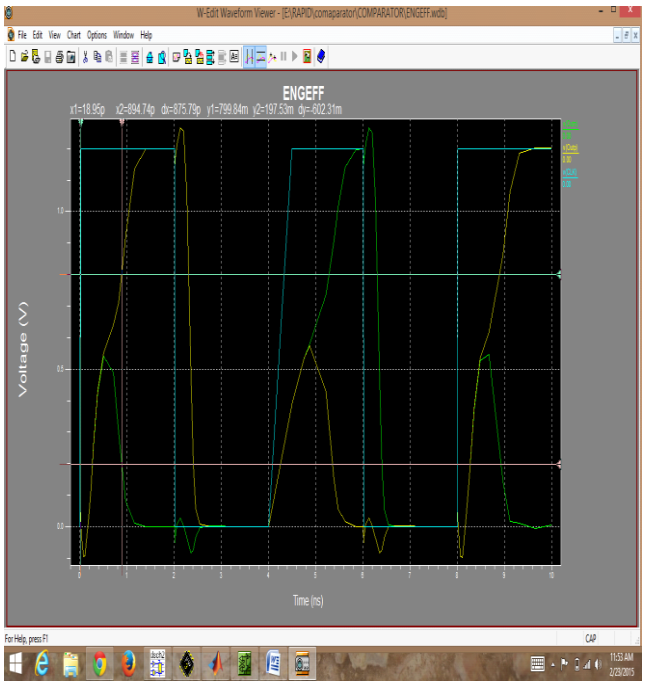

Fig -4 . Transient simulation of energy efficient comparator

Table –I. Performance comparison

Comparator structures	Parameters	
	Power(µW)	Delay(nS)
Double-tail Dynamic Comparator	150	1.02
Proposed Energy Efficient Comparator	52.2	0.802

achieved. The delay is obtained as 0.802nS. That is, there is a reduction of 21.4% in delay. Hence the proposed comparator is both energy efficient and delay efficient.

V. Conclusion

A new energy-delay efficient double tail dynamic comparator is proposed in this paper. It uses positive feedback mechanism with lower power consumption than conventional dynamic comparators. Low power and high speed are the two most important parameters of the comparators that are used in high speed ADCs. These comparators are targeted mainly for ADC applications. By adding a few minimum sized transistors to the existing system results in considerable power saving and delay saving. Though proposed comparator has highest number of transistors but it still consumes low power. The proposed comparator has got high speed with a 20% of reduction in delay. It can be concluded that the new energy efficient comparators are very attractive for many applications such as high speed ADCs , memory sense amplifiers and data receivers.

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Densy T D completed her B.Tech in Electronics & Communication Engineering from IES college of engineering, Thrissur, Kerala in 2010. She is currently pursuing the M.Tech in VLSI Design from Nehru college of engineering & research centre, Thrissur, Kerala. Her current research interests include low power, digital integrated circuits, CMOS VLSI design etc.

Sajitha A S had completed diploma in electronics Engineering from Govt.polytechnic, kothamangalam, Kerala in 2004. She had completed graduation in Electronics & Communication from institution of engineers in India in 2007. She completed her M.Tech in Embedded system,from amrita viswa vidhyapeetham,Ettimadai,coimbatore in 2010. Currently she is working as Asst.professor, in Nehru college of engineering & research centre, Thrissur, Kerala.Her area of interests include vlsi & Embedded Systems