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A Survey: To Design Low Noise Digital Decimation Filter for Sigma-Delta-ADC

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***Abstract*— This paper focused on the low noise digital decimation filter design techniques categorized as sigma-delta modulation based on word length. The general purpose DSP applications include classical LMS algorithms reported using sigma-delta modulator A single bit sigma-delta A/D converter with medium oversampling ratio for the processing of audio ,seismic and biomedical signal. A second-order single-stage sigma-delta modulator single bit quantize signal with oversampling ratio 96.Finaly a low noise filter discussed and compare order of modulator and decimation.**

***Index Terms*— oversampling,downsampling, quantization noise,noise shaper , decimation filter, CIC compensation filter.**

I. INTRODUCTION

There is no surprises that more task are accomplished in the Digital signal processing(DSP). Filter required large number of accumulator and multiplier in per sampling period. The alternate solution is Field Programmable Gate Arrays (FPGA) for digital filter task. The design for ADC the nyquist rate is $fs \geq 2*f_b$,where f_b is the high frequency component of the input signal and f_s is sampling frequency.To insure the filter the signal component about fs/2 to avoid aliasing must have very narrow transition band[1].The resolution of Nyquist rate conversion is low which is not suitable for every low signal voltage conversion. Oversampled ADC is preferred over nyquist rate due to high SNR (Signal to noise ratio) and high resolution[2].Here sigma delta modulator behave like noise shaper and digital decimation filter and CIC compensator filter are also used to remove band quantization nose ensure much higher SNR.

Some obvious applications that require fast and efficient digital filters are decimation filters, audio filter and software defined radio, so this requires high throughput. To achieve fast, noiseless and efficient implementations,various techniques are proposed. Reducing the complexity of the multiplier is to reduce the word length in both the input and the filter coefficient. This paper also focuses on these methods. To improve the efficiency of the digital filtering operations here many techniques are used in form of Sigma-Delta modulation like.We examine the synthesis and design of such techniques including general purpose short word length (SWL) DSP in this paper. The design focused on the off chip digital decimation filters for single bit sigma-delta A/D converter with medium over sampling ratio. To reduce hardware requires, multiplier less FIR filter architecture are used[3].The anti aliasing filter must have a very narrow transition band which is not easy to realize. Also the resolution of Nyquist rate converter is low which is suitable for a very low voltage converter.thus the reducation in base band quantizing noise is equivalent to increasing the effective resolution of the digital output. It is reduce by using CIC compensation filter design[4].

Basic of Sigma- Delta modulator- The simplest predictive modulator is the linear Delta modulator. Most of the in band noise outside signal frequency band that further improvement in the SNR it can be achieved by pushing noise to high frequency. This should be obtain only if signal transfer function is a low pass where as and noise transfer function is high pass[5]. This technique is called noise shaping and can be easily and efficiently implemented by modifying the delta modulator. So the integration of the input signal is encoded rather than the input signal directly[6].

Clearly integration being a linear function does not affect system transfer function. The significant modification of Delta modulation system is called Sigma-Delta Modulator.In FIR filter much work on the design and implementation of the Sigma-Delta modulation in various forms. More recently sigma-delta modulation based bit stream adder and multipliers modules have been described[7,8].To perform the filtering operation full precision filter coefficient where zero padded by R to match the oversampling ratio of the sigma-delta modulator. The Decoder circuit which comprises cascade comb and base band filter where used to remove the quantization noise and aliases from the filter out put signal. However the output signal was in a multi bit format in all of these scheme[9].

Overall and efficient implementation of narrow band digital filter thorough a requantizing operation has shown a 50% reduction in logic resources as compared to traditional FIR filter implementation. Signal encoding with sigma-delta modulation work as an ADC with coder circuit because single bit coder have no longer requirement for a conventional ADC[10].There no interpolation is required in this setup as a signal passing through Sigma-Delta modulator the output of modulator is very high sampling rate. After filtering out high frequency quantization noise, it possible to reduce the sample rate by using decimation filter.

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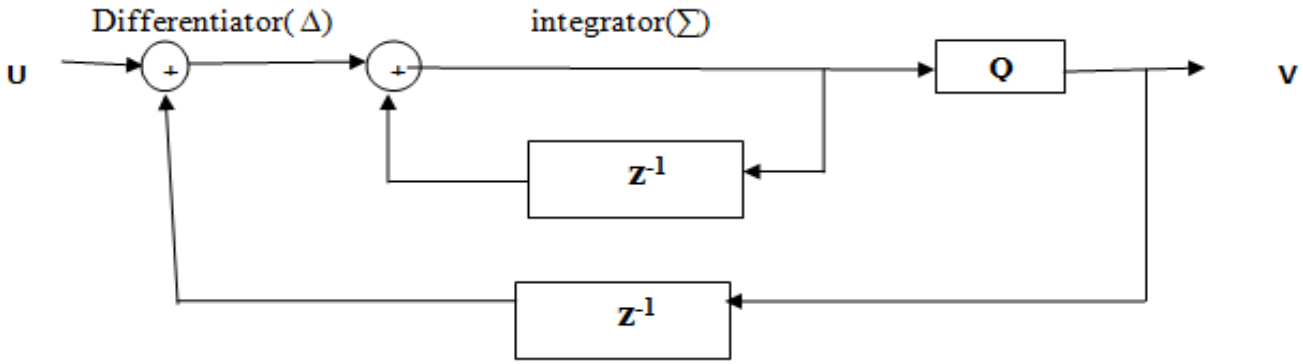

Fig.1. Block Diagram of second order sigma- delta modulator.

II. CHOICE OF FILTER TOPOLOGY –

Fall on two categories

(a)Remove Shaped Quantization Noise- Best choice of sigma-delta modulator should provide good noise shaping at low OSR.As the OSR increase, the order of filter should be increases to maintain same frequency response when sampling rate is high noise move to high frequency and most of it lies above base band[10,11]. The spectral density of noise at output of the modulator is

$$N(f)=e\sqrt{2\tau}\,(2\sin(\pi f\tau))^{l}$$

The spectral density of the decimated noise will be

$$N'(f) = e\sqrt{2\tau}\left(\frac{2\sin(\pi fN\tau)}{N}\right)^{l}$$

When this noise is equalize to compensate for the signal filtering it's become $N_0'(f) = e\sqrt{2\tau}\,(2\sin(\pi f\tau))^{l}\left(\frac{sinc(\tau f)}{sinc(N\tau f)}\right)$ $0<f<f_0$

Decimation filter attenuating noise at any high frequency noise that accompanies the signal, when it aliases baseband, here loss of resolution will be small. Decimation filter provides least attenuation for this noise.The decimation filter is the overall protection against the out-of-band noise[12]. It was found that using more than two cascaded comb filter did not improve the trade of between signal to noise rate of the coded output and the OSR. .

The decoder for this filter is used to reconstruct the original signal by resampling to the Nyquist rate and removing quantization noise by using low pass filter. The use of cascade comb filter as reported in [3] was adopted to further simplify the decoder design whilst removing any alias introduced into the system from the FIR filter. To perform the filtering operation full precision filter coefficient where zero padded by R to match the oversampling ratio of the sigma-delta modulator. Decoder circuit comprising cascade comb and base band filter where used to remove the quantization noise and aliases from the filter out put signal. However the output signal was in a multi bit format in all of these scheme.

(b)CIC Compensation Filter-The comb filter operation is equivalent to rectangular window finite impulse response filter (FIR). The comb filter must be used more additional digital filter stages.

A comb filter of length N is a FIR filter with all N coefficients equal to one. The comb filter transfer function is

$$H(Z)=\frac{Y(Z)}{X(Z)}=\sum_{N=0}^{N-1} Z^{-N}$$

..... (1)

in the discrete time domain for N=4

$$y(n)=x(n)+x(n-1)+x(n-2)+x(n-3)$$

Now from equation (1)

$$H(Z)=1+Z^{-1}+.....+Z^{N-1}$$

$$\frac{Y(Z)}{X(Z)}=\frac{1-Z^{-N}}{1-Z^{-1}}$$

$$Y(Z)=X(Z)\left[\frac{1}{1-Z^{-1}}\right]\left[1-Z^{-N}\right] \quad .....(2)$$

$$H(Z)=H_1(Z)Hc(Z)=\frac{Y(Z)}{X(Z)}$$

…… (3)

Where $H_1(Z) = \left[\frac{1}{1-Z^{-1}}\right]$ and

$H_c(Z) = \left[1-Z^{-N}\right]X(Z)$

We generalize equation number (3) for M number of integrator comb filter pairs, and R is the rate change factor. The equivalent time domain impulse response of CIC filter can be viewed as a cascade of M rectangle pulses. Each rectangular pulse has rn taps. Then equation (3) becomes

$$H(Z)=\frac{Y(Z)}{X(Z)}=H_1^M(Z)*H_C^M(Z^R) \quad .. (4)$$

The CIC filter frequency response does not have a wide and sharp flat pass band. To overcome the magnitude drop, a FIR filter that has a magnitude response that is the inverse of the CIC filter can be applied to achieve frequency response correction filters called compensation filter. Compensation filter used for down convertor follows the CIC filter. This filter always operates at the lower rate in a rate conversion design.Now, since the comb filter will be followed by an decimator, the differentiation function can be done at the lower rate.

Highly symmetric structure of a CIC filter allows efficient in

hardware but its pass band is not flat.This problem can be alleviated by a compensation filter.The method for designing CIC compensating filters sample rate conversion system.The MATLAB signal processing Toolbox is used to design the cofficents of the compensation FIR filters.The magnitude response of an N-stage CIC filter at high frenquency(f_s).

$$|H_1(f)|=\left|\frac{\sin(Nf\pi)}{\sin(\frac{\pi f}{R})}\right|^N \quad \text{.....(5)}$$

for large number of stage ,the CIC filter frequency response does not have a flat,wide pass band.to Overcome the amplitude droop,a filter that has aamplitude response which is the inverse of the CIC filter and can be applied to achieve frequency response correction is called a CIC compensation filters.To achieve a more efficient hardware solution the compensation filter operates at the lower in a rate conversion design.Amplitude response of the compensation filter is the inverse of CIC is[4,13].

$$|H_C(f)|= \left|MR\frac{\sin(f\pi/R)}{\sin(\pi Mf)}\right| =\left|\frac{\pi Mf}{\sin(\pi Mf)}\right|^N =|\text{sinc}^{-1}(Mf)|^N$$

.....(6)

The H(f) of the casecade CIC and compensatation filter are

$$H(f)= H_1(f).H_C(f) \quad \text{.....(7)}$$

That is more time sharing in the compensation FIR filter to achieve a flat pas band, the compensation FIR filter should have a magnitude response is the inverse of CIC FIR filter.When R is large the compensation filter response can be approximated by the inverse sinc function,so the compensation filters sometimes to as the 'inverse sinc' filter.If R is change the compensation filter are also a multi-rate filters. Also in CIC and compensation demonstrate of choosing pass band width on noise amplification in the stop band. Choice of pass band width is important when desiging the CIC filter and compensation filter cascade. The pass band edge to be less than a quarter of the null on the low frequency scale.The solution of filter stage is multiple decimation stages, and it is decimated by 4 and CIC filter is followed by a compensation FIR filter that imppinted additional decimation by-2[4,14].

III. SUMMARY

In this survey work on efficient low noise filter design by employinSigma-Delta modulator. A single bit signal processing technique are used is known as SWL[15]. In synthesized hardware efficient and single bit FIR filters.The work provides an important analysis of the relation between oversampling ratio,signat-to-noise ratio,resister size(bit),order of decimation filter and modulator.Noise and buffering problem is reduces in concept of paper and using CIC compensation filter[4,13].

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