A Comparative study on Bulk PMOS resistive load inverter and Double gate PMOS resistive load inverter

Sima Baidya, Arindam Chakraborty

Abstract— **Double-gate symmetric FinFET technology has been proposed as promising alternative for bulk MOSFET technology. Scholars have studied the performance or power advantages of FinFET circuits over Bulk MOSFET circuits. In this work focus on the comparative study between a bulk pmos resistive load inverter and Double Gate PMOS resistive load inverter in 45nm technology have been concentrated. The simulation have been done using cadence virtuoso and the results are compared. Double Gate PMOS inverter 45nm exhibits better delay performance than the bulk pmos inverter. The results and discussion stated validate that FinFET based circuit is more robust than bulk MOSFET.**

***Index Terms*—Bulk PMOS, Double Gate PMOS, Fall Delay, Rise Delay, VTC**

I. INTRODUCTION

It have been studied by the scholars that scaling of bulk MOSFET beyond 45nm is severely restricted by short channel effects and vertical gate insulator tunneling, but in case of double gate FinFET technology the limitation have been eradicated for which it is the promising alternative for bulk MOSFET, and for the above reasons scaling technology of DGPMOS have been done in this work. In this work analysis of performance and delay of DGPMOS inverter over Bulk PMOS inverter have been focused. Research in differential switched capacitor circuit presented on a single monolithic wide band VCO for Multi standard radios and verified in a fully integrated CMOS VCO [1]. The area of research was restricted to low-power analog circuits for DG MOSFET, and focused light voltage control on the bottom gate [2].

Research on delay and power dissipation of a (CMOS) buffer driven interconnected load in sub-threshold regime of operation on three technologies 130, 90, and 65nm which shows operation of transistor in the sub threshold region in order to analyze the delay and power dissipation [3]. The impact of channel material engineering on the performance of silicon-on-nothing (SON) architecture for 32nm technology node. The analog performance of SON architecture in terms of drive current I , transconductance (g), early voltage V , transconductance generation efficiency, and output resistance with different channel material, i.e., Si, SiGe, Ge, GaAs, and InP has been investigated by using ATLAS 3D device simulation by Kumari, V[4]. Devi Tejashwini, G have proposed the design and performance of basic Digital (AND, OR, NAND, NOR, XOR, XNOR, NOT, Half Adder) and Analog (Current Mirror, Cascode Current Mirror, Comparator) circuits on 20nm FinFET technology, widths of NMOS and PMOS have been varied and low voltages, better results of power performance had been observed in both digital and analog circuits using FinFET technology [5].

Scholars have concentrated on CMOS technology for its better performance perhaps its manufacturing cost is more, so for overcoming this manufacturing cost bulk PMOS was introduced. In case of bulk PMOS the delay performance doesn't satisfy the need, but whereas implementing Double Gate PMOS it had been observed that the performance and the manufacturing cost both can be rectified and satisfied so the comparative study flash on Double Gate PMOS performance over Bulk PMOS.

II. FINFET STRUCTURE

When a MOSFET consist of gate more than one in a single device is referred as a multigate device or multiple gate field effect transistor. Multiple gates can be controlled by single gate electrode or by independent gate electrode, in case of single gate electrode the multiple gate surface acts electrically as single gate. Since the inception of the integrated circuit industry, market have not changed the design metrics like performance, power, area, cost and time perhaps as the process technology shrinks continuously its getting impossible to achieve a similar scaling of certain device parameter so an alternative have been introduced that is FinFET(Fin Field Effect Transistor) as compared to planner technology. As the new technology promises to have much better performance at the same power budget or equal performance at a much lower power budget and at minimum delay.

The Berkeley team proposed two possible structures shown in Fig 1 and Fig 2 that is ultra thin body and double gate to be more precise this is the thin body MOSFET which are the origin of today's FinFET transistors which would control short channel effect and suppress leakage by keeping the gate capacitance in closer proximity to the whole of the channel.

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Sima Baidya, Sima Baidya, Heritage Institute of Technology, Kolkata, India,9933914000.

Arindam Chakraborty, Arindam Chakraborty, Dr Sudhir Chandra Sur Degree Engineering College, Kolkata, India,8420035594.

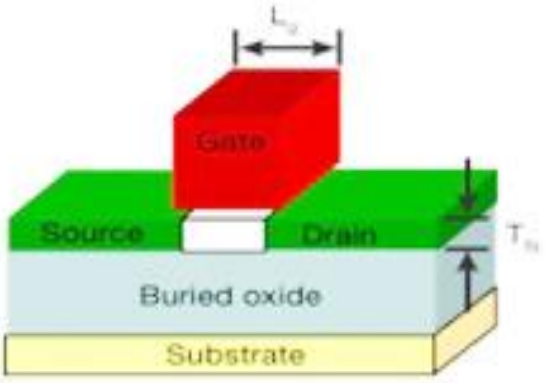

Fig1: Ultra Thin Body (UTB)

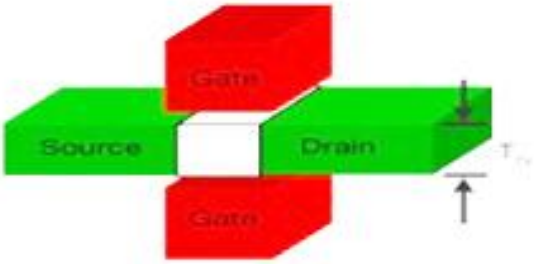

Fig 2: Double Gate (DG)

Double Gate MOSFET abbreviate to DGMOSFET are of two types. Fig 3 shows the flowchart of division of the DGMOSFET technology. There are two modes of operation three terminal and four terminal (independently driven) mode, in case of three terminal mode two gates are electrically connected and switched simultaneously where as in four terminal mode two gates are biased differently with only one gate switching. This results depicts that there is a disadvantage from the fixed second gate voltage that is four terminal driven DGMOSFETs exhibit non-ideal threshold slope, it is due to the potential across the silicon film does not move entirely to the switching gate if the potential of non-switching gate is fixed. Perhaps the four terminal driven DG MOSFET also shows worse short channel effect than the commonly used three terminals driven DG MOSFET

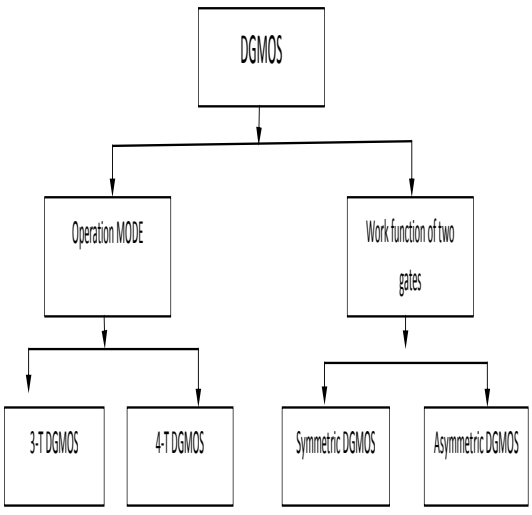

Fig 3: Classification of DGMOSFET

III. Modeling of Symmetric Gate DGPMOSFET and Implementation with Verilog-A

As designers need compact models to design circuits they implemented double gate MOSFET (DGMOS) architecture with tied driven gates. The physical models are basically in non-optimized form so the computing time is very significant from a circuit designer's perspective. There are various methods of modeling a MOS transistor. The model is written in Verilog –A language to make it compatible with spice simulator.

A. Long Channel model

In 1966 Pao-Sah's double integral of drain current proposed[6] for bulk MOSFET s as it consists of both drift and diffusion currents and thus is valid and accurate in all operating regions. But analytically it cannot be carried out as this has to be done in presence of both the depletion and mobile charges. All current models including the BSIM, PSP[] and HiSIM[6] models of bulk MOSFETs are based on the charge sheet approximation.In contrast to bulk MOSFETs, depletion charges are negligible in DG MOSFETs since the silicon film is undoped. Thus, only the mobile charge charges term needs to be included in poisson's equation. As a result, the exact solutions to poisson's and current equations based on gradual channel approximation can be derived without the charge sheet approximation.

B. Analytical drain current model

Poisson's equation along a vertical cut perpendicular to the Si film takes the following form, for an undoped symmetric DG MOSFET shown schematically with only the mobile charge (electrons) term:

$$\frac{d^2\Psi}{dx^2} = \frac{q}{\varepsilon_{si}}\eta_i e^{\frac{q(\psi - V)}{KT}} \quad (1)$$

Where q = The electronic charge

ε_{SI} = The permittivity of silicon

η_I = The intrinsic carrier density

$\psi(x,y)$ = The electrostatic potential defined as a intrinsic level referenced to the Fermi level of the source

K=Boltzmann's constant whose value is 1.380648 x 10^{-23} JK^{-1}

T = temperature in Kelvin;

V = The electron quasi-Fermi potential which varies from source voltage V_s to the drain voltage V_d and independent of x

$$\psi(x) = V - \frac{2KT}{q}\ln\left[\frac{t_{si}}{2\varepsilon_{siKT}}\cos\frac{2\beta x}{t_{si}}\right] \quad (2)$$

Where β=a function of y (independent of x) to be determined from the boundary condition.

$$\frac{q(Vg - \Delta\phi - V)}{2KT} - ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}\,KT}{q^2\eta_i}}\right] = ln\beta - ln[cos\beta] + 2r\beta tan\beta \quad (3)$$

Where $r = \frac{\varepsilon_{si}\,t_{ox}}{\varepsilon_{ox}\,t_{si}}$

Replacing V as Vs for source and Vd for drain for which equation (3) gives the result βs to βd respectively. So the drain current is

$$I_{ds} = \mu\frac{W}{L}\frac{4\varepsilon_{si}}{t_{si}}\left(\frac{2KT}{q}\right)[g_r(\beta_s) - g_r(\beta_d) \quad (4)$$

For source $\beta = \beta_s$ and for drain $\beta = \beta_d$

I_{ds} is the analytical drain current for a tied gate symmetrical DG MOSFET.

C. Short channel model

The long channel core model is only validate till the device dimensions are sufficiently large but as the channel length becomes shorter short channel effects have to be included in to the long channel core model. Short channel MOSFETs shows lower threshold voltage and larger sub threshold swing than long channel devices. The carrier velocity in a short channel DG MOSFET tends to saturate at a much lower drain voltage, which causes the saturation current to deviate from 1/L dependence. In the saturation region, the saturation current of a short channel DG MOSFET increases with the drain voltage more rapidly than long channel devices

D. Short channel effect

The short channel effect as an indicator of devices scalability [8], is the leading factor that limits how far DG MOSFET can be scaled. Numerical simulation have shown that DG MOSFETs have better short –channel effects and therefore can be scaled to shorter channel length than bulk MOSFETs[9]. The model includes. The current equation in the sub threshold region is derived, and then the threshold voltage roll-off and DIBL.

- *Subthreshold current solution*

As the mobile and fixed charges are negligible for their little effect on the threshold voltage of an undoped DG MOSFET in the sub-threshold region [10], the Poisson's equation becomes Laplace equation in both the silicon and insulator regions. Solution of this 2-D potential expression had done in [10]

$$\psi(x,y) = \left[\frac{\Delta\varphi_1 - \Delta\varphi_2}{t_{si} + 2t_i\frac{\varepsilon_{si}}{\varepsilon_i}}x + V_g - \frac{\Delta\varphi_1 + \Delta\varphi_2}{2} + \frac{b_1 \sinh\left[\frac{\Pi(L-y)}{\lambda_1}\right] + c_1 \sinh\left[\frac{\Pi y}{\lambda_1}\right]}{\sinh\left[\frac{\Pi L}{\lambda_1}\right]}\cos\left(\frac{\Pi x}{\lambda_1}\right)\right]$$

Where φ_1 & φ_2 = work function of two gates of DGMOSFET for symmetric work $DG\ \Delta\varphi_1 = \Delta\varphi_2$.

Other parameters are $b_1 = B\left(\frac{E_g}{2q} + \frac{\Delta\varphi_1+\Delta\varphi_2}{2} - V_{g0}\right)$

$c_1 = B\left(\frac{E_g}{2q} + V_{ds} + \frac{\Delta\varphi_1+\Delta\varphi_2}{2} - V_{g0}\right)$

Where $B = \frac{2\lambda^2 \tan\left(\frac{\Pi t_i}{\lambda_1}\right)\sin\left(\frac{\Pi t_{si}}{2\lambda_1}\right)}{\Pi^2 t_i[\frac{t_{si}}{2} + \frac{t_i \sin\left(\frac{\Pi t_{si}}{\lambda_1}\right)}{\sin\left(\frac{2\Pi t_i}{\lambda_1}\right)}]}$

λ_1 is the scale length that can be expressed as the function of ratio $K = \frac{\varepsilon_{si}}{\varepsilon_i}$.

As the insulator is silicon dioxide (ε_i=3.9) the function is

$\lambda_1 = (K^4 + 23.98K^3 + 219.8K^2 + 96.18K + 15.98)^{\frac{1}{4}}\, t_i$

- *V_t roll off and DIBL effect*

The threshold voltage shift ΔV_t is extracted from the parallel shift of $I_{ds} - V_g$ curves of short channel device with respect to the long channel device at the same current level normalized to $\frac{W}{L}$. At the direction of channel the drain current is largely controlled by the point of maximum electron energy barrier(maximum potential) at y_c, this point obtained by $\frac{d\psi(x,y)}{dy}|_{y=y_c} = 0$. At the direction of x it is controlled by the largest resistance point (minimum potential) at x_c. x_c=0 for the symmetric DG MOSFET .ψ(x,y) spatially varies stringly in the y direction than that in the x direction, we take Taylor expansion of ψ(x,y) in the direction at (x_c, y_c).

E. Velocity saturation effect

At low lateral electric field, the velocity of the carrier v is proportional to the both electric-field E_y and carrier mobilityμ_{eff}. But when the lateral electric field insufficiently high, carrier velocity is no longer proportional to the electric field and tends to saturate due to the increasing phonon-scattering encountered by carriers. The velocity and electric field relationship takes the following empirical form which is valid at low and high electric field.

$$v = \frac{\mu_{eff}E_y}{[1 + (\frac{E_y}{E_c})^{\alpha}]^{1/\alpha}}$$

Where E_c = the critical field at which the velocity saturates α=fitting parameter indicating how rapidly the carrier velocity approaches saturation. Experimental data show α=1 for electrons and α=2 for holes. But to conserve symmetric property generally we take α=2. An approximate solution based on α=2 is thus developed to model the velocity saturation effect in DG MOSFETs[37].

$$\frac{I_{ds}(with\ velocity\ saturation)}{I_{ds}(without\ velocity\ saturation)} = \frac{1}{\left[1 + \left(\frac{V_{ds}}{E_c L}\right)^2\right]^{1/2}}$$

F. Model implementation

A number of circuit simulators such as SPICE3, cadence and ADS are available or model implantation with their own languages supported. The standard simulator for model implementation had been SPICE3 simulator since made it publicly available [11]. All the publicly released BSIM models are written in C within the SPICE3 simulator. This can be very time-consuming and prone to errors especially when the drain current or charge model is a complex function of applied voltages.

Verilog-A language is an Analog Hardware Description Language (AHDL) and was conceived as a general- purpose analog modeling language. Now a days are becoming as leading candidate for new compact model development tool [12] as an alternative to SPICE3. The increased level abstraction allows device modeling developer to focus in specific. The implementation of any model using verilog-A allows easy introduction in some SPICE circuit simulators. The T-SPICE circuit simulator links the listed in SPICE with verilog-A models for components like resistance, capacitance, inductors and transistors. Additionally, the transportability of the model is allowed. So here it have been implemented the compact model in Verilog-A language with NEWTON-RAPSON method of solving nonlinear equation. After model implementation symbols of PMOS is generated as shown in the Fig 4 and Fig 5

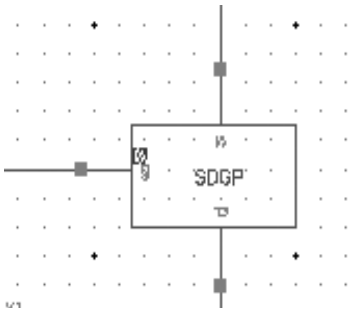

Fig 4: Symbol of Symmetric Double Gate PMOS

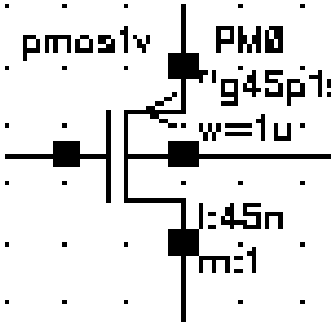

Fig 5: Symbol of Bulk PMOS

IV. Circuit Analysis

Using the implemented symbol the DG PMOS device characteristics have been studied in different aspect and compared the result with the BULK PMOS in 45 nm technologies and the simulation is done by cadence virtuoso.

As it is know that an inverter is a logic gate which implements logic negation. An inverter circuit outputs a voltage representing the opposite logic level to its input. Inverters can be constructed using single PMOS transistor coupled with a resistor. Since this 'restive drain 'approach uses only a single type of transistor, it can be fabricated at low cost. However, because current flows through the resistor in one of the two states, the resistive-drain configuration is disadvantaged for the processing speed that means delay is more in this case. So alternatively inverter can be constructed using DOUBLE GATE PMOS transistor coupled with a resistor. This configuration greatly reduced delay and performance is also better compared to BULK PMOS .so we get the better performance followed by the reduced delay and as well as the fabrication cost is also very low. Fig 6 shows the circuit of BULK PMOS inverter.

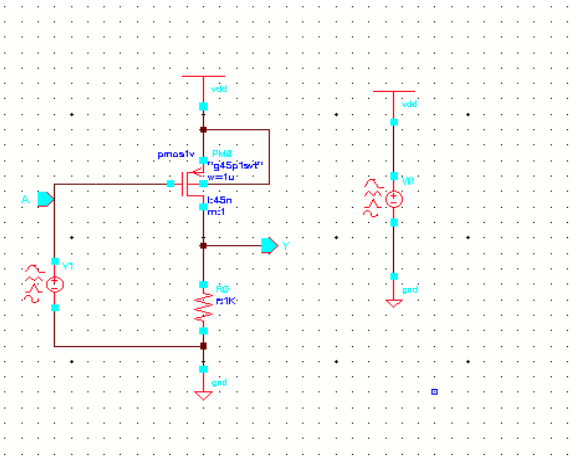

Fig 6: Circuit diagram of BULK PMOS inverter

From graphical analysis Fig 7, Fig 8, Fig 9, Fig 10, Fig 11 it can be observed that variation of width of PMOS from 0.5 µm to 5.5 µm the logic '1' is not achieved perhaps the value at the point 5.5 µm is 0.789mV. Hence it is clear that achieve logic '1'the width of PMOS should be further extended. In addition to it TABLE 1 shows that it's impossible to evaluate delay when the width of PMOS varies from 0.5 µm to 3.5 µm, after exceeding the width of PMOS that is from 4 µm the delay increases periodically. Therefore, the processing speed of the BULK PMOS is low. Fig 9 & Fig 10 shows the delay performance of BULK PMOS.

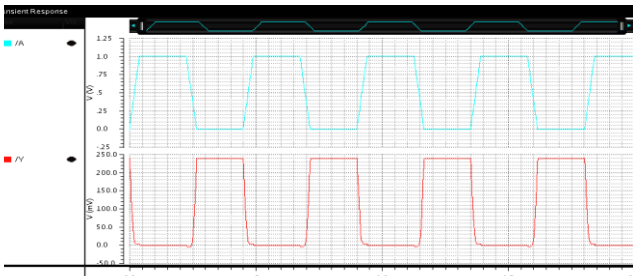

Fig 7: Output of BULK PMOS when width of PMOS is 1 µm

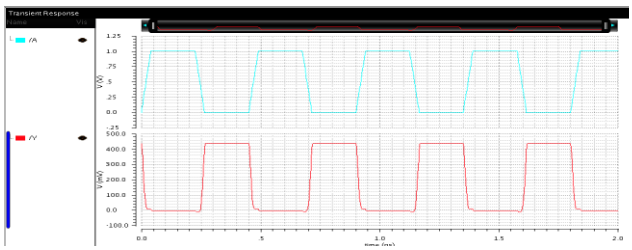

Fig 8: Output of BULK PMOS when Width of PMOS = 2 µm

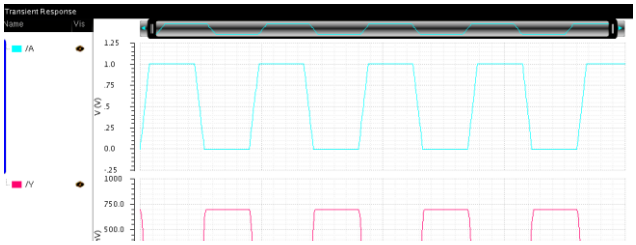

Fig 9: Output of BULK PMOS when Width of PMOS = 4 µm

TABLE 1 Delay of BULK PMOS

Width of PMOS (μ)	Resistance (kΩ)	Rise delay(ps)	Fall delay (ps)	Delay of BULK PMOS (ps)
0.5	1	-	-	-
3.5	1	-	-	-
4	1	18.08	-10.14	7.94
4.5	1	18.35	-8.246	10.14
5	1	18.38	-6.7442	11.63

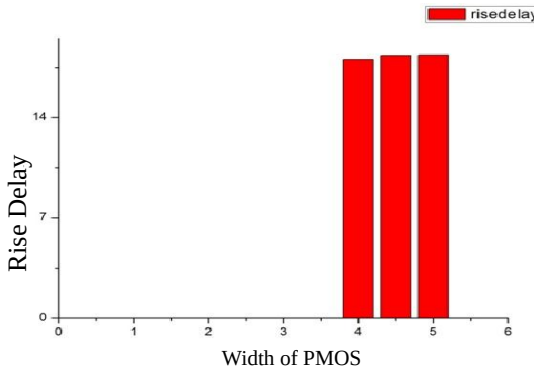

Fig 10: Rise delay of BULK PMOS

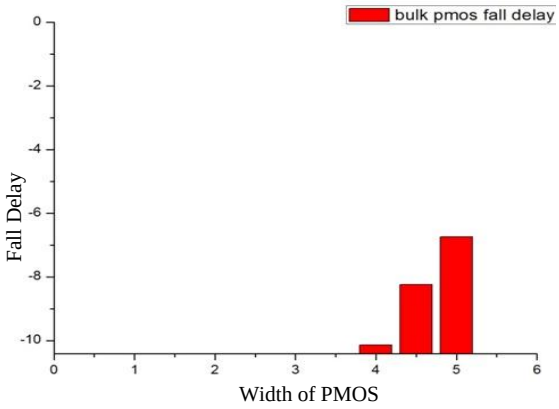

Fig 11: Fall delay of BULK PMOS

Since it is observed that BULK PMOS processing speed is low so DG PMOS have been taken in consideration as the advantages of double gate MOSFETs over conventional, single gate transistor are described I terms of performance and potential for ultimate scaling. In DGPMOS the top gate and bottom gate are biased simultaneously to establish equal surface potentials. In fully depleted transistors with a thin film, controlling the channel from both sides, forces most of the carriers to flow in the middle of the film. Fig 12 shown the circuit of DG PMOS INVERTER

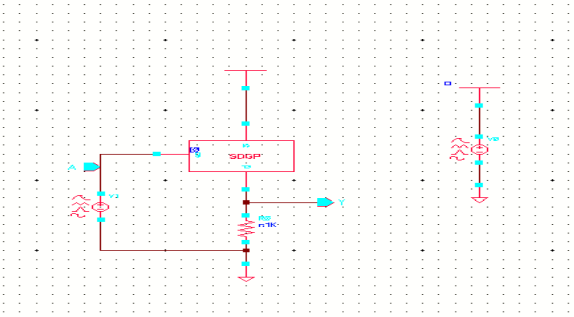

Fig 12: Circuit of DG PMOS inverter

Further by graphical analysis Fig 13, Fig 14, Fig 15, Fig 16, Fig 17 it can be observed that variation of width of PMOS from 0.5 µm to 5.5 µm the logic '1' is almost achieved when the value at the point 5.5 µm is 0.995mV. Hence it is clear that for achieving logic '1' the width of PMOS should be precisely extended, as at width of 5.5 µm is very prone to logic '1' so it means that a minute precise extension of width is required. In addition to it TABLE 2 shows that it's impossible to evaluate delay when the width of PMOS is 1.5 µm or grater, as at the width of 1.4 µm the delay is about 1.128 so this confirms that the delay is reducing gradually, from the width 0.5 µm to 1.4 µm the delay is reduced. Therefore, the processing speed of the DG PMOS is better. Fig 18, Fig 19 and Fig 20 shows the delay performance of DG PMOS.

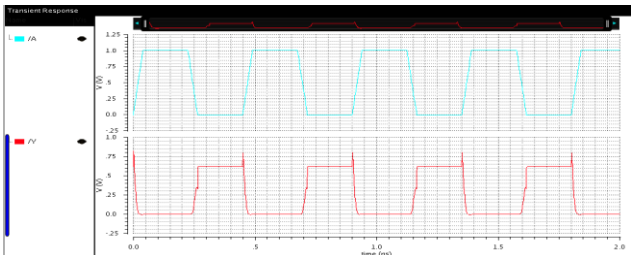

Fig 13: Output of DG PMOS when width of PMOS 0.5 µm

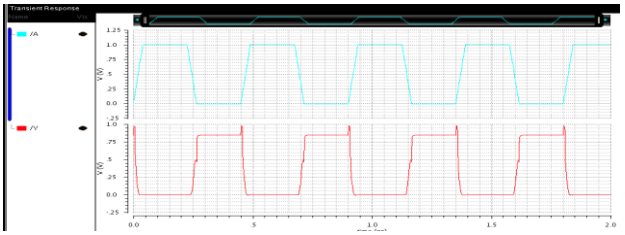

Fig 14: Output of DG PMOS when width of PMOS 0.8 µm

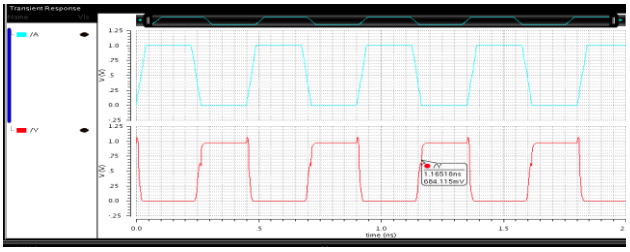

Fig 15: Output of DG PMOS when width of PMOS 1.2 µm

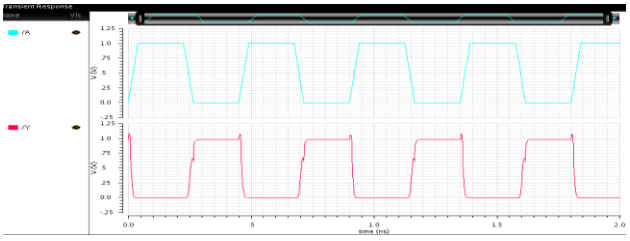

Fig 16: Output of DG PMOS when width of PMOS 1.3 µm

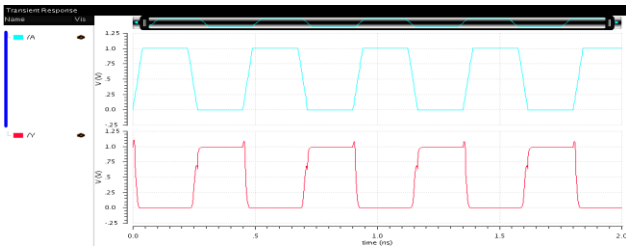

Fig 17: Output of DG PMOS when width of PMOS 1.4 µm

TABLE 2 Delay of DG PMOS

Width of PMOS (μ)	Resistance (kΩ)	Rise delay(ps)	Fall delay(ps)	Delay of DG PMOS(ps)
0.5	1	20.24	-13.96	6.28
10.8	1	20.05	-10.79	9.26
1.21	1	11.96	-9.440	2.52
1.2	1	9.988	-8.406	1.582
1.3	1	9.254	-7.965	1.289
1.4	1	8.702	-7.574	1.128

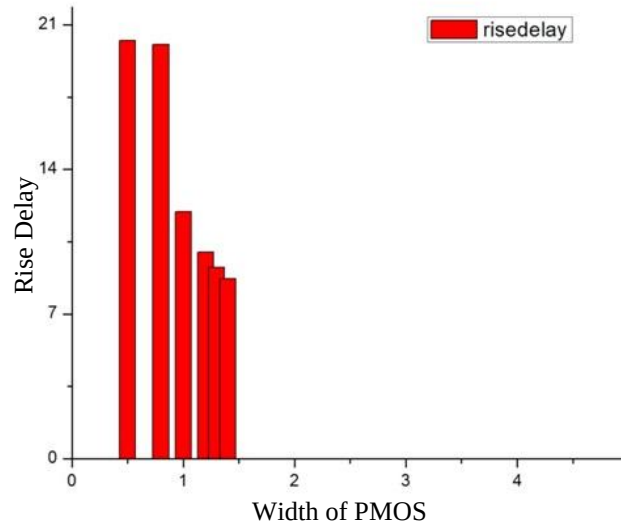

Fig 18: Rise Delay of DG PMOS

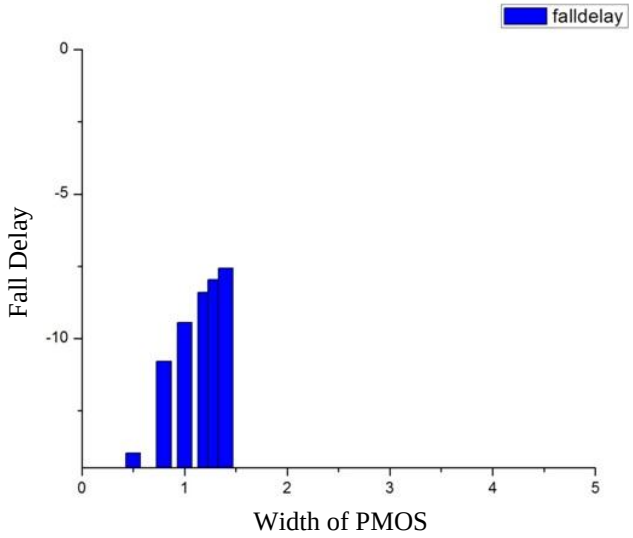

Fig 19: Fall Delay of DG PMOS

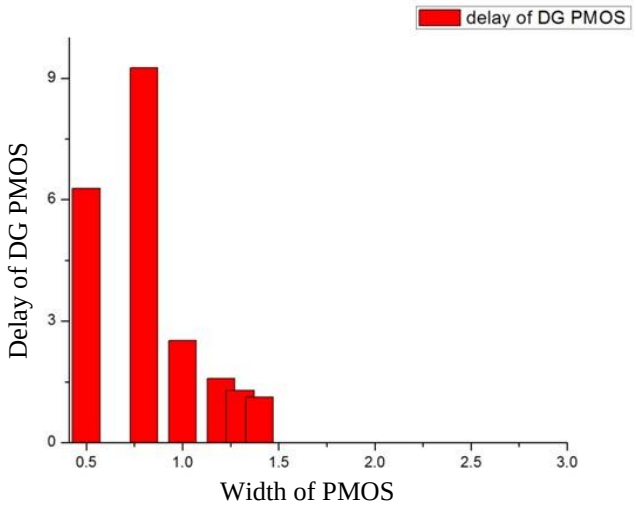

Fig 20: Delay of DG PMOS

V. Result and Discussion

All the simulation and calculations shows that BULK PMOS fabrication cost is low but the delay is high so it is less favorable for processing i.e. processing speed is low. Perhaps Double Gate MOS inverter has two gates top gate and bottom gate are biased simultaneously to establish equal surface potentials. In fully depleted transistors with a thin film, controlling the channel from both sides, forces most of the carriers to flow in the middle of the film. Therefore the delay observed is very less compared to BULK PMOS inverter, so it can be preferred as its processing speed is better. The result of comparative study is presented in TABLE 3 and TABLE 4 and a graphically in Fig 21, Fig 22, Fig 23.

TABLE 3 Delay comparison between double gate PMOS & bulk PMOS

Width of the PMOS(μ)	Resistance (kΩ)	Delay of DG PMOS (ps)	Delay of BULK PMOS(ps)
0.5	1	6.28	-
10.8	1	9.26	-
1.21	1	2.52	-
1.2	1	1.582	-
1.3	1	1.289	-
1.4	1	1.128	-
2	1	-	-
2.5	1	-	-
3	1	-	-
3.5	1	-	-
4	1	--	7.94
4.5	1	-	10.14
5	1	-	11.63

TABLE 4 Comparison study of Width of the PMOS to reach logic'1'

Width of the PMOS(μ)	Wp required to reach logic'1'for DG PMOS	Wp required t reach logic '1' For BULK PMOS
0.5	0.75	0.125
0.8	0.841	0.13
1	0.94	0.250
1.2	0.971	0.250
1.3	0.98	0.258
1.4	0.987	0.35
2	0.987	0.4
2.5	0.988	0.44
3	0.989	0.545
3.5	0.989	0.649
4	0.99	0.697
4.5	0.99	0.75
5	0.991	0.75
5.5	0.995	0.789
5.5	0.995	0.789

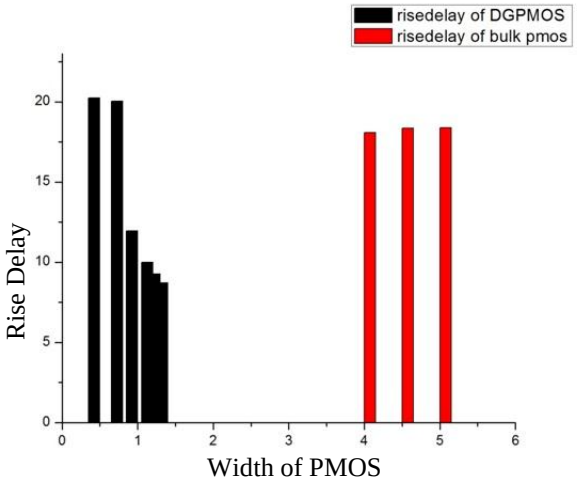

Fig 21: Comparison study of rise delay between DG PMOS and BULK PMOS

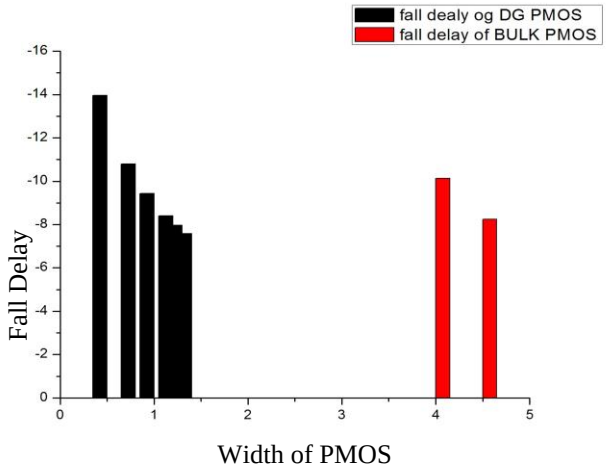

Fig 22: Comparison study of fall delay between DG PMOS and BULK PMOS

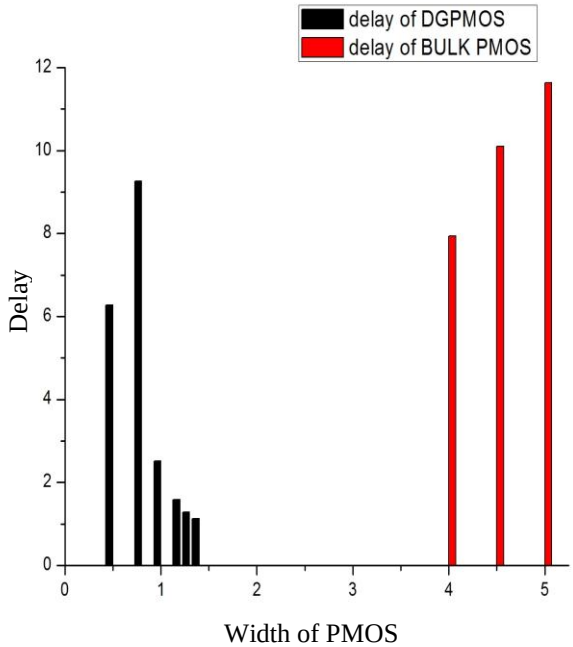

Fig 23: Delay comparison of DGPMOS and BULK PMOS

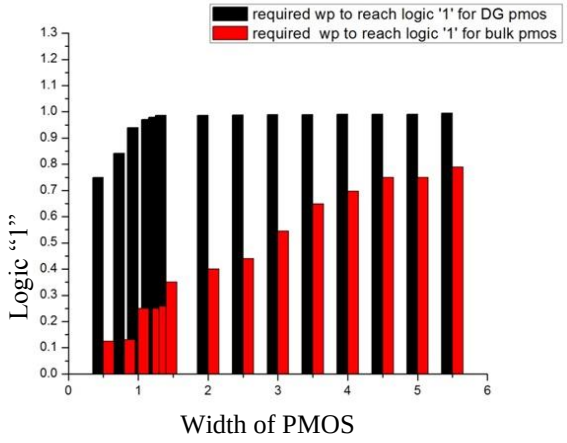

Fig 24: Comparison to required Width of PMOS to reach logic'1'

In VTC i.e. voltage transfer characteristics curve analysis it shows that DGPMOS has achieved logic " 1 ", where as Bulk PMOS didn't achieved logic " 1 " at 1kΩ resistance and width of PMOS is 1 μm in Fig 25, Fig 26.

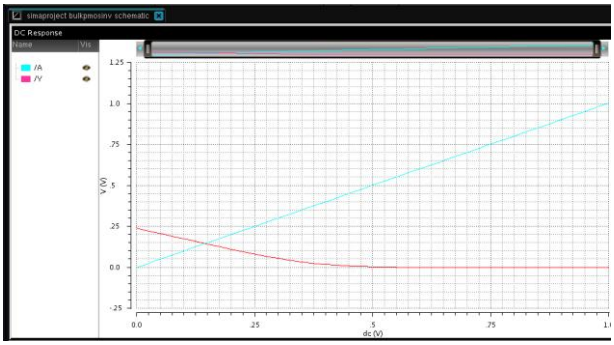

Fig 25: VTC Curve of Bulk PMOS

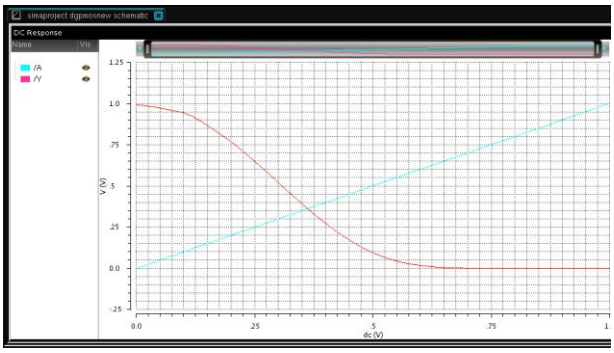

Fig 26: VTC Curve of DG PMOS

VI. Conclusion

In this paper we presented DGPMOS and BULK PMOS delay properties where it had been observed the delay of BULK PMOS is more compared to DG PMOS. The tendency towards logic '1' is higher for DG PMOS compared to BULK PMOS. Hence it can be concluded that implementation of DG PMOS is better than conventional PMOS. Hence it is favorable and economic to implement DGPMOS instead of Bulk PMOS as it consist more advantages over Bulk PMOS

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Sima Baidya currently pursuing M.Tech in VLSI and Micro Electronics, at Heritage Institute of Technology under West Bengal University of Technology. Her interest includes VLSI, Digital Signal Processing, FPGA, Fabrication, FinFET Technology.

Arindam Chakraborty currently pursuing M.Tech in Mechanical Engineering at Dr Sudhir Chandra Sur Degree Engineering College under West Bengal University of Technology. His interest includes Mechatronics, Fabrication, Nano Manufacturing, AI, VLSI technology.