Design and Simulation of 2-Bit Full Subtractor Using Various CMOS Technologies

Shital Baghel, Pranay Kumar Rahi

***Abstract*— Low power and efficient area are frequently required in very large scale integration design. The Complementary Metal Oxide Semiconductor CMOS are used in various electronic fields *viz* manufacturing of digital integrated circuits, microcontrollers and microprocessors. In this paper, the proposed CMOS 2- bit full subtractor is simulated and analyzed using Microwind 3.1. A comparison has been done on account of the power and surface area. The simulations in 90nm, 70nm and 50nm CMOS technologies were done. The full subtractor using 50nm CMOS technology provides low power and efficient surface area as compared to 90nm and 70nm CMOS technologies.**

***Index Terms*— CMOS, VLSI, Full Subtractor, Power consumption, CMOS technology**

I. INTRODUCTION

The full-subtractor is a combinational circuit which is used to perform subtraction of three bits. It has three inputs, A (minuend) and B (subtrahend) and C (subtrahend) and two outputs D (difference) and B (borrow) [1].For more than four decades, downscaling of CMOS has been the fundamental strategy for improving the performance of VLSI circuits. However, there have been reports suggesting that the MOS transistor cannot shrink beyond certain limits dictated by its operating principle [2].The speed and power dissipation are the important parameters which should be taken into consideration in digital circuits. Since number of integrated transistors become double in once in 18 months, there is a much need to fabricate low power VLSI chips. Portable consumer electronic products powered by batteries is an another factor for low power VLSI Design, since the battery technology alone cannot solve the low power problem [3]. Basically a subtractor is a digital circuit that performs subtraction of numbers or one could possibly say that it performs one of the four basic binary operations [4].

II. SUBTRACTOR

Subtractor is a circuit which is used to do subtraction. There are two types of subtractor i.e., Half Subtractor and Full Subtractor.

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Shital Baghel, pursuing Masters of Technology in Electronics and Communication Engineering from Indian Institute of Technology Kharagpur, India

Pranay Kumar Rahi, pursuing Masters of Engineering in Electronics and Communication Engineering from National Institute of Technical Teacher's Training & Research, Punjab University, Chandigarh, India

A. HALF SUBTRACTOR

The half subtractor is a combinational circuit which is used to perform the subtraction of two bits. It consists of two inputs called the minuend denoted as A and the subtrahend denoted as B and two outputs called difference denoted as D and borrow denoted as Bin [5]. The logic diagram for half subtractor is shown in Fig. 1. The truth table for the half subtractor is given in table I:

Table I. Truth Table of Half Subtractor

Inputs		Outputs	
A	**B**	**D**	**B_{in}**
0	0	0	0
1	0	1	0
0	1	1	1
1	1	0	0

The Boolean expression for the two output variables are as follows [5]:

$$D = A'B + AB' \quad (1)$$

$$Bin = A'B \quad (2)$$

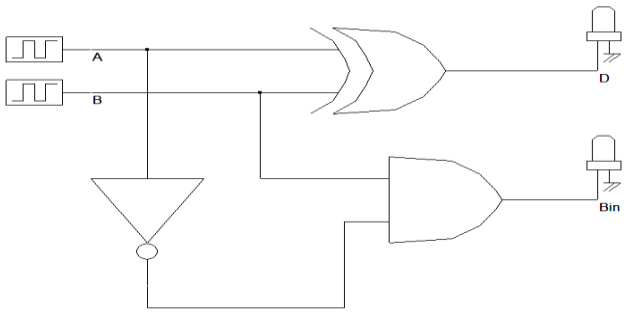

Fig.1 Half Subtractor using XOR, AND and NOT gate.

B. FULL SUBTRACTOR

The full-subtractor is a combinational circuit which is used to perform subtraction of three bits. It has three inputs, A(minuend) and B(subtrahend) and Bin (subtrahend) and two outputs D (difference) and Bout (borrow)[1]. Full subtractor is constructed using two half subtractor using two XOR, two AND, two NOT and one OR logic gates. The Full Subtractor

is used in various VLSI application. It is widely used in microprocessors. In arithmetic logical unit they are used to perform arithmetic operations. The logic diagram for full subtractor is shown in Fig. 2. The truth table for the full subtractor is given in table II:

Table II. Truth Table of full subtractor

Input			Output	
A	**B**	**B_{in}**	**D**	**B_{out}**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

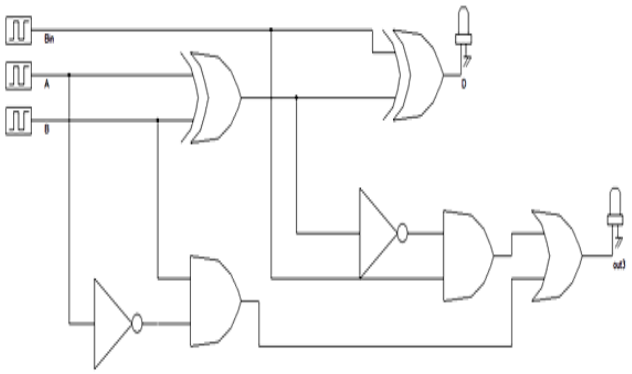

Fig.2 Full Subtractor using XOR, NOT, AND, OR logic gates

The Boolean expression for full subtractor for the two output variables are as follows [5]:

$$D = A \oplus B \oplus Bin \qquad (3)$$

$$Bout = A'B_{in}+A'B+BB_{in} \qquad (4)$$

Dynamic dissipation and short circuit are the component of power to be considered during the input signal transition. To modify the charge content of the capacitive load, the dynamic power is dissipated and it is proportional to the switching frequency and to the load capacitance, and also depends on the area of the buffers. By the simultaneous conduction of P and N transistors during the transition of the input signal the short circuit power dissipation is produced. The ratio of input to transition times is a good indicator of short circuit power dissipation. The value of ratio should be comparable or lower than unity, and it is the objective of buffer design, the short circuit power dissipation can be omitted. In the result just consider the dynamic component to optimize objectives. The total value of the load capacitances includes layout parasitic (diffusion and interconnect) and active loads is the minimum capacitance [6].

III. SIMULATION

The full subtractor are compared based on the performance parameters like surface area and power dissipation. To achieve better performance, the circuits are designed using CMOS process by Microwind 3.1 in 90nm, 70nm and 50 nm technology. The proposed full subtractor circuit shown in figure 3, uses two 2-bit X-OR, two 2-bit AND, one 2-bit OR and two 1-bit NOT logic gates. All the layouts and simulation results presented here are done in Microwind3.1 which is a layout editor and simulator. On the layout presented by this tool, simulation can be done. Simulation is first performed using schematic entry and its corresponding test patterns are generated and is verified whether it is functioning properly or not. The schematic file after verification is converted to VERILOG file. Then the VERILOG file is imported using the command "compile Verilog file" using MW environment so that the schematic of the logic design will be converted into physical layout. MSK File is used to store the information of the layout design. Power dissipation, rise delay, fall delay, timing results, layout area are the performance characteristics which can be provided by this tool. There is a facility in this tool to convert layout to Caltech Intermediate Format (CIF) which provides the information for fabrication. To extract the electrical parameter there is a program EXTRACT in this tool. Metal Oxide Semiconductor Implementation Service (MOSIS) uses standard mask layout like CIF for fabrication.

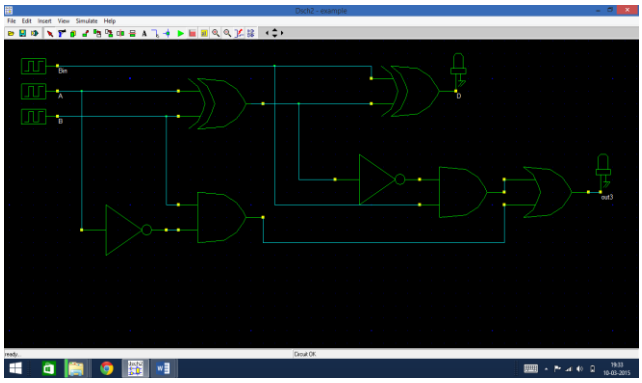

Fig.3 Schematic design flow of proposed Full Subtractor

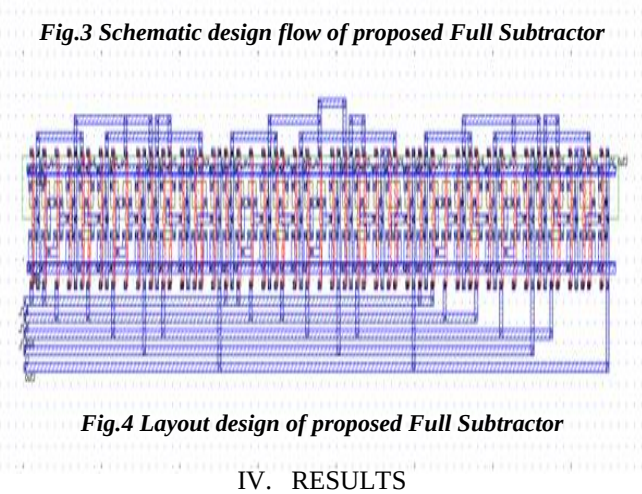

Fig.4 Layout design of proposed Full Subtractor

IV. RESULTS

Figure 5-7 shows the timing diagram results of proposed full subtractor using 90nm, 70nm, 50nm CMOS fabrication technology.

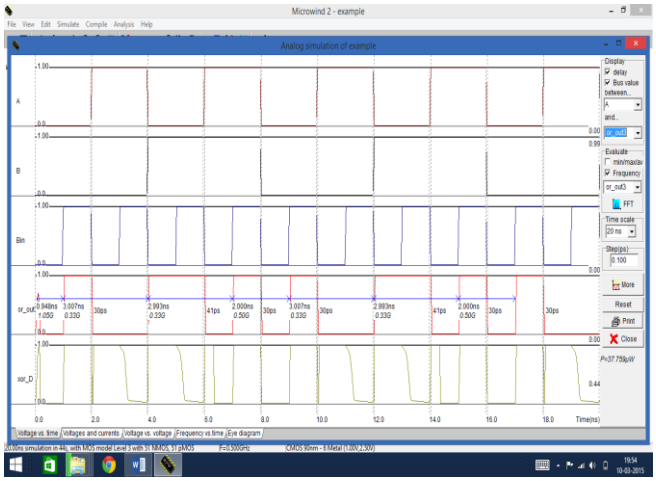

Fig.5 Output of proposed Full Subtractor using 90nm CMOS Technology

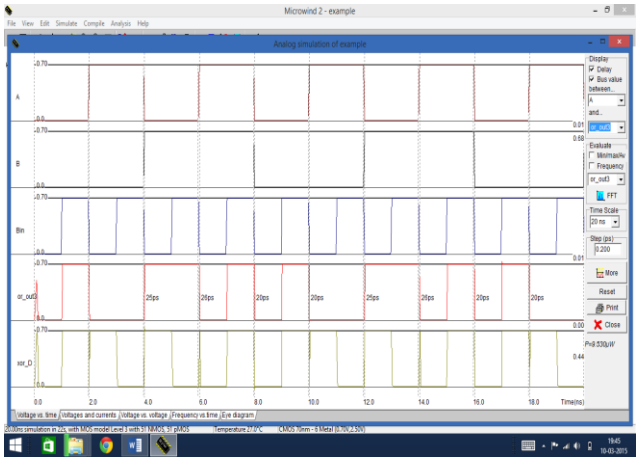

Fig.6 Output of proposed Full Subtractor using 70 nm CMOS Technology

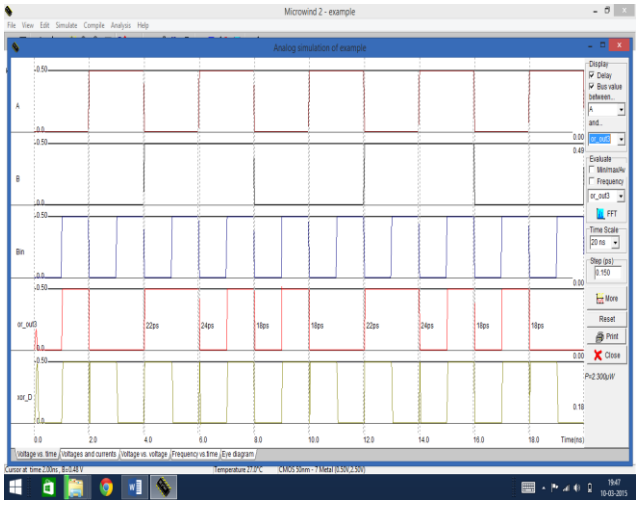

Fig.7 Output of proposed Full Subtractor using 50 nm CMOS Technology

The comparative results for proposed full subtractor for 90nm, 70nm and 50 nm CMOS design technology are given in Table-III. Figure 8 shows the graphical comparison of 2-bit Full Subtractor using 90nm, 70nm, 50nm CMOS technology.

Table III. Power and surface area analysis of 2-bit Full Subtractor in different CMOS technologies

CMOS Technology / Parameters	90 nm	70 nm	50 nm
Power (in µW)	37.759	5.3	2.3
Surface Area (in µm^2)	251.5	123.3	62.9

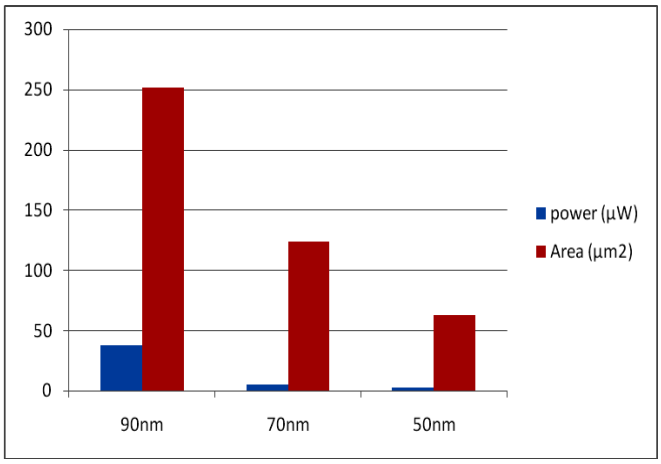

Fig. 8 Graphical comparison of 2-bit Full Subtractor using 90nm, 70nm, 50nm CMOS Technology.

V. CONCLUSION

Simulation of the proposed full subtractor with 90 nm, 70 nm and 50 nm CMOS technologies is done. The power consumption and surface area are compared of different foundaries. For 70nm CMOS technology the overall power and surface area has been improved by 85.96% and 50.97% respectively for proposed full subtractor. Finally an improvement of 93.90% and 74.99% for proposed full subtractor in 50nm CMOS technology is achieved.

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AUTHORS

Shital Baghel received the Bachelors of Technology degree in Electronics and Telecommunication Engineering from CSIT Durg, Chhattisgarh Swami Vivekananda Technical University, Bhilai, Chhattisgarh, India in 2009, and pursuing Masters of Technology in Electronics and Communication Engineering from Indian Institute of Technology Kharagpur, India.

Pranay Kumar Rahi received the Bachelors of Technology degree in Electronics and Telecommunication Engineering from Government Engineering College, Guru Gasidas University, Bilaspur, Chhattisgarh, India in 2004, and pursuing Masters of Engineering in Electronics and Communication Engineering from National Institute of Technical Teacher's Training & Research, Punjab University, Chandigarh, India