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Power Efficient Arithmetic Logic Unit

Silpa T S, Athira V R

Abstract— **In the modern era, power dissipation has become a major and vital constraint in electronic industry. Many techniques were already introduced to reduce power dissipation. Gate Diffusion Input (GDI) Technique allows power dissipation to a greater extend compared to the other logic styles. This technique also reduces the transistor count and thus the area of the circuit. Thus the circuit will be much simpler and easy to manage. This paper describes the design of an 8 – bit Arithmetic Logic Unit using Gate Diffusion Input (GDI) Technique and also the comparison with other logic styles. Basic Logic Gates, half adders, full adders, multiplexers etc are also designed and performances are compared in terms of power dissipation and transistor count. The ALU design uses 2x1 multiplexers, 4x1 multiplexers, half adders, full adders and OR gates to realise the basic arithmetic and logic functions.The arithmetic functions are Addition, Subtraction, Increment, and Decrement. The logic functions that can be realised are AND, OR, XOR, and XNOR. The simulation tool used is Tanner EDA 13.0 using 250nm technology.**

Index Terms— **GDI Technique, CMOS logic, Transmission Gate logic, Arithmetic Logic Unit.**

I. INTRODUCTION

With the rapid increase in the use of portable electronic devices, the power dissipation has become a major constraint. As the technology grows rapidly and the device size scales down to the nanometer range, power dissipation, area and propagation delay are the major factors to be considered.The look for improving the performance of circuits based on CMOS logic resulted in the introduction of many logic styles like Pass Transistor logic, Transmission Gate logic, Double Pass Transistor logic and also many other hybrid logics.Pass Transistor logic is one of the most widely used logics for low power digital circuits. It has many advantages over CMOS, ie high speed, low power dissipation and lower interconnection effects. GDI Technique can overcome certain drawbacks of PTL Logic.

A wide range of complex logic functions in which PTL was used, can be replaced by GDI Technique and this makes the circuit simple. Easier design of fast, low power circuits with less number of transistors are enabled using GDI Technique. Arithemetic and lgic operations are the inevitable part of all high speed and low power circuits in the field of microprocessors, digital signal processing, image processing etc. An Arithmetic Logic Unit with low power dissipation, lesser transistor count and lesser propagation delay can contribute much to the modern era.

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Silpa T S, M.Tech Scholar, Department of ECE, NCERC,Pampady, Thrissur, Kerala, India/ Mobile No.0091 9567147379.

Athira V R, Assiatant Professor, Department of ECE, NCERC,Pampady, Thrissur, Kerala, India/ Mobile No.0091 9633086640,

In this paper an 8-bit ALU is designed using GDI Technique and its power dissipation and transistor count is compared with the CMOS logic. The sub blocks used are multiplexers, adders and gates. The basic logic gates AND, OR, XOR, XNOR and combinational circuits like half adder, full adder, multiplexer etc are designed and compared with the existing logic styles, CMOS and Transmission Gate , in terms of power dissipation and transistor count. Simulation environment is Tanner EDA tool using 250nm technology.

The Section II comprises of comparison of different logic styles and previous works.In Section III, the basic ideas of GDI cell and is operational analysis is discussed. Section IV deals with the design of basic gates, combinational circuits and ALU using GDI Technique and the comparison with existing logic styles. In Section V, simulation results and the discussions are shown. The paper is concluded in Section VI.

II. COMPARISON AND PREVIOUS WORKS

The comparison is carried out with CMOS Logic, Transmission Gate Logic and theGDI Technique. The previous worksin the design of ALUs using these techniques are also explained in this section.

A. Comparison

CMOS logic style consists of a pull-up and pull-down network. The pull-up network comprises of the pMOS transistors and the nMOS transistors forms the pull-down network. Any logic functions can be realised using this. The advantages of CMOS logic are (1) robustness, (2) transistor sizing, (3) reliable operation at low speed. It also has certain disadvantages. They are (1) slow speed, (2) high power consumption [1].

Pass Transistor logic is another popular one. The difference between PTL and CMOS is that the source side of logic network is connected to some input signal instead of power lines. The advantages of PTL are (1) high speed, (2) low power consumption; (3) lower interconnect effect. The disadvantages are (1) slow operation, (2) reduced voltage swing. Transmission Gate logic deals with the voltage drop caused by pass transistor logic. This can be used to implement a wide range of functions using fewer transistors.

GDI Technique is a new low power technique that can be used to overcome the drawbacks of CMOS and PTL logic. In this technique, power dissipation and transistor count will be less compared to other logics.

B. Previous Works

There are different types of full adders designed so as to reduce the power dissipation since adders are the integral part of any digital system. A conventional CMOS full adder using 28 transistors are proposed in [6]. This full adder will reduce power consumption and transistor count. The conventional

CMOS full adder has 42 transistors. The new adder thus will reduce power consumption and transistor count.

Transmission Gate full adders using 24 transistors are proposed by A. Sharma, R. Singh and R. Mehra. Since buffers are needed at each stage, the power consumption will be more than that of 28 transistor CMOS full adder. The CPL full adder consists of 18 transistors. Transmission Function full adder (TFA) based on transmission function theory has 16 transistors. T. Esther Rani, M. Asha, Dr. Rameshwar Rao designed ALU using Hybrid PTL and GDI Technique.

In this paper, 8-bit ALU is designd using only GDI cells. All sub circuits used, ie multiplexers, full adders, halfadders, gates etc are designed only using GDI cells.Buffers are also added to each stage inorder to restore the voltage drop after each stage. Voltage drop occurs since in GDI cell has no voltage supply given to it. The buffers added will be given power supply and it will restore the voltage drop.

III. GDI CELL

A GDI cell is a new technique for low power combinational circuits [2]. It was introduced by Arkidy Morgenshtein, Alexander Fish and Israel. A. Wagner in the year 2002. In this approach only two transistors are used to implement a wide range of complex logic functions. This technique provides incell swing restoration under certain conditions.

The basic GDI cell is as shown if Fig. 1. It resembles CMOS inverter in the first glance. The important difference of the GDI cell from CMOS inverter is that it has three inputs.

The three inputs are:

G: The common gate input of nMOS and pMOS.

P: Input to the source or drain of pMOS.

N: Input to the source or drain of nMOS.

Bulks of both nMOS and pMOS are connected to N or P respectively, so that it can be biased at contrast with a CMOS inverter.

The output node: the common diffusion node of both transistors. It can be used as input or output nodes. The basic functions that ca be implemented using GDI cell are shown in the Table.1

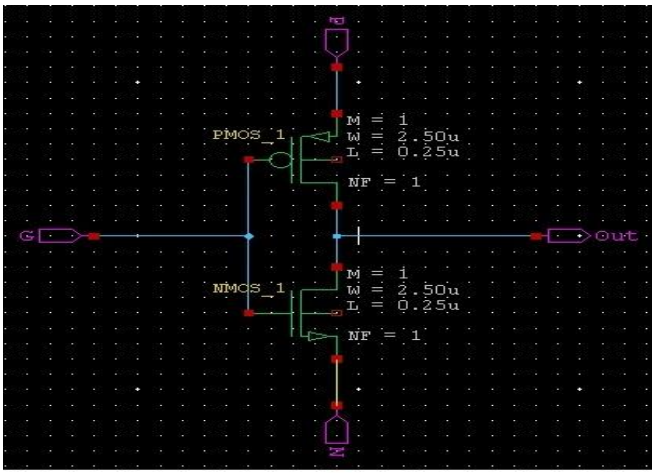

Fig. 1 Basic GDI Cell

Table. 1 Basic GDI Cell Functions

N	P	G	OUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	FUNCTION1
B	1	A	A’+B	FUNCTION2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MULTIPLEXER
B’	B	A	A’B+AB’	XOR
B	B’	A	AB+A’B’	XNOR

IV. COMBINATIONAL CIRCUITS

Combinational circuits, called as time independent logic in digital circuit theory, are a type of digital logic which is implemented by Boolean circuits. In these circuits, output will be a function of input alone, whereas in sequential logic, the output depends on the present input and also on the history of input. In otherwords, the combinational circuit is memoryless and sequential circuits have memory. Combinational and sequential circuits are used in computers to perform arithmetic and logic functions and are made up of combinational circuits. Logic gates are the integral part of combinational circuits.

A. Logic Gates

A physical device that is used to implement Boolean functions is called a logic gate. In other words, a logic gate performs a logic operation on one or more logical inputs and produces a single logical output. The basic building blocks of almost all electronic circuits are logic gates. The devices such as multiplexers, registers, ALUs etc may contain large number of logic gates. The three basic logic gates are AND, OR and NOT, with which all other gates can be implemented. NAND and NOR gates are called universal gates. Any Boolean function can be implemented using these gates.

The gates AND, OR, NOT, XOR, and XNOR are designed in GDI Technique and the performances are compared. When compared to other two logic styles the GDI Technique use less transistors and power dissipation is also less.

B. Multiplexers

A multiplexer is a device used to select one of the several analog or digital inputs. This input is then fed to the output line. The selection of the particular input depends on the select lines. A multiplexer with 2^n inputs will have n select lines. The combination of these select lines determines the input which has to be routed to the output. A multiplexer is also known as data selector.

Using CMOS logic, the implementation of a 2x1 multiplexer need 12 transistors, and four transistors are needed in the Tramsmission Gate logic implementation. In GDI Technique, a 2x1 multiplexer can be implemented using 2 transistors.

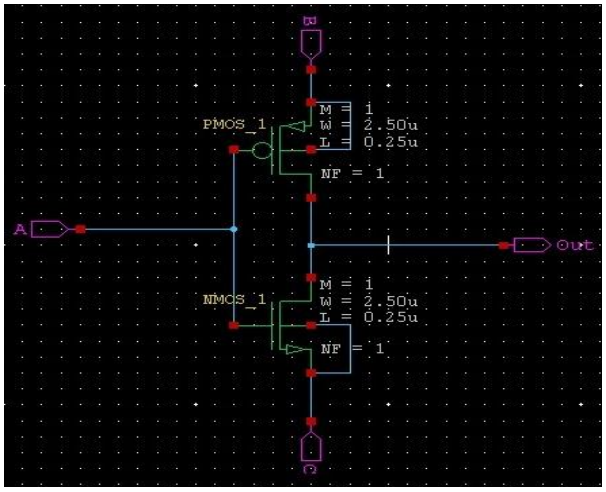

Fig. 2 GDI 2x1 Multiplexer

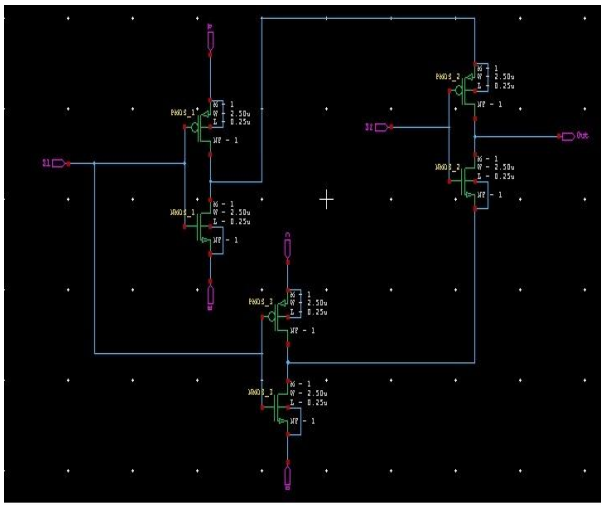

Fig. 3 GDI 4x1 Multiplexer

Fig 2 shows the GDI implementation of 2x1 multiplexer. For implementing 4x1 multiplexer, just 6 transistors are needed in GDI Technique. This is shown in Fig 3.

C. Adders

Since arithmetic opertions play an important role in all digital applications, adders, multipliers etc are the integrable part of digital systems. A full adder cell is the basic building block in all digital systems [3]. It consists of three inputs A, B, Cin and two outputs Sum and Carry. The Sum is expressed as

$$Sum = A \oplus B \oplus Cin.$$

Carry can be expressed in the form

$$Carry = (A \oplus B)Cin + AB$$

CMOS full adder uses about 40 transistors. The most significant advantage of CMOS full adder is the high noise margin and reliable operation at lower speeds.

The parallel connection of both pMOS and nMOS transistors are used in transmission gate logic. This gives full swing in the output.Transmission gate full adder uses this transmission gate logic which also uses the complementary inputs. The advantage of Transmission Gate full adder over CMOS full adder is that the number of transistors used is less and it is fast**.**

Due to the weak capability, additional buffers will be needed at the output in Transmission Gate full adder, which increases the final power consumption and area.GDI Full Adder uses only ten transistors. The implementation is based on XOR and XNOR functions. GDI XOR and XNOR full adders are available. This results in low power consumption and transistor count. Fig. 4 shows the GDI Full Adder [4].

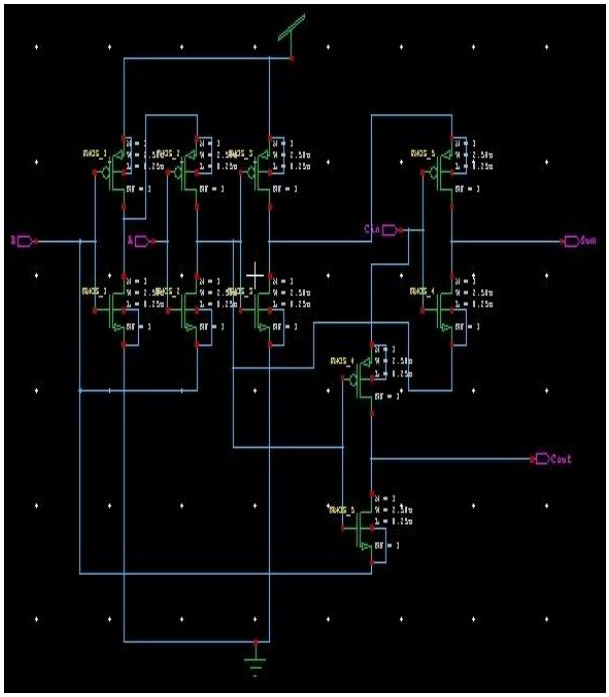

Fig. 4 GDI Full Adder

Since GDI cell has no power supply connected to it, there will be a voltage drop at the output. This drop will be negligible for small circuits. When incorporating into bigger circuits like ALU, multiplier etc, the voltage drop at each stage will be critical. After few stages there will not be sufficient voltage to drive the next stage. Buffers are to be added in such situations. The use of buffer increases the power dissipation when compared to GDI cell is used alone, but will is less than that of CMOS and Transmission Gate logic circuits.

D. Design of ALU

An ALU is a digital circuit used to perform arithmetic and logic operations [5]. It is a fundamental building block of the Central Processing Unit (CPU) of a computer. Arithmetic operations like addition, subtraction, increment, decrement, transfer, etc and logic functions like AND, OR, XOR, XNOR etc are performed in ALU. This paper deals with the design of an 8- bit ALU which performs the foresaid functions. The design of ALU is as shown in Fig. 5. It consists of sixteen 4x1 multiplexers, eight 2x1 multiplexers, eight full adders, eight half adders and eight OR gates. The functions are performed on the basis of select line combinations. When $S_2 = 0$, arithmetic functions are performed. Logic functions will be performed when $S_2 = 1$.

Table. 2 ALU Operations

SELECTION LINES			OPERATIONS
S_2	S_1	S_0	
0	0	0	INCREMENT
0	0	1	ADDITION
0	1	0	SUBTRACTION
0	1	1	DECREMENT
1	0	0	AND
1	0	1	OR
1	1	0	XOR
1	1	1	XNOR

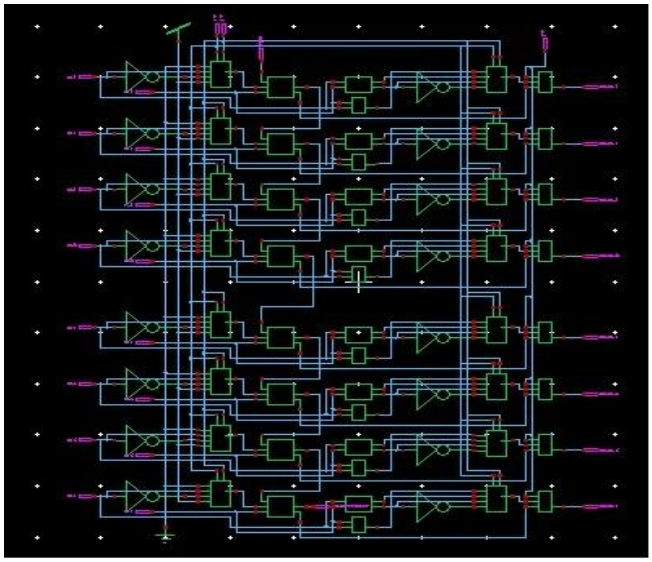

Fig. 5 Schematic of 8- bit ALU

Increment operation is performed by the addition of '1' to the addend and decrement operation is performed by the complement addition. Two's complement method is used for subtraction in which complement of B is used. The funtions obtained from the full adder are Addition, Subtraction, Increment, Decrement and Transfer. The functions XOR, XNOR, and AND are obtained from the half adder and an OR gate is used to get the OR function.

V. SIMULATIONS AND RESULTS

In this section the simulations results of the circuits using CMOS, TG and GDI logic styles are described. The simulation results using Tanner EDA tool 250nm technology is shown in the figures below. The Table 3 shows the comparison of the different logic styles in the basis of power consumption and transistor count.

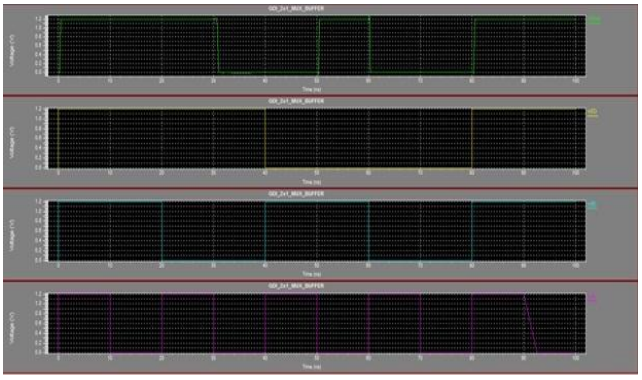

Fig. 6 2x1 Multiplexer Simulation Output

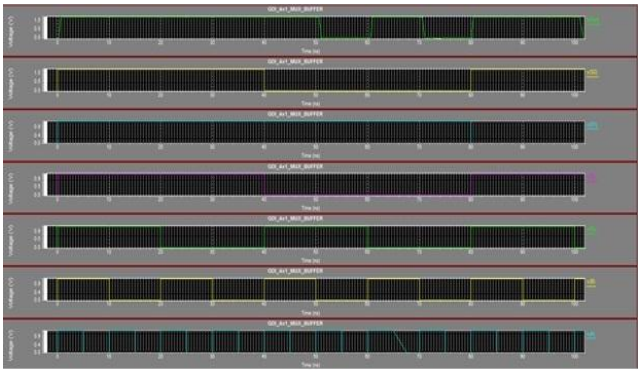

Fig. 7 4x1 Multiplexer Simulation Output

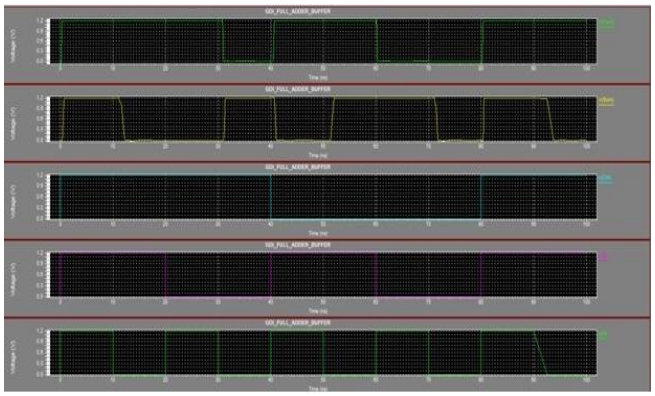

Fig. 8 GDI Full Adder Simulation Output

Table. 3 Comparison and Analysis

CELL	DESIGN	POWER(µW)	TRANSISTOR COUNT
AND	CMOS	2.89	6
	TG	2.21	6
	GDI	1.4pW	2
	GDI BUFFER	2.05	6
OR	CMOS	2.2	6
	TG	2.42	6
	GDI	0.11	2
	GDI BUFFER	2.3	6
XOR	CMOS	5.41	12
	TG	4.75	8
	GDI	.897	4
	GDI BUFFER	2.693	8

XNOR	CMOS	5.244	12
	TG	4.31	8
	GDI	1.312	4
	GDI BUFFER	3.47	8
MUX 2x1	CMOS	3.869	12
	TG	0.53	4
	GDI	1.44pW	2
	GDI BUFFER	1.87	6
MUX 4x1	CMOS	10.5	26
	TG	.55	6
	GDI	1.44 pW	6
	GDI BUFFER	3.27	10
HALF ADDER	CMOS	7.64	18
	TG	5.64	8
	GDI	1.02	6
	GDI BUFFER	4.825	14
FULL ADDER	CMOS	15.56	42
	TG	19.2	20
	GDI	7.3	10
	GDI BUFFER	10.5	18
ALU 4 BIT	CMOS	52.43	536
	GDI	20.08	144
	GDI BUFFER	42.21	336
ALU 8 BIT	CMOS	62.43	1072
	GDI	19.22	288
	GDI BUFFER	55.79	672

VI. CONCLUSION

Power consumption in CMOS circuits can be broadly classified into static power dissipation and dynamic power dissipation. Static power dissipation is mainly due to leakage current ie the direct current flow through the components from Vdd to Gnd. This occurs due to the rise time and fall time of the signals. Dynamic power dissipation is due to the transistor switching activity or in other words due to the charging and discharging of the load capacitance. Dynamic power dissipation is given as

$P_{dynamic} = \alpha CV^2f$, where

α = Switching Factor
C = Load Capacitance
V = Supply Voltage
f = Frequency of Operation

The static power dissipation is negligible compared to dynamic power dissipation. The GDI Technique reduces the dynamic power dissipation. Since the transistor count is reduced the power dissipation and area of the circuit can be reduced. Various combinational circuits are designed in different logic styles and simulated using Tanner EDA tool 250nm technology and performanceis compared. From these comparisons it is proved that GDI Technique has the best performance in terms of power dissipation and transistor count.

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Ms. Silpa T S, student, is currently pursuing her M.Tech VLSI Design in department of ECE in Nehru College of Research and Engineering, Pampady, Trissur. She has completed B.Tech in Electronics and Communication Engineering in Sahrdaya College of Engineering and Technology, Thrissur. Her research areas are VLSI, Low Power Design

Ms. Athira V R, Assistant Professor, Department of ECE, Nehru College of Research and Engineering, Pampady, Trissur. She has completed M.Tech VLSI Design in Amrita School of Engineering and AMIE in Electronics and Communication Engineering. Her research areas are VLSI, Digital IC Design..