A Novel Non-Linear Transient Analysis for Phase-Locked Loop Design

Zhi-Ming Lin, *Member, IEEE*, Po-Yu Kuo, *Member, IEEE*, Shu-Chung Yi, *Member, IEEE*

***Abstract*—Phase-Locked Loop (PLL) circuits are widely used in wireless communication and control systems. To achieve the best performance of PLL circuits, it requires several model simulations to obtain the optimized circuit parameters. This paper proposed a time behavioral model of PLL. The new behavioral model allows us fine tuning the PLL circuit parameters. A new behavioral model of Phase Frequency Detector (PFD) is also proposed in this paper. The new PFD model allows the calculation of PLL transient response with different loop filter. To minimize the computation time, the new method applies two calculation techniques: *piecewise linear* and *cycle by cycle*. The new method takes few seconds to finish the calculations while HSPICE takes days to finish a similar simulation. Therefore, the new model is efficient and accurate for fine tuning the PLL circuit parameters and designing high performance PLL.**

***Index Terms*— Phase-Locked Loop (PLL), Phase Frequency Detector (PFD), piecewise linear, cycle by cycle, HSPICE simulation.**

I. INTRODUCTION

The Phase-Locked Loop (PLL) circuits are widely used in wireless communication and control systems. These circuits are the essential parts in System-on-Chip (SoC) integrated circuits. They are used for frequency modulation and demodulation, clock recovery and synchronization, and frequency synthesis.

In the early days, PLL circuits were pure analog circuits. Because there were no computer simulations in those days, circuit analyses were done by hand calculations. The linearized small signal model was developed to aid PLL circuit design [1]. However, any active circuits, which use transistors or vacuum tubes, are essentially non-linear circuits. Thus signals are controlled sufficiently small so that the transistors and vacuum tubes are operated in their linear regions. Mathematically, it is more feasible to solve the linear equations of PLL model than to solve the large signal non-linear equations. By applying the small signal model analysis, it provides key circuit performance factors such as loop frequency, phase margin, gain, and damping factor. The drawback is that the analysis is in frequency domain. In fact, the circuit designers would like to see the performance in time domain such as transient responses and settling time of the PLL circuits.

Recently, PLL circuits consist of analog and digital parts so that they are mixed signal integrated circuits. Because the transistors of digital circuits are operated in saturation region, the digital parts in PLL circuits are nonlinear circuits. To simulate both analog and digital circuits, the designers have to put the entire PLL circuit in HSPICE simulation. However, it takes a few days of HSPICE simulations even in a high performance workstation [2], [3]. To solve this issue, several approaches have been proposed in the past decades [4]–[7]. However, they fail to simulate PLL circuits without using HSPICE simulations. The main reason is that they were unable to model the Phase Frequency Detector (PFD) correctly and they still followed the small signal model analysis in frequency domain [1]. The fundamental problem is that they still use phase angle to do the transient analysis. Phase angle is a mathematical concept and it only works in frequency domain type of analysis. As a result, those recent approaches just apply discrete time analyses of the small signal model.

In this paper, we proposed a novel non-linear transient analysis method to simulate PLL circuits. Moreover, a complete and exact behavioral model for the digital PFD has been proposed. To reduce the computation time, *Piecewise linear* and *cycle by cycle* techniques are applied in the proposed method. The new method takes few seconds to finish the calculations while HSPICE takes days to finish a similar simulation.

The rest of this paper is organized as follows. Section II discusses the small signal model of PLL. Section III includes the proposed PFD behavioral model. Section IV describes the detail of non-linear PLL transient analysis. Section V verifies the proposed PLL model. Section VI shows the results of the PLL model with charge pumps and Section VII gives the conclusions.

II. SMALL SIGNAL MODEL OF PLL

The basic architecture of PLL consists of a phase/frequency detector (PFD), a loop filter (LF), and a voltage controlled oscillator (VCO). Fig. 1 shows the basic structure of PLL. From Fig. 1, each functional block is connected to form a closed loop phase-locked circuit. To achieve the best performance of PLL circuits, it requires several model simulations to obtain the optimized circuit parameters.

The voltage controlled oscillator, VCO, has a behavioral model which can be characterized as the following equation.

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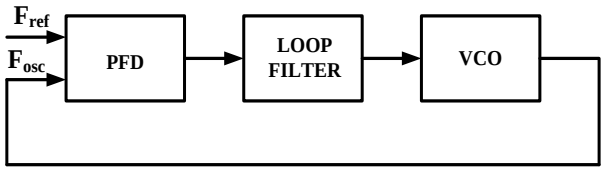

Fig. 1. The basic structure of PLL.

$$F_{\text{osc}} = F_{\text{o}} + K_{osc}V_{cntl} \tag{1}$$

where F_{osc} is the oscillator frequency, F_{o} is the zero bias free running frequency, V_{cntl} is the control voltage, and K_{osc} is frequency per volt. This structure is adequate because the PFD does not detect the minute changes of the frequency waveform. The PFD only check the zero crossings or the timing edges of the frequency output by the VCO. The loop filter (LP) is made up of linear circuit components, R, L, and C. Thus, the LP and VCO have existed circuit models for transient analysis. However, the digital PFD requires a precise and exact model for analysis.

The linearized small signal model does not attempt to model the PFD, especially the digital blocks [1]. It artificially creates a phase difference model that can work with the small signal model. Most analog circuit designers assume that the PFD output voltage is linearly proportional to the phase difference between the input frequency and the VCO frequency. The controlled voltage of VCO is an average over one frequency cycle as follows:

$$V_{\text{cntl}} = K_{\text{pd}} \times (\phi_{\text{osc}} - \phi_{\text{ref}}) \tag{2}$$

Therefore, it does not model the exact output of a PFD because the output may be pulses and may have undesirable high frequency signals. This is the reason that a loop filter is needed to be inserted between the PFD and the VCO. Because phase angle is a mathematical concept, it depends on the frequency. The linearized small signal model assumes that the PLL is close to lock condition. Thus, the reference frequency and oscillator frequency are almost equal and superimposed as one frequency that can be used to define the phase angle. The phase angle difference is the same from cycle to cycle. When the VCO frequency changes slowly, the phase angle also changes correspondently in each cycle. If the two frequencies are different, the phase angle difference accumulates from cycle to cycle. However, equation (2) does not consider the accumulated phase angles. Thus, in the linearized small signal model, an artificial integrator is added to the model after the VCO as shown in Fig. 2.

For linear analysis, it is assumed that the phase frequency detector output is a voltage and this output is a linear function of the difference in phase between its inputs as follows:

$$V_{pd} = K_{pd} \times (\theta_{ref} - \theta_{osc}) \tag{3}$$

where θ_{ref} and θ_{osc} are the phases of the input and feedback signals, respectively. K_{pd} is the gain factor of the phase frequency detector and has units of voltage per radian. Since the phase angle is the accumulative volume, an integrator has been added to change the VCO output frequency to phase angles.

$$\theta_{osc} = \frac{f_{osc}}{s} \tag{4}$$

The closed loop transfer function of the PLL is the transfer function of phase θ_{osc} to the input phase θ_{ref} as follows:

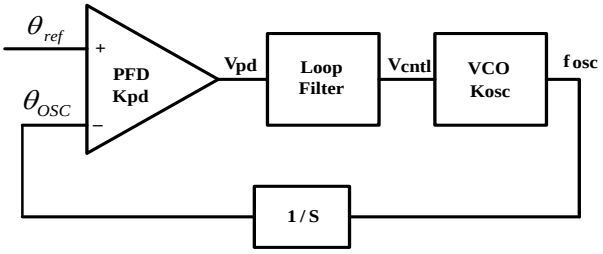

Fig. 2. Linear small-signal model of phase-locked loop.

$$H(s) = \frac{\theta_{osc}}{\theta_{ref}} = \frac{K_{pll} \bullet H_{lp}(s)/s}{1 + K_{pll} \bullet H_{lp}(s)/s} = \frac{1}{\dfrac{s}{K_{pll} \bullet H_{lp}(s)} + 1} \tag{5}$$

where K_{pll} is the PLL gain factor, and $H_{lp}(s)$ is the transfer function of the loop filter as given by

$$K_{pll} = K_{pd}\, K_{osc} \tag{6}$$

$$H_{lp}(s) = \frac{1 + s\tau_z}{1 + s\tau_p} \tag{7}$$

where $\tau_z << \tau_p$. The proposed new PFD model includes the effect of this integrator and does not use phase angle; τ_p is the time constant of the loop filter.

III. The Proposed PFD Behavioral Model

A. Description of the Model

To explain the detail of the PFD behavioral model, the HSPICE simulation results of the digital PFD is shown in Fig. 3. The top waveform is the output of the PFD. The bottom two waveforms are the frequency inputs of the PFD. It is noted that the *period of pulse, T*, is defined by the larger period of the two input frequencies. The *pulse width*, *W*, is the accumulation of period difference computed on a cycle by cycle basis. Thus, PFD is also considered as an integrator. When the sum of pulse width is larger than one period, one period of the other frequency is subtracted from the pulse width sum to keep the pulse width smaller than one period. The Up pulses get successively wider up to the 4th pulse. The width of fifth Up pulse is narrower as the result of one extra subtraction. The behavior of PFD output pulse at each cycle is modeled by the following codes:

```
### PULSE width and period calculation for each cycle ###

T_ref = 1/F_ref; T_osc = 1/F_osc;     # calculate the periods of the input
                                        frequencies.
Sum = Sum + ( T_osc - T_ref ) ; # calculate the "phase difference"
                                        and integrate.
if Sum > 0                              # it is Up pulse
while Sum > T_osc
Sum = Sum - T_ref ;
end
pulsewidth = Sum ; period = T_osc; sign = 1;
else                                    # it is Down pulse
while Sum < -T_ref
Sum = Sum + T_osc ;
end
```

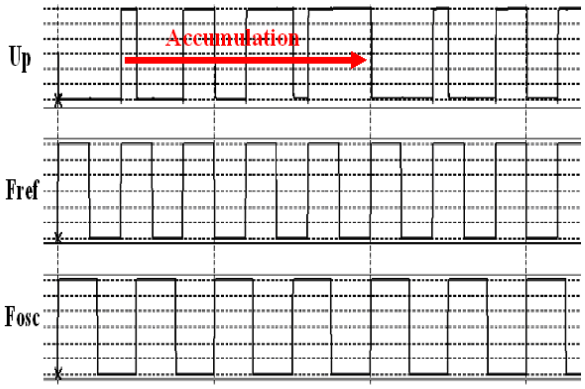

Fig. 3. The simulation results of the digital PFD.

```
pulsewidth = abs(Sum) ; period = T_ref; sign = -1;
  end;
end
```

At the start, the Sum is reset to zero. The two input frequencies are fixed. One pulse cycle is computed. One can run the program over several cycles and see that the codes produce the same pulses as the HSPICE simulation. The sign is used to indicate whether this is an Up or Down pulse. In these codes, the sign is set for the VCO and frequency increases with the control voltage.

If the VCO frequency decreases with increasing voltage, the sign has to be reversed. The PFD responds only to one cycle of the input frequency at a time. It does not care about the details within a cycle. In the PLL circuit, this allows adjustments of the VCO frequency according to the PFD output voltage at each cycle. The proposed behavioral model does not require near lock condition and can work with vastly different input frequencies. This model can also apply to the case that the two input frequencies are equal, but with an initial phase difference. The output pulses are constant. The pulse width is equal to the initial Sum. The period is just the period of either input frequencies, depending whether it is an Up pulse or Down pulse.

B. Modification of the Model with Dead Zone

In a real PLL circuit, the VCO frequency F_{osc} varies with the time. The pulses can change from Up pulses to Down pulses, and vice versa. During the transitions, the period is not defined by either of the two input frequencies. Thus, a minor correction to the period is needed. It is shown in the following codes:

```
Previous_sign = sign;      #save the sign from previous
                           cycle;
T_ref = 1/F_ref; T_osc = 1/F_osc;
Sum = Sum + ( T_osc - T_ref ) ;
if Sum > 0                 #Up pulse
while Sum > T_osc
Sum = Sum - T_ref ;
end
pulsewidth = Sum ; sign = 1;
      if previous_sign <0          #transition from Down
                                    to Up
      period = T_ref + pulsewidth;  #correcting the period
      else period = T_osc ;
      end
else                               #Down pulse
while Sum < -T_ref
Sum = Sum + T_osc ;
end
pulsewidth = abs(Sum) ; sign = -1;
      if previous_sign >0          #transition from Up to
                                    Down
      period = T_osc + pulsewidth;  #correcting the period
      else period = T_ref ;
      end
end;
end
```

The PFDs usually have Dead Zone when there are no output pulses. For a 10 picoseconds dead zone, it can be easily modeled by adding this line of codes:

If pulsewidth < 10 ps, then pulsewidth = 0;

Further refinements to this PFD behavioral model have very little effects to the PLL simulations. Therefore, a complete behavioral PFD model has been verified and proposed, and does not need the near lock assumption on the input frequencies.

IV. Non-Linear PLL Transient Analysis

In the previous discussions, each sub block of the basic PLL is modeled properly. The new non-linear transient analysis uses the individual block models to simulate the entire PLL circuit. The analysis has been finished by using Matlab. The model of the three sub block in PLL is implemented by Matlab program language. There are three parts to the program. With initial PLL circuit conditions, the PFD model computes the first pulse. The amplitude of the pulse is given the proper voltage or current values. The PFD model is almost like the HSPICE voltage/current source PULSE which generates each pulse width and period without rising and falling times. The PULSE is then applied to the loop filter circuit which produces the output voltage for the VCO. Since the VCO outputs a clock, the period of the clock cycle is the cumulative effect of the control voltage. Therefore, the VCO actually outputs an averaged frequency due to the varying input voltage and average VCO frequency is

$$<F_{osc}> = F_o + K_{osc} <V_{cntl}>. \quad (8)$$

The control voltage is averaged over that cycle and the average voltage is used to calculate the next VCO frequency and period. The loop filter calculation consists of the normal circuit calculation and an additional calculation to obtain the average output voltage, $<V_{cntl}>$. The VCO behavioral model in (8) is used to update the $<F_{osc}>$ for the PFD to calculate the next pulse. Moreover, the VCO frequency is changing and affecting the pulse when the PFD is outputting. To start, the PFD model uses the previous cycle's average control voltage, $<V_{cntl}>$, as an estimate to compute the next pulse and the new $<V_{cntl}>$. The new $<V_{cntl}>$ is then used to iterate the pulse calculation again. If $<V_{cntl}>$ does not change significantly from one cycle to next cycle, the pulse calculation should converge after a few iterations.

The pulse calculation is iterated only once if the proposed method is applied. The pulse is a non-linear signal. It can be observed that the filter output signal is also non-linear in a HSPICE simulation as shown in Fig. 4.

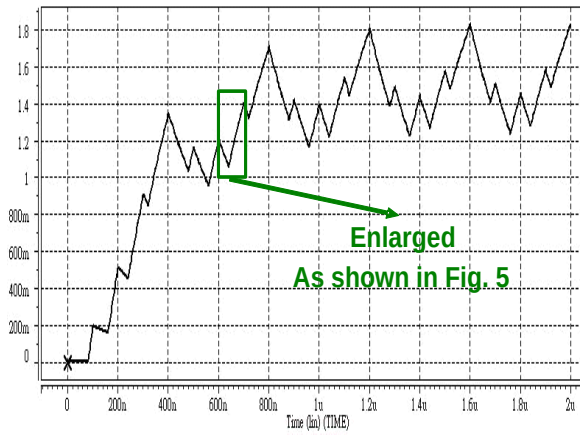

Fig. 4. The HSPICE simulation results of output voltage for the loop filter.

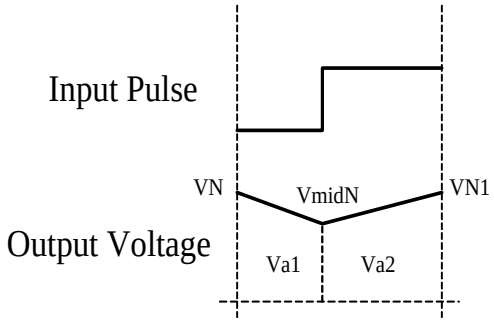

Fig. 5. The output of loop filter within one pulse cycle.

In HSPICE simulations, it uses very small time steps to make the signal piecewise linear [8]. Thus it requires hundreds of thousand calculations to simulate one cycle [9].

In the proposed method, one cycle is divided into two linear regions as shown in Fig. 5. There are only two calculations needed per cycle. The output pulse of the PFD is constant in these two regions, Va1 and Va2. At the beginning of the cycle, the voltage is VN. The linear equation (9) can be used to calculate the VmidN in the region Va1. The linear calculation (10) is used in the region Va2 to obtain VN1.

$$VmidN = VN(1-(T-W)) \div \tau_p \quad (9)$$

$$VN1 = VmidN + (signV_m - VmidN)W \div \tau_p \quad (10)$$

where T is the period of pulse, W is the pulse width, V_m is the amplitude of pulse signal, $sign$ = 1 if Sum > 0, $sign$ = -1. If Sum < 0, and τ_p is the time constant of the loop filter.

The voltage is averaged over this period to obtain $<V_{cntl}>$. The voltage VN1 is the new VN in the next cycle's calculation. That is the detail analysis of one cycle calculation. This is repeated as many cycles as needed to simulate the PLL transient response until it reaches lock condition.

V. Verification of the Proposed PLL Model

To verify the proposed PLL behavioral model, the non-linear transient analysis has been applied to simulate two regular PLLs: a simple 1st order low passes filter (R-C) and a low pass filter with a zero (R1-R2-C). The PFD output pulse is computed by the behavioral codes. The small signal models of those PLLs have been derived and compare the loop frequency and the damping factor ζ with the proposed model. The pulse signal amplitude V_{max} is set to ±1.5V. The pulse signal is applied to the loop filter.

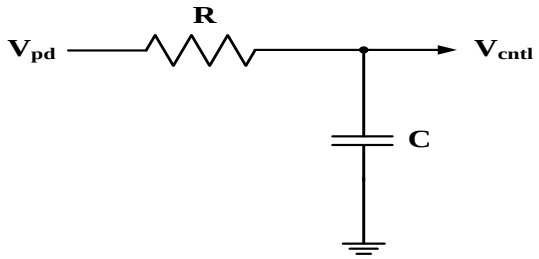

Fig. 6. The 1st order low pass filter.

A. First-Order Low Pass Loop Filter

The first PLL circuit is a simple first order low pass filter as shown in Fig. 6. The transfer function of the 1st order low pass filter is

$$H_{lp}(s) = \frac{1}{sRC+1} \quad (11)$$

where R is the low pass filter resistance, C is the low pass filter capacitance. The values are R = 10 KΩ and C = 100 pF.

We then inserted the 2X gain between the loop filter and VCO. The output of the loop filter is amplified by 2 before being applied to the VCO. The VCO has the behavior as follows:

$$F_{osc} = F_o + K_{osc}V_{cntl} \quad (12)$$

For example, if the VCO have frequency range from 10 MHz to 16MHz and voltage from 0V to 3V, then the tuning frequency range is ± 3MHz at 13MHz. The actual calculation is

$$F_{osc} = 10^7 + 2\times10^6 \times VN \quad (13)$$

The input frequency is 13 MHz and is equivalent to VN = 1.5V. Since the VCO has the effect of averaging the output frequency, $<F_{osc}> = F_o + K_{osc} <V_{cntl}>$. We can simulate the PLL to produce the waveform of $<V_{cntl}>$, which represents the PLL's transient response. The transient response of this first order low pass filter PLL $<V_{cntl}>$ is shown in Fig. 7. The result is then compared to the linear small signal calculation. By Substituting eq. (11) into eq. (5), the small signal PLL transfer function is as follows:

$$H(s) = \frac{1}{\frac{RC}{K_{pll}}s^2 + \frac{s}{K_{pll}} + 1} \quad (14)$$

An equivalent RLC circuit can be used to understand the Damping factor, ζ, as shown in Fig. 8. The transfer function of equivalent RLC circuit is derived as

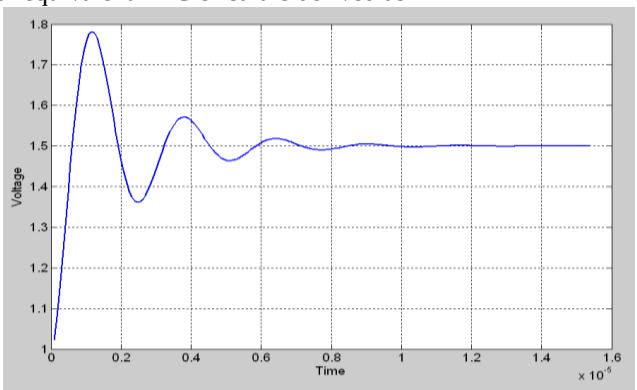

Fig. 7. The output of the 1st order low pass filter. (R=10KΩ and C=100pF).

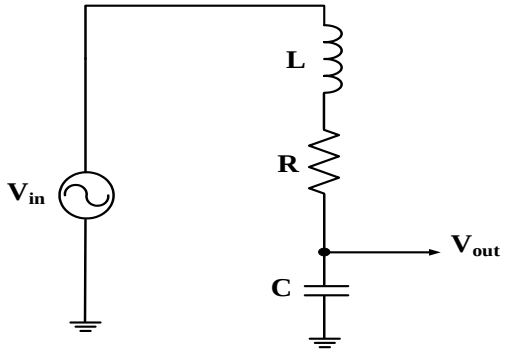

Fig. 8. An equivalent RLC circuit.

$$\frac{V_{out}}{V_{in}} = \frac{1}{LCs^2 + RCs + 1} \quad (15)$$

$$\frac{1}{\omega^2} = LC \Rightarrow \frac{1}{\omega} = \sqrt{LC} \quad (16)$$

Thus, the damping factor of the equivalent RLC circuit is

$$\frac{2\zeta}{\omega} = LC \Rightarrow \zeta = \frac{R}{2\sqrt{LC}} \quad (17)$$

Comparing the above equation with the transfer function (15) which defines the loop frequency and the damping factor, we can obtain

$$H(s) = \frac{1}{\frac{s^2}{\omega_0^2} + \frac{2\zeta s}{\omega_0} + 1} \quad (18)$$

By defining the parameters $\tau_p = RC$ and $\tau_l = \frac{1}{K_{Pll}}$, from eq. (18), we can obtain

$$\frac{RC}{K_{Pll}} = \frac{1}{\omega_0^2} \quad (19)$$

$$\frac{1}{K_{Pll}} = \frac{2\zeta}{\omega_0} \quad (20)$$

The PLL loop frequency is

$$\omega_0 = \sqrt{\frac{K_{Pll}}{RC}} = \frac{1}{\sqrt{\tau_p \tau_l}} \quad (21)$$

The damping factor is

$$\zeta = \frac{\omega_0}{2K_{Pll}} = \frac{\sqrt{\tau_l}}{2\sqrt{\tau_p}} \quad (22)$$

By considering the actual circuit parameters in the small signal model, the loop frequency ω_0 and damping factor ζ are

$$\omega_0 = \sqrt{\frac{K_{Pll}}{RC}} = \frac{1}{\sqrt{\tau_p \tau_l}} = 2.45 \times 10^6 \text{ radians}$$

$$\zeta = \frac{\omega_0}{2K_{Pll}} = \frac{\sqrt{\tau_l}}{2\sqrt{\tau_p}} = 0.204$$

To verify the model, the same circuit parameters are applied to nonlinear transient analysis. The results are shown in Fig. 9. From the results, the loop frequency is about $1/0.26\times10^{-5} = 3.85\times10^5$ Hz, and $\omega=2\pi f=2.42\times10^6$ radians. We compare the waveform to a standard damping waveforms which has curves with different damping factor ζ = 0.1, 0.3, 0.5, and 0.7. The closest is between 0.1 and 0.3. Therefore, both numbers agree with the small signal model calculations.

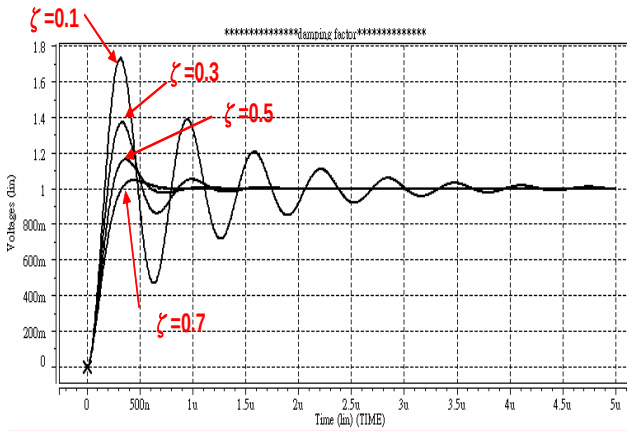

Fig. 9. The results of nonlinear transient analysis with damping factor, ξ = 0.1, 0.3, 0.5 & 0.7.

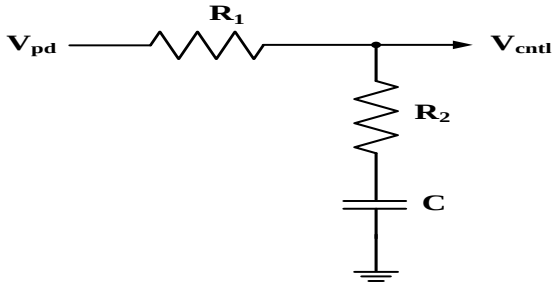

Fig. 10. The 1st order low pass filter with zero.

B. First-Order Low Pass Loop Filter with Zero

The second PLL is also verified by applying the nonlinear transient analysis. This PLL has a zero in the loop filter as shown in Fig. 10.

The transfer function of the 1st order low pass filter with zero is

$$H_{lp}(s) = \frac{sR_2C + 1}{s(R_1 + R_2)C + 1} \quad (23)$$

By substituting eq. (23) into eq. (5), the transfer function of the PLL with this low pass filter is as follows:

$$H(s) = \frac{(sR_2C + 1)}{\frac{(R_1 + R_2)C}{K_{Pll}} s^2 + (\frac{1}{K_{Pll}} + R_2C)s + 1} \quad (24)$$

Let's define the parameters $\tau_p = (R_1 + R_2)C$, $\tau_z = R_2C$, and $\tau_l = \frac{1}{K_{Pll}}$, the transfer function *H(s)* is

$$H(s) = \frac{(\tau_z s + 1)}{\tau_p \tau_l s^2 + (\tau_l + \tau_z)s + 1} \quad (25)$$

We then compare (25) with the standard damping equation as follows:

$$\frac{1}{\frac{s^2}{\omega_0^2} + \frac{2\zeta s}{\omega_0} + 1} \quad (26)$$

From eq. (25) and eq. (26), we can obtain

$$\tau_p \tau_l = \frac{1}{\omega_0^2} \quad (27)$$

$$(\tau_l + \tau_z) = \frac{2\zeta}{\omega_0} \quad (28)$$

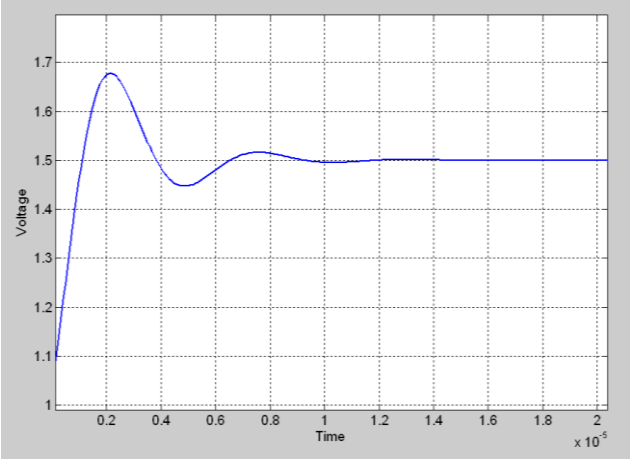

Fig. 11. The output of the low pass filter with zero. (R_1=36KΩ , R_2=4KΩ , and C=100 pF)

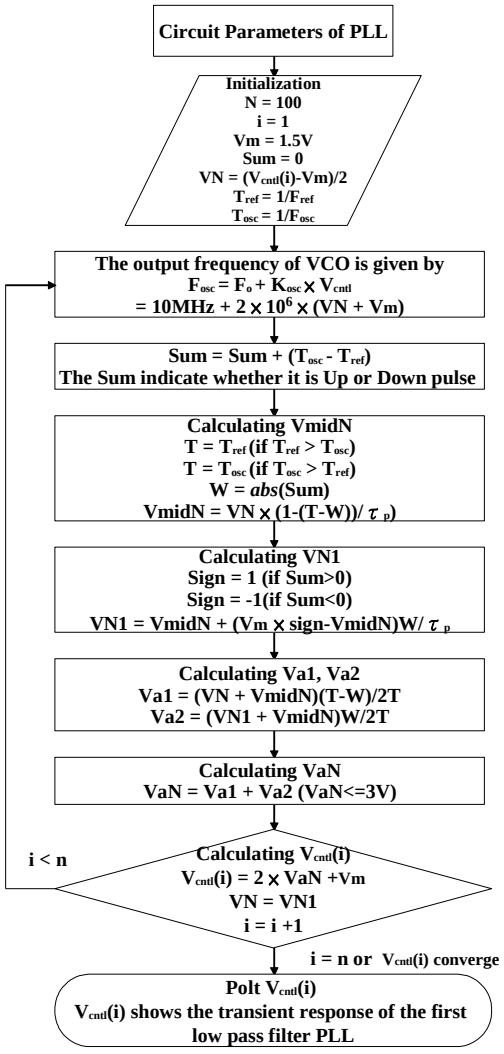

Fig. 12. Calculation flowchart of the regular PLL.

The PLL loop frequency is

$$\omega_0 = \frac{1}{\sqrt{\tau_p \tau_l}} \tag{29}$$

The small signal model damping factor is

$$\zeta = \frac{\omega_0(\tau_l + \tau_z)}{2} = \frac{(\tau_l + \tau_z)}{2\sqrt{\tau_p \tau_l}} \tag{30}$$

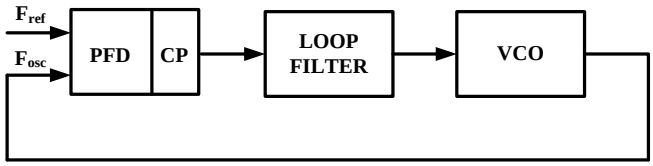

Fig. 13. The basic structure of PLL with charge pump.

It is assumed that R_1 =36 KΩ, R_2 = 4 KΩ, and C = 100 pF. From eq. (29), the small signal model loop frequency is

$$\omega_0 = \frac{1}{\sqrt{\tau_p \tau_l}} = 1.23 \times 10^6 \text{ radians}$$

From equation (30), the damping factor is

$$\zeta = \frac{\omega_0(\tau_l + \tau_z)}{2} = \frac{(\tau_l + \tau_z)}{2\sqrt{\tau_p \tau_l}} = 0.35$$

For the same circuit parameters, the transient response of the low pass filter with zero is shown in Fig. 11. From the waveform, the damping factor is between 0.3 and 0.5 and it is closer to 0.3. The loop frequency is about $1/(0.56 \times 10^5)$ $=1.79\times10^5$ Hz, and $\omega=2\pi f=1.12\times10^6$ radians. The damping factor and the loop frequency are in very close agreement with the small signal model calculations. To describe the proposed method, a flowchart of the above calculations for the new PLL model is illustrated in Fig. 12. The new model is verified by using Matlab as analytical tool.

VI. The Experiment Results

To convert the logic states of the PFD into current pulses, a charge pump is usually inserted between PFD and loop filter. Fig. 13 shows the basic structure of PLL with charge pump. By adding the charge pump, the current pulses of PFD are integrated by the capacitor in the loop filter into analog signals and it is suitable for controlling the VCO.

The non-linear transient analysis can be applied to simulate a PLL with charge pump. The PFD output pulse is calculated by behavioral codes as previous discussion. However, the pulse signal amplitude is set to ± 100μA. The pulse signal is applied to the loop filter as shown in Fig. 14. Moreover, there is no 2X amplifier after the loop filter.

The transfer function of the second order loop filter is as follows:

$$H_{lp}(s) = \frac{sR_2C_2 + 1}{s(C_1 + C_2)(s\frac{C_1C_2}{C_1 + C_2}R_2 + 1)} \tag{31}$$

where R_2 is a resistor, C_1 and C_2 are capacitors. By substituting eq. (31) into eq. (5), the charge pump PLL closed-loop transfer function is

$$H(s) = \frac{sR_2C_2 + 1}{\frac{s^2}{K_{PLL}}(C_1 + C_2)(s\frac{C_1C_2}{C_1 + C_2}R_2 + 1) + sR_2C_2 + 1} \tag{32}$$

Let's define the variables τ_z and τ_p as the following time constants.

$$\tau_z = R_2C_2 \tag{33}$$

$$\tau_P = \left(\frac{C_1C_2}{C_1 + C_2}\right)R_2 \tag{34}$$

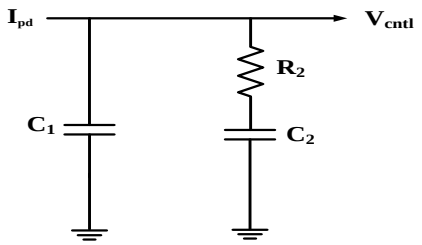

Fig. 14. The 2nd order loop filter.

Thus, *H(s)* can be expressed by the following equation.

$$H(s) = \frac{\tau_Z s + 1}{\frac{(C_1 + C_2)}{K_{pll}}(\tau_P s^3 + s^2) + \tau_Z s + 1} \quad (35)$$

Let

$$\frac{1}{\omega_0^2} = \frac{(C_1 + C_2)}{K_{Pll}} \quad (36)$$

The closed-loop transfer function is equal to

$$H(s) = \frac{\tau_Z s + 1}{\frac{\tau_P}{\omega_o^2} s^3 + \frac{s^2}{\omega_o^2} + \tau_Z s + 1} \quad (37)$$

From eq. (33) and eq. (34), we can obtain

$$\tau_z = \tau_p (\frac{C_1 + C_2}{C_1}) \quad (38)$$

Generally, the loop frequency is close to ω_0. We can express the denominator of *H(s)* in a form similar to the damping equation as follows:

$$\frac{s^2}{\omega_o^2} + (\tau_Z - \tau_P (\frac{\omega^2}{\omega_o^2}))s + 1 \quad (39)$$

It is noted that the damping factor is loop frequency dependent. The denominator of a standard 2nd order damping equation transfer function is shown as below:

$$\frac{s^2}{\omega_o^2} + \frac{2\zeta}{\omega_o} s + 1 \quad (40)$$

Let

$$\frac{2\zeta}{\omega_o} = (\tau_Z - \tau_P \frac{\omega^2}{\omega_o^2}) \quad (41)$$

The unit of K_{Pll} is same as the frequency. We can express K_{Pll} as follows:

$$K_{pll} = I_{pd} K_{osc} \quad (42)$$

Finally, the ω_o and ζ can be calculated as follows:

$$\omega_o = \sqrt{\frac{K_{Pll}}{(C_1 + C_2)}} \quad (43)$$

If $\omega \to \omega_o$, then

$$\zeta = \frac{\omega_o (\tau_Z - \tau_P)}{2} \quad (44)$$

To calculate the loop frequency ω_0 and the damping factor ζ, we plot in the circuit parameters in the equations. Assume that the circuit parameters are I_{pd}=100μA, R_2=100KΩ, C_2=45pF, and C_1=5pF. The K_{osc} is from the VCO model,

$$F_{osc} = F_o + K_{osc} V_{cntl} = 10^7 + 2 \times 10^6 \text{ Hz}$$

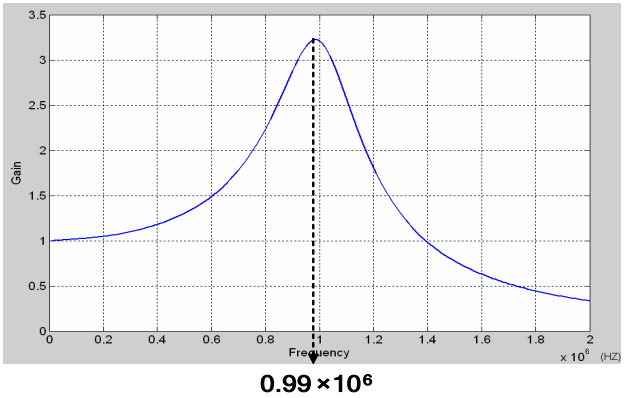

Fig. 15. Gain of PLL with charge pump for R_2=100KΩ.

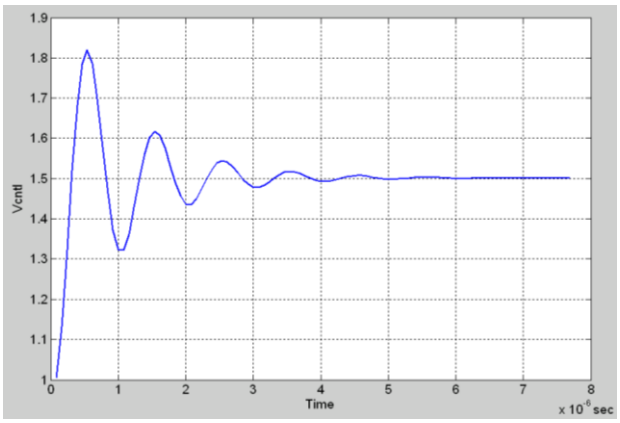

Fig. 16. Result of simulated V_{cntl} for R_2=100kΩ. (I_{pd}=100μA and C= 50pF).

Thus, $K_{osc} = 2 \times 10^6$. From eq. (33) and (34)

$\tau_Z = R_2 C_2 = 100 \times 10^3 \times 45 \times 10^{-12} = 4.5 \times 10^{-6}$ sec.

$$\tau_P = \left(\frac{C_1 C_2}{C_1 + C_2} \right) R_2 = 0.45 \times 10^{-6} \text{ sec.}$$

$$\frac{1}{\omega_o^2} = \frac{(C_1 + C_2)}{K_{PLL}} = 50 \text{ pF} / (100 \text{ μA} \times 2 \times 10^6) = = 0.25 \times 10^{-12}$$

Therefore, $\omega_0 = 2 \times 10^6$

$$\zeta = \frac{\omega_o (\tau_Z - \tau_P)}{2} = 4.05$$

These two numbers are calculated from the traditional definitions of ω_0 and ζ. The damping factor seems to be large. The small signal equation does not tell what the real loop frequency is. The numerator of the *H(s)* is usually ignored. There is another calculation from the small signal equation by including the numerator. We can use *H(s)* to calculate gain versus frequency for R_2=100KΩ. Fig. 15 shows the gain of PLL with charge pump for R_2=100KΩ. From the curve, the maximum gain appears when the frequency is at 0.99×10^6 Hz. Thus,

$$\omega = 2\pi f = 2\pi \times 0.99 \times 10^6 = 6.22 \times 10^6 \text{ radians}$$

$$\zeta = \frac{\omega_o (\tau_Z - \tau_P \frac{\omega^2}{\omega_o^2})}{2} = 0.1475$$

To verify the model, we compared both ω and ζ with the real transient simulation. The result of the non-linear transient simulation is shown in Fig. 16. From the result, the loop frequency is about 1 MHz. The calculated ω is 0.99×10^6 as

shown in Fig. 15. The damping factor, ζ , is between 0.1 and 0.2, or about 0.15. The calculated ζ is 0.15. From the simulation results, the calculated frequency ω and damping factor ζ are very close to the real ones. The proposed PLL model is accurate to present the real circuit. Thus, the loop frequency and the damping factor can be derived from the proposed small signal linear equations precisely.

VII. Conclusions

In this paper, a novel behavioral model that can handle two widely different input frequencies and accompanied with a non-near lock assumption PLL circuit for the digital phase frequency detector (PFD) is proposed. The model can also handle the dead zone of a PLL circuit as well. To reduce the computation time, a new non-linear transient analysis is proposed for PLL circuits. The analysis method takes few seconds to finish the calculations while HSPICE takes days to finish a similar simulation.

A new non-linear transient analysis method is applied to simulate two regular PLL circuits. This new non-linear transient analysis results indicated that we obtained the same results as the traditional small signal model analysis.

In this behavioral model, a PLL circuit with a charge pump is also simulated by using the non-linear transient analysis. Our simulation results indicated that the loop frequency and the damping factor can be derived from the new small signal linear equations efficiently. Therefore, we believed that the proposed non-linear transient analysis in this behavioral model is very practical to simulate PLL circuits. By using the newly proposed method, the circuit designers can optimize their PLL circuit parameters more efficiently comparing to the HSPICE simulations.

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