A Compact Wilkinson Power Divider with High Performance by GaAs-based Optimized IPD Process

E. S. Kim, Y Li, Z. Yao, N. Y. Kim

***Abstract*— This paper presents the design and implementation of a high-performance, compact Wilkinson power divider using an optimized integrated passive device fabrication process on a GaAs substrate for LTE application. Compared to the previous integrated passive device processes, this optimized fabrication process is developed to further reduce the fabrication time and total fabrication cost and to greatly increase the RF performances. The optimized processes are demonstrated and several key parameters are compared for the previous process and optimized process in detail. A Wilkinson power divider is realized using this proposed manufacturing process and is packaged using the SOT-26 packaging method, which shows excellent RF performances with a compact size and low cost. The bare-chip measurement results show two insertion losses below 3.35 dB/ 3.40 dB, all return losses of greater than 15.20 dB and an isolation of greater than 38.00 dB.**

The measured insertion losses for the packaged power divider are better than 3.50 dB/ 3.50 dB, all return losses of greater than 13.50 dB and an isolation of greater than 26.20 dB around the desired frequency. The operating frequency is between 2.24 GHz and 2.40 GHz, which is the LTE application frequency range of band 40. The reliability of the MIM capacitor and power divider is investigated by using a highly accelerated stress test, which results indicate that both the component and device fabricated by the optimized process have a stable and reliable performance.

***Index Terms*— High Performance, IPD Process, LTE Application, Wilkinson Power Divider.**

I. INTRODUCTION

Conventional Wilkinson power dividers are widely used in radio frequency (RF) front-end communication systems for equal/unequal power splitting with in-phase responses at different output ports. Recently, researchers reported several novel power dividers for facilitating the system integration and simplifying the architecture of the RF front-end [1-6]. However, these transmission line-based power dividers on the printed circuit board occupy a large chip area, increase the cost and incur additional power consumption capabilities. Therefore, the development of a high-level integrated fabrication process for the power divider is an important task with the aim of obtaining a compact size and low loss. Integrated passive devices (IPDs), which contain passive circuit components such as resistors, inductors, and capacitors, can be totally integrated and mounted on a semiconducting substrate [7-8]. Through IPD technology, it is possible to integrate individual passive components into an RF device or system [9]. IPDs can be applied to existing fields of applications, which use whole passive devices, and have already been applied to the front-end modules (FEMs) of mobile systems. In addition, in mobile phone communication systems, other functional blocks such as filters, baluns, diplexers, directional couplers, transformers, and power dividers/combiners can also be realized by using IPD technology [10-14].

In this work, a GaAs-based fabrication process that enables the integration of discrete passive components on an IC is considered. This method is highly competitive in terms of its reliability, cost, and yield. A few years ago, we developed a fabrication process for IPDs that consisted of thin film resistors (TFRs), spiral inductors, and metal-insulator-metal (MIM) capacitors with only six layers [15-16] and we continue to improve this previous fabrication process. Currently, this process has been modified to develop a more reliable, cost effective and higher RF performance fabrication process. These optimizations consist of the modification of the bottom metal fabrication processes from the semi-additive method to the subtractive method, the improvement of the bottom metal smoothness, the adjustment of the air-bridge metal thickness, the use of the sputter-etching process, and the use of the SU-8 photoresist as a final passivation. Additionally, several integrated passive components are fabricated using both the previous process and the optimized fabrication process and these two types of IPD fabrication processes are compared by using these components in view of the measurements.

A compact Wilkinson power divider is proposed as a result of this optimized IPD manufacturing process. The Wilkinson power divider is designed and implemented and has very good RF performances with a very compact size. On the other hand, packaging determines the reliability and long-term stability of a microwave device, and good packaging is essential for its commercial success. Therefore, the fabricated power divider was finally packaged using the SOT-26 packaging method and was analyzed. The reliability of the MIM capacitor and packaged power divider was investigated by using highly accelerated stress test. The reliability experimental results indicate that both the component and device fabricated by the optimized process have a stable and reliable performance.

Manuscript received October 17, 2014.

E. S. Kim, Deportment of Electronics, Kwangwoon University, Seoul, South Korea, 82-10.

Y. Li, Deportment of Electronics, Kwangwoon University, Seoul, South Korea.

Z. Yao, Deportment of Electronics, Kwangwoon University, Seoul, South Korea.

N. Y. Kim, Deportment of Electronics, Kwangwoon University, Seoul, South Korea, 82-10, Corresponding Author.

II. Experimental Details

A. Design Theoretical Details

Generally, the design of the power divider starts from the transmission line-based schematic. Fig. 1 (a) depicts a conventional transmission line-based Wilkinson power divider with two λ/4-long transmission lines and an isolation resistor between the output ports. A distributed transmission line with a characteristic impedance of Z_0 and an electrical length can be equivalent to its lumped equivalent π-networks as shown in Fig. 1 (b). The component values can be calculated using the following explanation: the $1/\sqrt{LC}$ is the LC-circuit resonant frequency, which should be equal to the desired center frequency. The impedance of the lumped equivalent equals to that of the distributed transmission line. The impedance of the lumped circuit is $\sqrt{LC}$, which is equal to $\sqrt{2}$ Z_0, and is the characteristic impedance of the transmission line. The two formulas can be ended up with the following:

$$\sqrt{\frac{L}{C}} = \sqrt{2}Z_0 \quad (1)$$

$$\frac{1}{\sqrt{LC}} = \omega \quad (2)$$

Therefore, the corresponding C and L can be obtained as shown in Eq. 3 and Eq. 4 by equating Eq. 1 and Eq. 2, where ω is the operating frequency of 2.4 GHz and Z0 is 50 Ω.

$$C = \frac{1}{\sqrt{2}Z_0\omega} \quad (3)$$

$$L = \frac{\sqrt{2}Z_0}{\omega} \quad (4)$$

In this design, we used a 5.65 nH inductor (L) and an appropriate 0.78 pF capacitor (C) to meet our requirements. Fig. 2 shows a 3-D view of the proposed Wilkinson power divider. Its structure is derived from the lumped π-network, which is depicted in Fig. 1 (b). The design procedure is as follows: first, the first metal line is covered by the second metal line. Two inductive metal lines are 15 μm in width, and the spacing of the metal lines is also chosen as 15 μm to achieve a high Q-factor for the inductor. Two metal lines inter-wound with a 2.0 μm space between the primary side and the secondary side are placed in the cross-sectional area, which forms the air-bridge structure. This part of the structure makes up the spiral inductor, whose design exhibits a Q-factor of 28.5 at 2.4 GHz, as shown in Fig. 3. Second, two different types of capacitors are utilized to realize the MIM capacitors. Type 1 capacitors are directly in series with the inductor and grounding pads. Another two capacitors are realized by Type 2 capacitors, which are connected in parallel. The advantages of this proposed design are not only the reduction of the whole size but also the reduction of the transmission loss by using a 90° parallel connection during the packaging process. Finally, because the accuracy of the 50 Ω TFR is substantially better than the 100-Ω TFR, therefore, two 50-Ω TFRs are designed and fabricated in both sides instead of a 100-Ω resistor.

B. Fabrication Procedures

The substrate used for the fabrication is a 6-inch GaAs wafer polished to a 200 μm thickness, which is advantageous for avoiding the parasitic capacitive and inductive loading of an otherwise conductive substrate for high-speed microelectronic applications. The optimized process starts with a first passivation layer, which is composed of SiN_x and is deposited by plasma enhanced chemical vapor deposition (PECVD) up to a thickness of 2000 Å (Step 1). This layer is necessary to attain an even surface over the defects and a roughness of the substrate surface. After the SiN_x deposition,

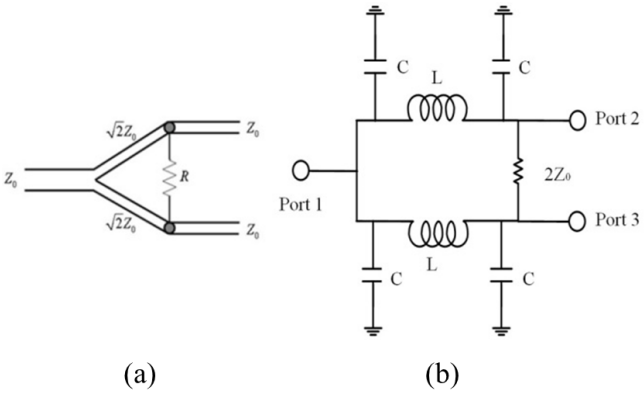

Fig. 1 The schematic structure of: (a) a distributed Wilkinson power divider and (b) a lumped Wilkinson power divider.

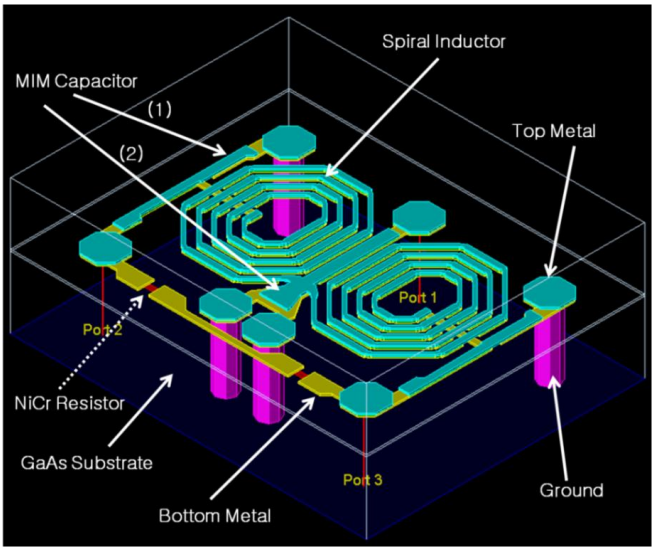

Fig. 2 Three-dimensional (3-D) view of the proposed Wilkinson power divider modeled by Advanced Design System (ADS).

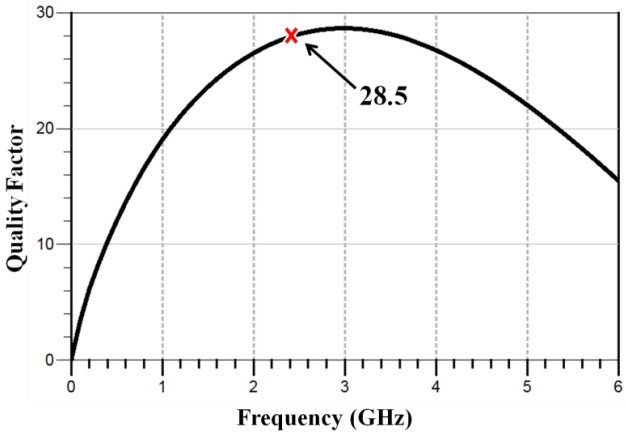

Fig. 3 The quality factor of the designed inductor (L).

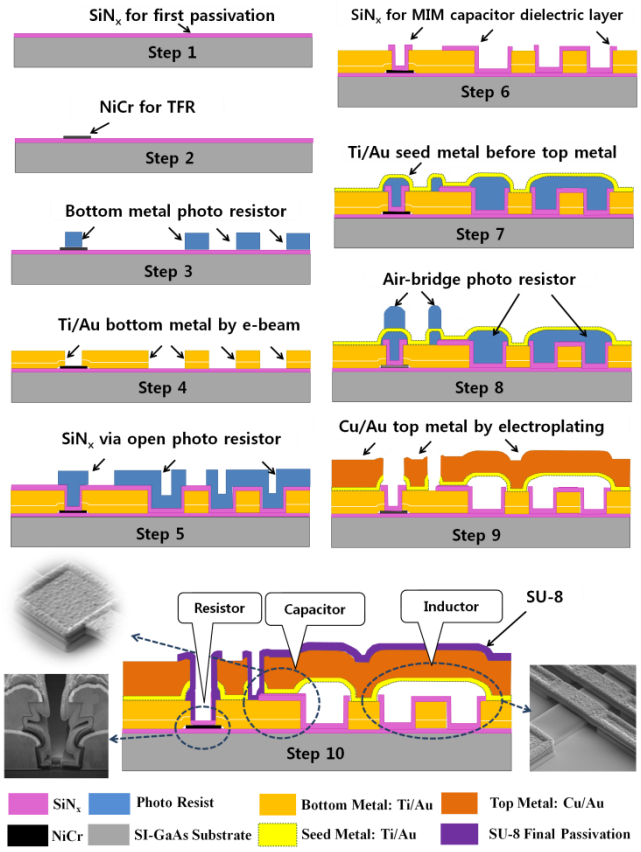

Fig. 4 The optimized IPD fabrication process flow.

an e-beam-evaporated NiCr layer is deposited to obtain the expected TFR (Step 2).

In the next step, the wafer is masked by a photo resistor to define the structures of the bottom metal layer (Step 3). Then, a 50/450 nm-thick Ti/Au metal layer (bottom metal) is used instead of the previous semi-additive method and is formed by e-beam evaporation (Step 4), which is used as the contact metal for the NiCr resistor, the bottom metal layer for the MIM capacitor, and the metal beeline and coils for the spiral inductor. The previous bottom metal layer fabrication procedures were described in [15]. In brief, to improve the bottom metal smoothness, methods such as metal source wiping, source pre-melting, and metal evaporation rate adjustment before e-beam evaporation are used [16]. A 2000 Å SiNx layer is deposited again and then masked to define the dielectric for the MIM-typed capacitor (Step 5). In this step, a pre-deposition treatment is introduced to enhance the reliability and stability of the MIM capacitor [17]. After the deposition step, a reactive ion etching (RIE) step in O_2/SF_6 is performed to remove the undesired layer of SiN_x (Step 6). Next, a 1000 Å-thick Ti/Au seed metal layer followed by an air-bridge post-photo process is deposited by sputtering with a supplementary 30-second sputter-etching before the real seed metal sputter process (Step 7) to reduce the metal peel-off. Then, an air-bridge photo process (Step 8) is performed prior to a Cu/Au (6.5 µm/0.5 µm) top metal definition and plating process by which the top metal and air-bridge are made for the capacitor, and the air-bridge interconnections are formed at the broken coil paths around the metal beeline for the inductor. After the electroplating process, the air-bridge mask is stripped, and the RIE of the Ti/Au seed metal is performed (Step 9). Finally, all

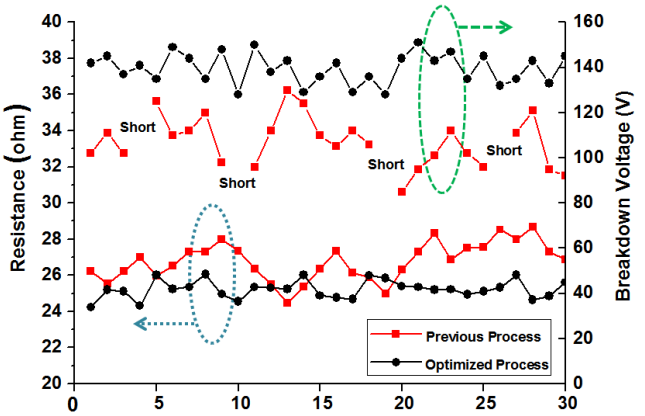

Fig. 5 200 µm × 200 µm TFRs measurement result of resistance and 200 µm × 200 µm MIM capacitors measurement result of breakdown voltage by both the previous and optimized fabrication processes.

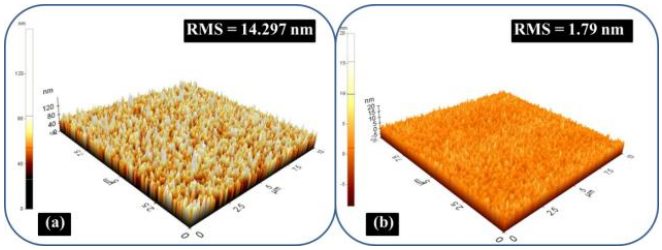

Fig. 6 The three-dimensional (3-D) atomic force microscope (AFM) images of the surface morphology. The images are 3-D AFMs of 10 × 10 µm2 areas: (a) the previous first metal layer roughness with an RMS value of 14.297 nm and (b) the first metal layer roughness after the optimization process with an RMS value of 1.790 nm.

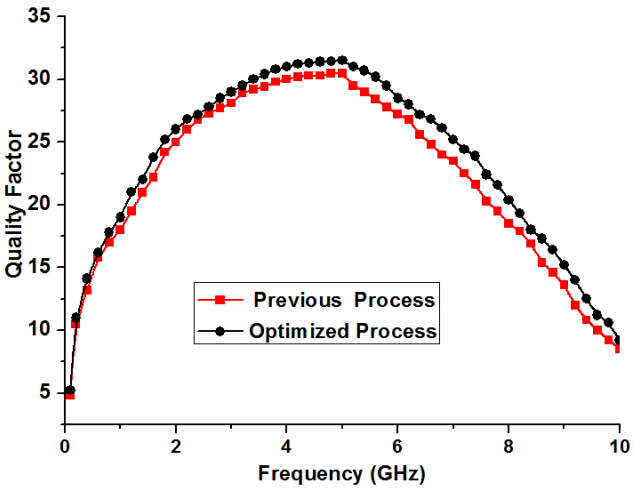

Fig. 7 Fabricated spiral inductor (inner diameter = 150 µm, width = space = 15 µm, turn number = 5, metal thickness = 7.5 µm) measurement result of the Q-factor by both the previous and optimized fabrication processes.

components are passivized with a thickness of 20 µm SU-8 to protect the components from oxidization and moisture (Step 10). The detailed manufacturing process flow of the IPD and information about the layers are shown in Fig. 4.

III. Discussion and Results

The high-quality GaAs substrate and RF passive integration technology of accurate NiCr TFRs, high Q-factor

spiral inductors, and high-breakdown voltage MIM capacitors enable us to realize fully integrated passive functional blocks. Fig. 5 shows the resistances of 200 × 200 μm^2 TFRs and breakdown voltages of 200 × 200 μm^2 MIM capacitors by both the previous and optimized processes. From this figure, it is observed that the sheet resistance of the resistor developed by the optimized process has a greater accuracy of approximately 25 Ω/sq, because all of the seed-related processes (such as seed metal reactive ion etching process) can be avoided and the number of O_2/H_2 cleaning processes can be reduced. With regard to the MIM capacitor, a higher breakdown voltage can be achieved versus the previous process because the breakdown electric field of the MIM capacitors mainly depends on the surface morphology [17]. A rough surface of the bottom metal can create poor coverage during SiNx deposition, which will cause a serous electrical short. In this research, an e-beam evaporation method is applied to realize the bottom metal layer instead of electroplating, which results in a better surface morphology. The first metal layer roughness can be seen in Fig. 6. The root mean square (RMS) value of the surface roughness for the optimized process is approximately 1.790 nm, which is significantly lower than the previously reported data of over 14.297 nm. Fig. 7 shows the Q factor of the fabricated spiral inductors in which the Q factor made by the optimized process is better than the previous fabrication process. Thickness lifting will result in an increasing Q-factor because of the current-crowding effect in spiral rings, which causes part of the current to flow along the edge of the spiral and results in a decreasing series resistance.

After the optimization of components, Fig. 8 (a) demonstrates the device microphotograph of the designed Wilkinson power divider implemented in the IPD process with a chip area of 800 μm × 610 μm. A good implementation of two metal lines inter-wound with a 1.8 μm space between the primary side and secondary side is achieved and could meet our requirement as shown Fig. 8 (b) and (c), which will not introduce additional parasitic effects. The S-parameters of the power divider are extracted from the Agilent network analyzer. Additionally, the wire bonding effect is included in the measurement of the performance for consideration of the actual implementation of the entire process. The measured results for the fabricated bare-chip power divider and packaged power divider are presented in Fig. 9, respectively. The bare-chip measurement results show two insertion losses below 3.35 dB/ 3.40 dB, all return losses of greater than 15.20 dB and an isolation of greater than 38.00 dB. The measured insertion losses for the packaged power divider are better than 3.50 dB/ 3.50 dB around the desired frequency.

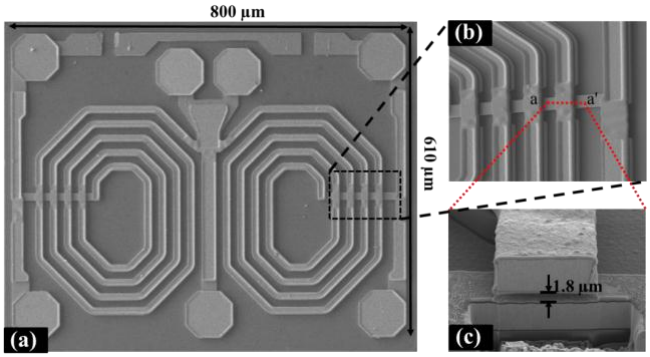

Fig. 8 Focused ion beam (FIB) images of the fabricated IPD Wilkinson power divider: (a) top view, (b) enlarged intertwined air-bridge, and (c) cross-sectional view of the enlarged air-bridge part.

Moreover, the performance of the insertion loss, isolation and VSWR only shows a slight change, which can meet the expected specification. The compared results are shown in Table 1, which shows that the proposed power divider has excellent characteristics because of the advanced and accurate fabrication process and excellent design. Table 2 shows the detailed and packaged measurement results compared to the

Table 1 Summary of several currently published power dividers with a similar frequency band.

Substrate (εr/thickness)	Frequency (GHz)	Insertion loss (S_{21},S_{31}dB)	Return loss (dB)	Isolation (dB)	Size (mm^2)	Reference
Teflon (2.65/1.0 mm)	2.46	3.45/3.34	19.3	14	513	[18]
F4B (2.65/0.8 mm)	2.4	6.16/2.39	15	15	3953	[19]
Teflon (2.65/0.6 mm)	2.4	3.5/3.5	10	10	750	[20]
Teflon (2.65/0.6 mm)	2.4	3.6/3.6	25	30	625	[21]
GaAs (12.85/200 μm)	2.4	3.53/3.4	15.2	38	0.488	This work

Table 2 Summary of the packaged measurement results with the design specifications.

Parameters	Unit	Requirement	Measurement
Frequency	GHz	2.3-2.4	2.24-2.4
Insertion loss (S21/S31)	dB	3.5 (Max)	3.4-3.5
Return loss (S11/S22/S33)	dB	10 (min)	13.5-15.5
Isolation (S23)	dB	20(min)	20-26.2
Port impedance	Ohn	50	50

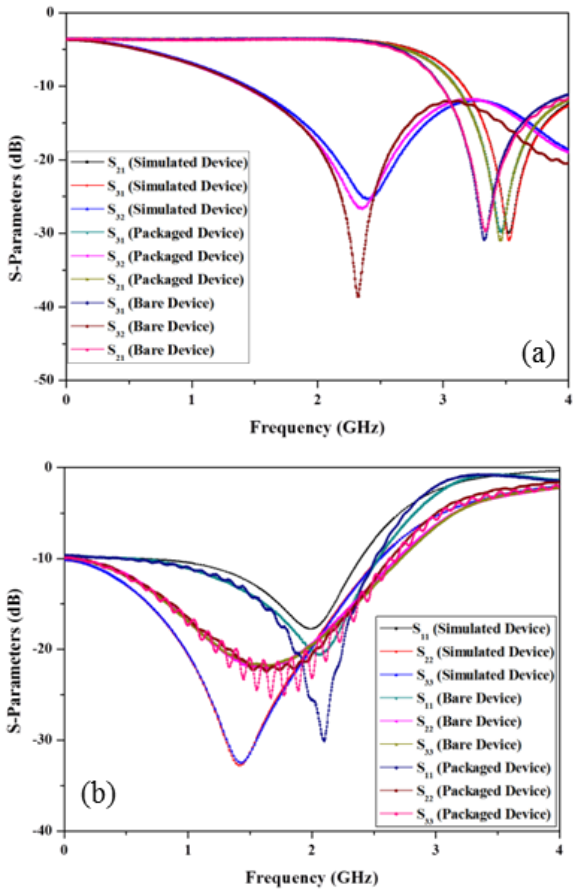

Figure 9. The final S-parameters comparison among the simulated results, measured results of the bare fabricated power divider, and packaged power divider: (a) transmission (S_{21} and S_{31}) and isolation (S_{32}) properties and (b) input matching (S_{11}) and output matching (S_{22} and S_{33}) performances.

I. Conclusion

The demand for cost and yield are constantly pushing all companies in the supply chain to find new solutions for better product competitiveness. Until now, there have been plenty of studies in RF passive integration on IPDs for low-cost, high-yield and mass-production processing. In this paper, we presented the design and implementation of a high-performance, compact Wilkinson power divider using an optimized IPD fabrication process on a GaAs substrate for LTE application. Compared to the conventional IPD process, the proposed fabrication process is developed to further reduce the fabrication time and total fabrication cost and to enhance the reliability and increase the RF performances. Furthermore, the presented Wilkinson power divider is designed and fabricated by using the proposed IPD fabrication technology for the LTE application and reveals excellent characteristics when compared to other works.

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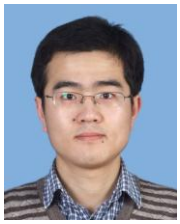
Eun-Seong Kim was born in Seoul, Korea in 1994. He is research assistant of RFIC center in Kwangwoon University. He is currently preparing toward the Master degree at Kwangwoon University, Korea. His current research interests include nano electronic devices, LED packaging, embedded passive devices, bio sensor and system on packaging.

Yang Li was born in Heilongjiang, China, in 1987. He received the B.S. degree in Integrated Circuit Design and Integrated System from Qingdao University of Science & Technology, China, in 2011. He is currently working toward the Ph. D. degree at Kwangwoon University, Korea. His current research interests include microelectronic devices, radio frequency front-end modules, embedded passive devices, and system on packaging.



Zhao Yao was born in Binzhou, China, in 1990. He received the B.S. degree in Communication Engineering from Qingdao University of Science & Technology, China, in 2012. He is currently working toward the Ph. D. degree at Kwangwoon University, Korea. His current research interests include microelectronic devices, integrated passive devices, high-K material, nano-scale crystallite ceramic material and LED packaging.

Nam-Young Kim has received two Masters and two Ph. D. degrees from State University of New York at Buffalo and Midwest University: the M.S. and the Ph.D. in Electronic Engineering. He has also received M. Div and D.C.E. degrees in Theology from Midwest University in 2004 and 2006, respectively. He was a research scientist for CEEM at SUNY at Buffalo in 1994. After completing his research at CEEM at SUNY at Buffalo, Dr. Kim joined the Department of Electronic Engineering of Kwangwoon University as an assistant professor in 1994. His main research focus is in RFIC devices and systems, which use wireless application techniques in order to develop high speed structures in GaAs, Si, and other materials. The founder of the RFIC Education and Research Center, Dr. Kim also serves as director for the Fusion Technology Center. His RFIC research center was honored and sponsored as a ITRC (Information Technology Research Center) by the Ministry of Communication and Information (MIC) of Korea, where he has been acting Director of the RFIC since 2000. He leads the RFIC and RF related Fusion Group at Kwangwoon University, where he has researched along with 22 professors. During his career, he has published almost 130 refereed journal papers and 355 refereed conference papers. Dr. Kim has been issued more than 40 patents and 45 semiconductor design patents. His research fields are in the areas of RF nano device, RFIC, RF biosensor and MMIC design..