Application of Digital System with Clock Speed in Phase Locked Loop Clock Multipliers

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***Abstract*— As the bandwidth demand of computer and digital communications components continues to grow, high-speed serial I/O links are replacing traditional parallel buses. High-performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Phase locked-loops (PLLs) are widely used to generate well-timed on-chip clocks in high-performance digital systems. This paper focuses on the application of Digital System with Clock Speed in the 1-Ghz range relying on the Chip of a Phase Locked Loop Clock Multipliers**

***Index Terms*— Phase Locked Loop, Sequence, Clock, Chips**

I. INTRODUCTION

As the bandwidth demand of computer and digital communications components continues to grow, high-speed serial I/O links are replacing traditional parallel buses. Operating at speeds of giga hertz range, such high-speed I/O circuits are already found in packet switches, circuit switches, and processor-memory interconnects. Hundreds of these high-speed I/Os have been successfully integrated on a single chip enabling monolithic switches with aggregate I/O bandwidths as high as 1 Tb/s. By increasing the bandwidth per package pin and connector pin, high-speed I/Os reduce the system size and cost per unit bandwidth and meet the demand for higher bandwidth computer and communication systems[1]. Highly scaled CMOS devices can only operate from lower voltages and their analog transistor characteristics can be degraded compared to longer channel length devices. This raises many design concerns particularly for conventional analog circuits. On the other hand, CMOS technology scaling still results in significant speed and functional density increases. This opens up many new opportunities for mitigating analog and mixed-mode design challenges using appropriate circuit and design solutions.

Almost all electronic communication and computation devices rely on phase-locked loop (PLL) synthesizers to generate frequency references and clocks. Designing and application of a PLL is a true mixed-signal design challenge covering from high-speed analog and RF blocks (VCO), to high-speed digital blocks (dividers), to low-speed, low-noise analog (charge pump and loop filter) and low-speed digital (phase frequency detector) circuits. In this work, we study the application of digital systems with clock speed in the giga-hertz range relying on ON-CHIPphase locked loop clock multipliers. In particular we focus on scaling the supply voltage, scaling down the area, operation over a frequency range of 1GHZ, and achieving ultra low noise and jitter performance.

An ultra low voltage (ULV) of 1-GHz PLL including a GFSK modulator and implemented in a standard digital 90-nm CMOS technology is first introduced. The design addresses robustness concerns and speed issues due to the aggressive supply voltage scaling (down to 0.5V). Next, a 2.5-GHz ultra-compact analog PLL implemented in a 45-nm CMOS technology is described to demonstrate that area scaling can indeed be achieved in PLLs. The 0.042 square mm fully integrated PLL includes an on-chip LC-VCO and an on-chip passive R-C loop filter. A rigorous methodology for area-scaling LC oscillators by taking advantage of increased transistor speed is described as well as a novel stacked capacitor-inductor device is introduced to further reduce area. In the past thirty years, CMOS has become dominant in commercial, or more specifically, digital IC products. From the fastest microprocessors to the simplest CD4000 by RCA includes two 3-input NOR gates and one inverter. The CD4000 series is for general purpose and currently called 4000 series, which includes both the original CD4000 and HEF4000 series. digital cooking timers, over 99% of today's commercial ICs are fabricated in CMOS, and this dominance is not expected to be changed in the foreseeable future. Because the market of CMOS logic has become so diversified, semiconductor industries developed transistors with different characteristics targeting various applications. High performance (HP) transistors are used in chips where high-speed computation is needed, such as the central processing units (CPUs) in desktop personal computers (PCs) and servers. They have the shortest gate length for highest speed, and the resulting power consumption is also the highest. Low power transistors are used by portable or mobile systems, and they can further be divided into two categories: low operating power (LOP) and low standby power (LSTP). LOP transistors are typically used in relatively high performance mobile systems where larger batteries are available (e.g. laptop computers). This type of transistors emphasizes on lower operating (dynamic) power, and therefore the corresponding supply voltage is the lowest. The gate length is about one year behind HP transistors for the development. LSTP transistors are used in consumer electronics with lower performance and a very limited battery capacity (e.g. cellular phones). Such transistors have the highest threshold voltage and supply voltage to minimize the leakage to achieve a long battery life. The gate length of LSTP logic is about two years behind that of HP logic to develop ultra-low leakage process. The above three types of transistors are thin oxide devices. Most foundries allow only

Manuscript received October 14, 2014.

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one type of thin oxide transistors on the same wafer. On the other hand, analog integrated circuits have evolved from simple amplifiers made of a few transistors to very large mixed-mode systems, which are capable of interfacing the real world for complicated computation systems, handling continuous or discrete time signals, detecting signals as small as nano-volts or pico-amperes, or operating at frequencies beyond 100 GHz. The diversity of analog functions have enabled countless new applications [4-5].

New emerging applications such as software-defined radios or highly integrated test instrumentation require a frequency synthesizer with ultra wide frequency coverage and ultra low phase noise. Two approaches are presented to achieve these challenging design and application objectives by exploiting the capabilities of nanometer transistors. A wideband synthesizer covering from 125 MHz to 32 GHz with a constant jitter performance across the entire frequency range is described; the scaling and design methodologies to achieve constant jitter performance across the ultra-wide frequency range are discussed. Finally, an ultra low noise, two-step synthesizer is presented to show how ultra-low phase-noise fractional-N frequency synthesis can be achieved by taking the full advantage of nano-scale CMOS transistors [2][3].

II. COMPONENTS USED IN THE DESIGN AND APPLICATION

The components of used in this design include:

- A digital system
- Phase locked loop (PLL)
- Analog system
- LDO

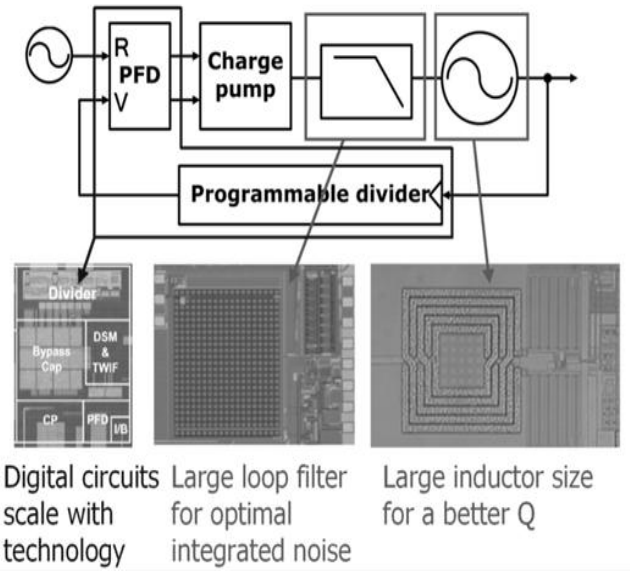

Figure1: A block diagram of a digital system application using a phase locked loop

III. APPLICATION OF DIGITAL SYSTEMS WITH CLOCK BIT PHASE LOCKED LOOP MULTIPLIERS.

The most versatile application of the phase locked loops (PLL) is for clock recovery, clock distribution, clock generation and in digital systems, microprocessor, networking, parallel and serial data communication, and frequency synthesizers. Because of the increase in the speed of the circuit operation, there is a need for a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range and we are going to examine the application of 1GHz clock bit range relying on ON-Chip PLL which must operate in the GHz range with less lock time. The PLL performance and stability of the whole PLL system depends on the order of the loop filter. The voltage controlled oscillator (VCO) is the heart of the PLL[10].

3.1 Clock Recovery System

Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock bit from an approximate frequency reference(1Ghz) and then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery. In order for this scheme to work, the data stream must have a transition frequently enough to correct any drift in the PLL's oscillator.

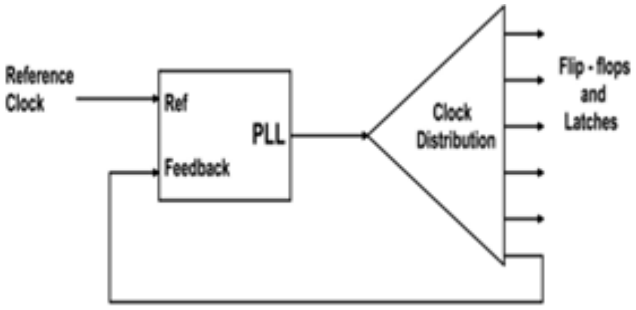

Figure2: Block diagram showing clock distribution using PLL

3.2 Clock Distribution

Typically, the reference clock enters the on chip at a clock bit that drives a phase locked loop (PLL), for the purpose of this paper, we are looking at a digital on chip PLL in the 1GHz range. This then drives the system's clock distribution. The clock distribution is usually balanced so that the clock arrives at every endpoint simultaneously. One of those endpoints is the PLL's feedback input. The function of the PLL is to compare the distributed clock to the incoming reference clock, and vary the phase and frequency of its output until the reference and feedback clocks are phase and frequency matched. PLLs are ubiquitous—they tune clocks in systems several feet across, as well as clocks in small portions of individual chips. Sometimes the reference clock may not actually be a pure clock at all, but rather a data stream with enough transitions that the PLL is able to recover a regular clock from that stream. Sometimes the reference clock is the same frequency as the clock driven through the clock distribution, other times the distributed clock may be some rational multiple of the reference.

3.3 Clock generation

Many electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs,

which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertz and the reference crystal is just tens or hundreds of megahertz.
The innovative three-PLL architecture includes ultra-high resolution pre-scalers, multipliers and output dividers with VCO ranges up to 1GHz to enable nearly any combination of clock scaling ratios from a single input frequency. Two of the internal PLLs include selectable spread-spectrum modulators with fully programmable characteristics, such as spread frequency and ratio. This feature is especially useful to minimize the Electromagnetic interference (EMI) induced by clock signals and enables system designs to meet stringent regulatory requirements. In addition, each PLL also supports programmable loop filter settings to optimize jitter performance in customer applications.

3.4 Frequency Synthesizer

A frequency synthesizer is an electronic system for generating a range of frequencies from a single fixed time base or oscillator. Frequency Synthesizer manufacturers include Analog Devices, National Semiconductor and Texas Instruments. VCO manufacturers include Sirenza, Z-Communications. The design procedure of an 1-GHz phase-locked loop (PLL)-based frequency synthesizer used in IEEE 1394b physical (PHY) system is presented in this paper. The PLL's loop dynamics are analyzed in depth and theoretical relationships between all loop parameters are clearly described. All the parameters are derived and verified by Verilog-A model, which ensures the accuracy and efficiency of the circuit design and simulation. A 4-stage ring oscillator is employed to generate 1-GHz oscillation frequency and is divided into low frequency clocks by a feedback divider. The architecture is a third-order, type-2 charge pump PLL. The simulated settling time is less than 4μs. The RMS value of period jitter of the PLL's output is 2.1 ps. The PLL core occupies an area of 0.12 mm2, one fourth of which is occupied by the MiM loop capacitors. The total current consumption of the chip is 16.5 mA. The chip has been sent for fabrication in 0.13 μm complementary metal oxide semiconductor (CMOS) technology [11][12].

IV. CONCLUSIONS

Phase-locked loops are widely used for synchronization purposes; in space communications for coherent carrier tracking and threshold extension, bi synchronization, and symbol synchronization. Phase-locked loops can also be used to demodulate frequency-modulated signals. In radio transmitters, a PLL is used to synthesize new frequencies which are a multiple of a reference frequency, with the same stability as the reference frequency.

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