Low Area Power -Aware FIR Filter for DSP

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Abstract— Digital signal processing (DSP) is used in wide range of applications such as telephone, radio, video, etc. Most of DSP computations involve the use of multiply accumulate operations and therefore the design of fast and power efficient multiplier is imperative. Moreover, the demand for portable applications of DSP architectures has dictated the need for low power and area designs. Digital Finite Impulse Response (FIR) filter has lot of arithmetic operation modules such as adder and multiplier modules, consume much power, energy, and circuit area. In some applications, the FIR filter circuit must be able to operate at high sample rates while in other applications, the FIR filter circuit must be a low power circuit operating at moderate sample rates.

This paper presents the methods for implementing digital FIR filter that requires optimized area and less power consumptions. Multiplierless Multiple Constant Multiplications (MCM) technique has been used which reduces multiple circuits. The Digit Serial Adder avoids the unwanted addition and thus minimizes the area too. Various filters are designed using MATLAB and implemented using VHDL code. Simulation is performed using ACTIVE -HDL and functional verification is carried out using Synopsis Design Compiler and Encounter compiler.

Index Terms— Digit serial adder, FIR filter, MCM, low area, power, shift and and multiplier

I. INTRODUCTION

With the growing demand on battery powered mobile computing and communication devices, how to achieve low power dissipation in order to extend battery life becomes a major concern of IC designer. DSP systems are widely used in commuting and communication area. FIR filter is one of the basic element in DSP application. Impulse response can either finite or infinite. The method for designing and implementing these two filter classes differ considerably. FIR filters are digital filter whose response to the unit filter (Unit Sample Function) is finite in duration. This is in contrast to Infinite impulse response (IIR) filters whose response to unit impulse is infinite in duration.

FIR and IIR filters each have advantages and disadvantage, and neither is based in all situations. FIR filter can be implemented using either recursive or non-recursive techniques, but usually no recursive technique are used. FIR filters are widely used in DSP systems that are characterized by the extensive sequence of multiplications operations. In some applications, the FIR filter circuit must be able to operate at high sample rates, while in other applications, the FIR filter circuit must be a low power circuit operating at moderate sample rates.

Design of low power, high throughput FIR filter is hot topic in DSP research area. In recent years various technique for low area, low power FIR design have been proposed [1-2]. Bhardwaj et al., [3] introduce the new measurement, power awareness to indicate the ability of the system energy to scale with changing conditions and quality requirements. Parallel (or block) processing can be applied to digital FIR filters to either increase the effective throughput or reduce the power consumptions of the original filters. While sequential FIR filter implementation has been given extensive configuration that deals with directly reducing the hardware complexity or power consumptions of parallel FIR filters [4]. Selecting multiplier with more hardware breadth rather than death would not only reduce the delay, but also the total power consumptions [5]. There is a novel approach for a design method of low power digital base band processing to optimize the bit-width of each filter coefficients [7]. Data transitions power diminution techniques (DPDT) is also used to reduce dynamic switching power of FIR filter [8].

Multiplier plays an important part in today’s DSP systems. Examples of their use occur in implementation of recursive and transverse filters, Discrete Fourier transform, correlation, range measurement and most of these cases it is enough with a multiplier unit design for specific purpose. Multiplier has a large area, long latency and consumes considerable power. Therefore low power multiplier designs have been an important part in low power VLSI system design. The primary objective is power reduction with small area and delay overhead. By using new coding or architectures, it is even possible to achieve both power reduction and area/delay reduction which is strength of high level optimization. In this paper, a novel method to design low area power-aware FIR filter is proposed. Based on pipelining multipliers and adders a very high throughput is achieved. For reduced power consumptions and area we are using MCM technique along with digit serial adder, shift/add multipliers. Various filters are compared for area and power and demonstrated that our approach is most effective for implementation with the constraints of low cost and low power.

II. FIR FILTER THEORY

Digital filters are typically used to modify or alter the attributes of signal in the time or frequency domain. The most common digital filter is the linear time invariant (LTI) filter. LTI interacts with its input signal through process called linear convolution, denoted by $Y=f*x$ where $f$ is the filter impulse response, $x$ is the input signal and $Y$ is the convolved output. The linear convolution process is formally defined by:

$$Y[n]=x[n]*f[n]=\sum_{k=0}^{\infty} x[n-k]f[k]$$

(1)

LTI digital filters are generally classified as FIR or IIR. As the
name implies, FIR filter consists of a finite number of sample values, reducing the above convolution sum to a finite sum per output sample instant. FIR filter with constant coefficients is a LTI digital filter. The output of FIR of order or length L, to an input time-series \( x[n] \) is given by a finite version of the convolution sum given in equation 1 namely,

\[
y[n] = x[n]*f[n] = \sum_{k=0}^{L-1} f[k]x[n-k]
\]  

where \( f[0] \neq 0 \) through \( f[L-1] \neq 0 \) are the filter L coefficients. They also correspond to FIR impulse response. For LTI systems it is some time more convenient to express in the z-domain with

\[
Y(z)=F(z)X(z)
\]  

where \( F(z) \) is the FIR transfer function define in the z-domain by

\[
F(z) = \sum_{k=0}^{L-1} f[k] Z^{-k}
\]  

The Lth order LTI FIR filter is graphically interpreted in Fig 1. It can be seen to consist of a collection of a “tapped delay line”, adders, and multipliers. One of the operands presented to each multiplier is an FIR coefficient often to refer as a “tapped weight” for oblivious reasons. Historically, the FIR filter is also known as by the name “transversal filter”, suggesting its “tapped delay line” structure [9].

In this paper we propose implementations of various FIR filters using various techniques to optimize area and power. Digital filters are composed of adders/subtractors, multipliers and delay elements.

Filter0 is of type 0 is implemented as shown in Fig.2. Here input is delayed and given to multiplier. Each multiplier gives products corresponding to different filter coefficients and all these products are accumulated and give FIR filter output. RTL schematic of filter is shown in Fig.3.

But we can’t test it as it need filter coefficients. So further filter0 is modified to Co-efficient Filter of type I. In this, filter coefficients and finite state machine (FSM) is applied at the input pattern to produce output sequentially. We use filter coefficients from matlab and suitably convert these values into binary for input to design filter. For both the filters we are getting high area and power as given in Table I and Table II. RTL schematic of Co-efficient Filter is shown in Fig.4. Fig 5 shows the FSM pattern applied to input.
Multiplication operation is expensive in terms of area, power and delay. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area [10]. So a multiplierless design in MCM based filter is proposed under multiple constant multiplications architecture. This significantly reduces the area of filters when compared to those designed previously using multiplier blocks. Here sharing of partial terms in multiple constant multiplications (MCMs) concept [11] is used which reduces area and covers all possible partial terms that is used to generate the set of coefficients in MCM instance. Latch is used at the output of design to get output sequentially. Fig 6 shows the RTL schematic of MCM based filter.

Bit-serial systems process one bit of the input sample in one clock cycle, for area efficient and ideal for low speed applications [12]. On the other hand bit-parallel systems process one whole word of the input sample in one clock cycle, are ideal for high speed applications [13]. Both these systems occupy considerable amount of area. To this end, digit serial systems [14] [15] have become attractive for digital designers.

These systems process multiple bits of the input word, referred to as the digit size in one clock cycle. DSP architectures have in need of low-power designs [16] causes the batteries life. Design of digit serial architectures which can be pipelined at the bit-level [17]. The advantage of digit serial architectures is processing in speeds options, less area and critical path is reduced. Therefore, bit adder of previous designed filter is replaced by digit serial adder. RTL schematic of Digit Serial Adder Filter is shown in Fig.7. Fig.8 shows the RTL schematic of digit serial adder.

Realization of FIR filter combining the MCM with shift-add architecture and digit serial adder by using the high-level optimization technique is proposed in final MCM based Digit Serial Adder Filter is shown in Fig 9.
Due to the combination of both the advanced techniques, area and power is drastically reduced as given in Table I and Table II.

IV. SIMULATION AND RESULT

Various filters are implemented using MATLAB and developed VHDL code. Area is calculated using Encounter RTL compiler. Total area of filter is calculated as:

Total cell area=Combinational area +Non-Combinational area

Power estimation is done using Synopsis Design Compiler. Dynamic power is the power dissipated when the circuit is active i.e. performing some function. Dynamic power is further divided into two components: Switching power and internal power. Thus total power for filter is determined as:

Total Dynamic Power=cell internal+net switching power

Area and power of all implemented filters are tabulated as given below in Table I and Table II.

<table>
<thead>
<tr>
<th>Filter Name</th>
<th>Type</th>
<th>Combination Area (µm²)</th>
<th>Non-Combinational Area (µm²)</th>
<th>Total Cell Area (µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter0</td>
<td>0</td>
<td>27050.4519</td>
<td>1404.14563</td>
<td>28454.59</td>
</tr>
<tr>
<td>Co-efficient Filter</td>
<td>1</td>
<td>29009.7793</td>
<td>5616.58252</td>
<td>34626.36</td>
</tr>
<tr>
<td>MCM based Filter</td>
<td>2</td>
<td>15383.1843</td>
<td>5616.58252</td>
<td>20999.76</td>
</tr>
<tr>
<td>Dgit Serial Adder Filter</td>
<td>1</td>
<td>13273.2121</td>
<td>151.114597</td>
<td>13424.32</td>
</tr>
<tr>
<td>MCM based Dgit serial Adder Filter</td>
<td>1</td>
<td>837.700495</td>
<td>151.114597</td>
<td>988.8150</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Filter Name</th>
<th>Cell Internal Power</th>
<th>Net Switching Power</th>
<th>Total Dynamic Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter0</td>
<td>3.4263 mW</td>
<td>2.4014 mW</td>
<td>5.8277 mW</td>
</tr>
<tr>
<td>Co-efficient Filter</td>
<td>7.7737 mW</td>
<td>5.0117 mW</td>
<td>12.7854 mW</td>
</tr>
<tr>
<td>MCM based Filter</td>
<td>1.4735 mW</td>
<td>871.5258 uW</td>
<td>2.3450 mW</td>
</tr>
<tr>
<td>Dgit Serial Adder Filter</td>
<td>4.2176 mW</td>
<td>3.0952 mW</td>
<td>7.3128 mW</td>
</tr>
<tr>
<td>MCM based Dgit serial Adder Filter</td>
<td>113.2492 µW</td>
<td>35.9731 µW</td>
<td>0.1492223 mW</td>
</tr>
</tbody>
</table>

V. CONCLUSION

In this paper various FIR filter are implemented and their speed, power and complexity of the designs are compared. It has been seen that transposed form FIR filter using Digit Serial Adder and MCM with shift and add technique reduces the complexity and area. Proposed design technique for the digit serial architecture in the design of digit-serial operations and FIR filter, yield better performance, with high efficiency. The proposed activity evaluation method leads to consumed low power estimation with fast estimation time. Also the proposed design is an area efficient multiplier useful in decreasing area consequently which reduces the cost.
REFERENCES


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