Low Area Power -Aware FIR Filter for DSP

Ms.Rashmi Patil , Dr.M.T.Kolte

***Abstract*— Digital signal processing (DSP) is used in wide range of applications such as telephone,radio, video, etc. Most of DSP computations involve the use of multiply accumulate operations and therefore the design of fast and power efficient mutiplier is imperative. Moreover, the demand for portable applications of DSP architectures has dictated the need for low power and area designs.Digital Finite Impulse Response (FIR) filter has lot of arithmetic operation modules such as adder and multiplier modules,consume much power, energy,and circuit area.In some applications the FIR circuit must be able to operate at high sample rates while in other applications the FIR filter circuit must be a low power circuit operating at modearte sample rates.**

This paper presents the methods for implementing digital FIR filter that requires optimized area and less power consumptions. Multiplierless Multiple Constant Multiplications (MCM) technique has been used which reduces multiple circuits. The Digit Serial Adder avoids the unwanted addition and thus minimizes the area too. Various filters are designed using MATLAB and implemented using VHDL code. Simulation is performed using ACTIVE -HDL and functional verification is carried out using Synopsis Design Compiler and Encounter compiler.

***Index Terms*— Digit serial adder,FIR filter,MCM,low area,power,shift and and multiplier**

I. INTRODUCTION

With the growing demand on battery powered mobile computing and communication devices, how to achieve low power dissipation in order to extend battery life becomes a major concern of IC designer. DSP systems are widely used in commuting and communication area. FIR filter is one of the basic element in DSP application. Impulse response can either finite or infinite. The method for designing and implementing these two filter classes differ considerably. FIR filters are digital filter whose response to the unit filter (Unit Sample Function) is finite in duration. This is in contrast to Infinite impulse response (IIR) filters whose response to unit impulse is infinite in duration.

FIR and IIR filters each have advantages and disadvantage, and neither is based in all situations. FIR filter can be implemented using either recursive or non-recursive techniques, but usually no recursive technique are used. FIR filters are widely used in DSP systems that are characterized by the extensive sequence of multiplications operations. In some applications, the FIR filter circuit must be able to operate at high sample rates, while in other applications, the FIR filter circuit must be a low power circuit operating at moderate sample rates.

Manuscript received September 19, 2014.

Ms.Rashmi Patil B. Eng. Degree in Electronics & Communication fromS.S.G.M.C.E.Shegaon, India

Dr.M.T.Kolte B.Tech, M.E., and Ph.D in Electronics and Telecommunication. Head of Dept.in M.I.T.C.O..E.,Pune,India.

Design of low power, high throughput FIR filter is hot topic in DSP research area. In recent years various technique for low area, low power FIR design have been proposed [1-2]. Bhardwaj et al., [3] introduce the new measurement, power awareness to indicate the ability of the system energy to scale with changing conditions and quality requirements. Parallel (or block) processing can be applied to digital FIR filters to either increase the effective throughput or reduce the power consumptions of the original filters. While sequential FIR filter implementation has been given extensive configuration that deals with directly reducing the hardware complexity or power consumptions of parallel FIR filters [4]. Selecting multiplier with more hardware breadth rather than death would not only reduce the delay, but also the total power consumptions [5]. There is a novel approach for a design method of low power digital base band processing to optimize the bit-width of each filter coefficients [7]. Data transitions power diminution techniques (DPDT) is also used to reduce dynamic switching power of FIR filter [8].

Multiplier plays an important part in today's DSP systems. Examples of their use occur in implementation of recursive and transverse filters, Discrete Fourier transform, correlation, range measurement and most of these cases it is enough with a multiplier unit design for specific purpose. Multiplier has a large area, long latency and consumes considerable power. Therefore low power multiplier designs have been an important part in low power VLSI system design. The primary objective is power reduction with small area and delay overhead. By using new coding or architectures, it is even possible to achieve both power reduction and area/delay reduction which is strength of high level optimization. In this paper, a novel method to design low area power-aware FIR filter is proposed. Based on pipelining multipliers and adders a very high throughput is achieved. For reduced power consumptions and area we are using MCM technique along with digit serial adder, shift/add multipliers. Various filters are compared for area and power and demonstrated that our approach is most effective for implementation with the constraints of low cost and low power.

II. FIR FILTER THEORY

Digital filters are typically used to modify or alter the attributes of signal in the time or frequency domain. The most common digital filter is the linear time invariant (LTI) filter. LTI interacts with its input signal through process called linear convolution, denoted by Y=f*x where f is the filter impulse response, x is the input signal and Y is the convolved output. The linear convolution process is formally defined by:

$$Y[n]=x[n]*f[n]=\sum_{k=0} x[n]f[n-k]=\sum_{k=0} f[k]x[n-k] \quad (1)$$

LTI digital filters are generally classified as FIR or IIR.As the

name implies, FIR filter consists of a finite number of sample values, reducing the above convolution sum to a finite sum per output sample instant. FIR filter with constant coefficients is a LTI digital filter. The output of FIR of order or length L, to an input time-series x[n] is given by a finite version of the convolution sum given in equation 1 namely,

$$y[n]=x[n]*f[n]=\sum_{k=0}^{L-1} f[k]x[n-k] \qquad (2)$$

where f[0] ≠ 0 through f[L-1] ≠0 are the filter L coefficients. They also correspond to FIR impulse response. For LTI systems it is some time more convenient to express in the z-domain with

$$Y(z)=F(z)X(z) \qquad (3)$$

where F[z] is the FIR transfer function define in the z-domain by

$$F(z)=\sum_{k=0} f[z]\, z^{-k} \qquad (4)$$

The Lth order LTI FIR filter is graphically interpreted in Fig 1. It can be seen to consist of a collection of a "tapped delay line", adders, and multipliers. One of the operands presented to each multiplier is an FIR coefficient often to refer as a "tapped weight" for oblivious reasons. Historically, the FIR filter is also known as by the name "transversal filter", suggesting its "tapped delay line" structure [9].

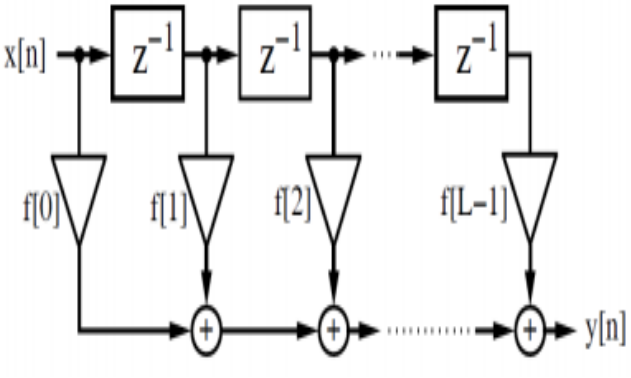

Figure 1. FIR filter in the transposed structure

III. FIR FILTER IMPLEMENTATION

In this paper we propose implementations of various FIR filters using various techniques to optimize area and power. Digital filters are composed of adders/subtractors, multipliers and delay elements.

Filter0 is of type 0 is implemented as shown in Fig.2.Here input is delayed and given to multiplier .Each multiplier gives products corresponding to different filter coefficients and all these products are accumulated and give FIR filter output.RTL schematic of filter is shown in Fig.3.

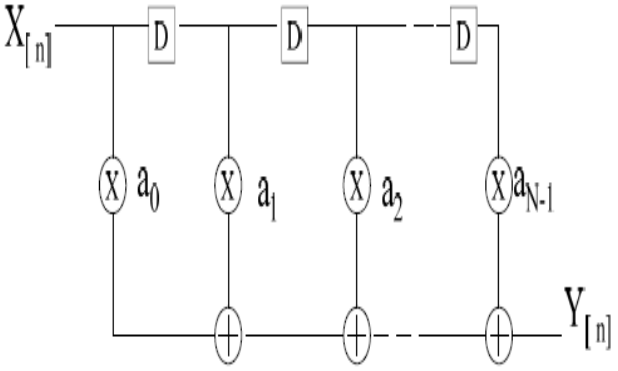

Figure 2. Filter0

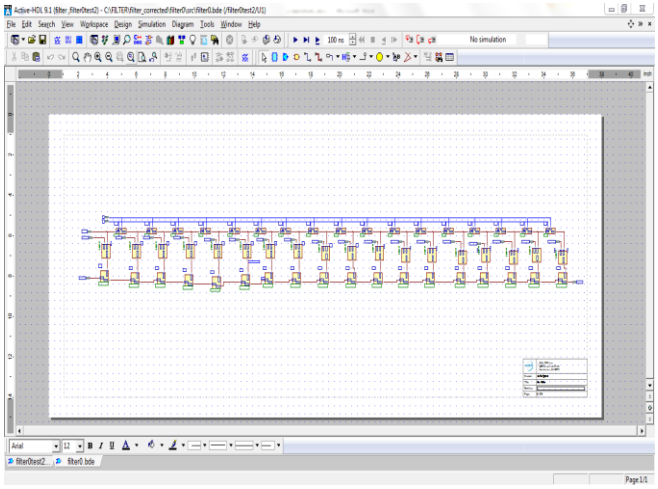

Figure 3. RTL schematic of Filter0

But we can't test it as it need filter coefficients. So further filter0 is modified to Co-efficient Filter of type 1.In this, filter coefficients and finite state machine (FSM) is applied at the input pattern to produce output sequentially. We use filter coefficients from matlab and suitably convert these values into binary for input to design filter. For both the filters we are getting high area and power as given in Table I and Table II.RTL schematic of Co-efficient Filter is shown in Fig.4.Fig 5 shows the FSM pattern applied to input.

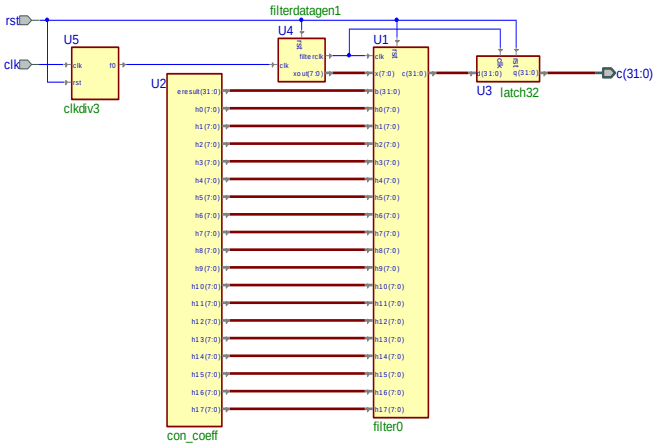

Figure 4. RTL schematic of Co-efficient Filter

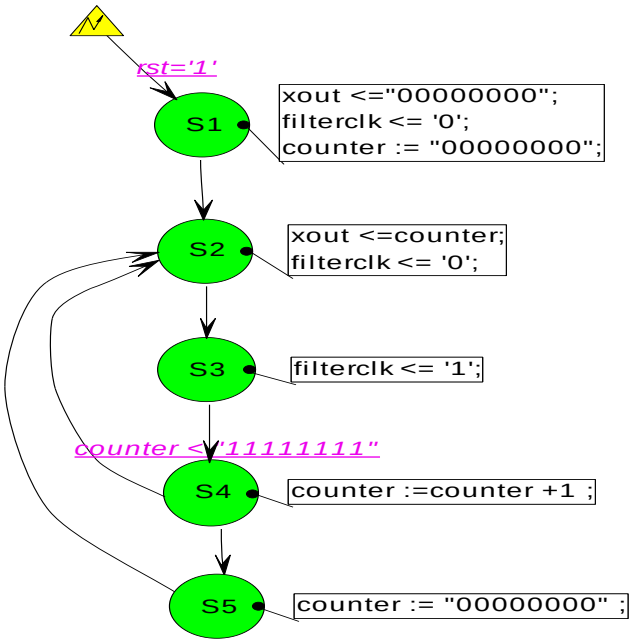

Figure 5. FSM pattern applied to input

Multiplication operation is expensive in terms of area, power and delay. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area [10].So a multiplierless design in MCM based filter is proposed under multiple constant multiplications architecture. This significantly reduces the area of filters when compared to those designed previously using multiplier blocks. Here sharing of partial terms in multiple constant multiplications (MCMs) concept [11] is used which reduces area and covers all possible partial terms that is used to generate the set of coefficients in MCM instance. Latch is used at the output of design to get output sequentially. Fig 6 shows the RTL schematic of MCM based filter.

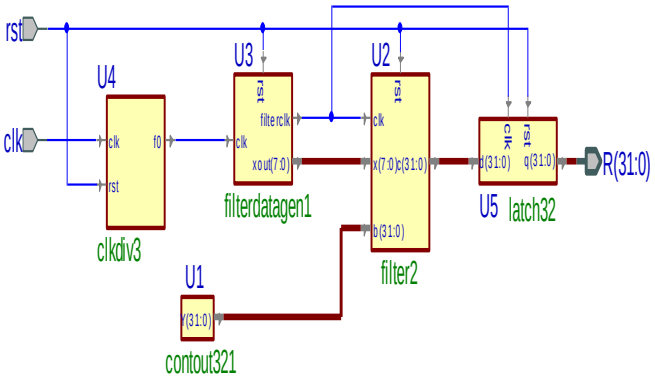

Figure 6. RTL schematic of MCM based filter

Bit-serial systems process one bit of the input sample in one clock cycle, for area efficient and ideal for low speed applications [12].On the other hand bit-parallel systems process one whole word of the input sample in one clock cycle, are ideal for high speed applications[13].Both these systems occupy considerable amount of area. To this end, digit serial systems [14] [15] have become attractive for digital designers.

These systems process multiple bits of the input word, referred to as the digit size in one clock cycle.DSP architectures have in need of low-power designs [16] causes the batteries life. Design of digit serial architectures which can be pipelined at the bit-level [17]. The advantage of digit serial architectures is processing in speeds options, less area and critical path is reduced. Therefore, bit adder of previous designed filter is replaced by digit serial adder.RTL schematic of Digit Serial Adder Filter is shown in Fig.7.Fig.8 shows the RTL schematic of digit serial adder.

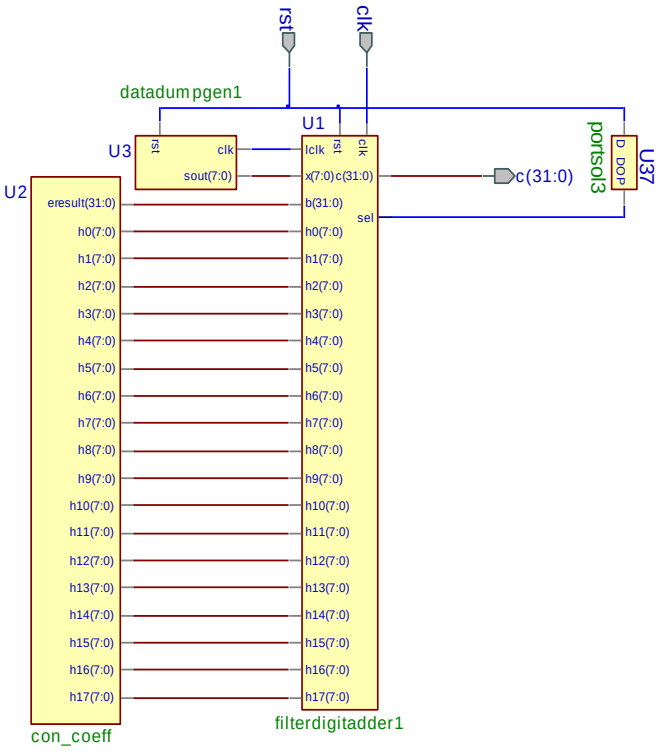

Figure 7. RTL Schematic of Digit Serial Adder Filter

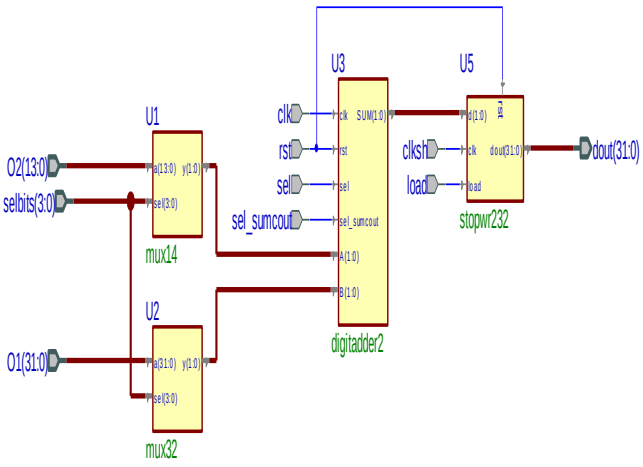

Figure 8. RTL schematic of digit serial adder

Realization of FIR filter combining the MCM with shift-add architecture and digit serial adder by using the high-level optimization technique is proposed in final MCM based Digit Serial Adder Filter type1.RTL schematic of final proposed FIR filter is shown in Fig 9.

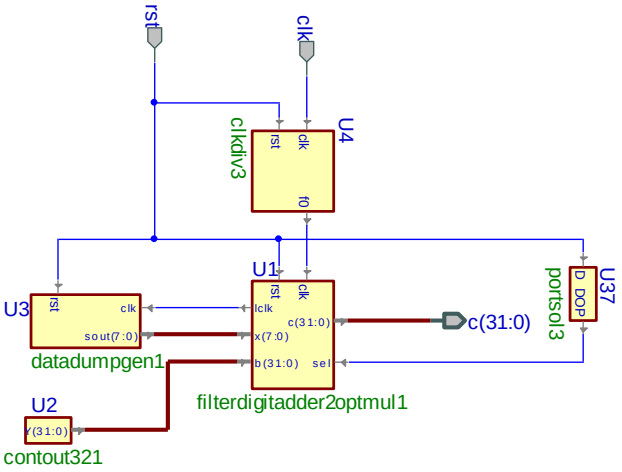

Figure 9. RTL schematic of MCM based Digit serial Adder Filter

Due to the combination of both the advanced techniques, area and power is drastically reduced as given in Table I and Table II.

IV. SIMULATION AND RESULT

Various filters are implemented using MATLAB and developed VHDL code. Area is calculated using Encounter RTL compiler. Total area of filter is calculated as:
Total cell area=Combinational area +Non-Combinational area

Power estimation is done using Synopsis Design Compiler. Dynamic power is the power dissipated when the circuit is active i.e. performing some function .Dynamic power is further divided into two components: Switching power and internal power. Thus total power for filter is determined as:
Total Dynamic Power=cell internal+net switching power
Area and power of all implemented filters are tabulated as given below in Table I and Table II.

TABLE I.
Comparison Table for Area

Filter Name	Type	Combinational Area (μm^2)	NonCombinational Area (μm^2)	Total Cell Area (μm^2)
Filter0	0	27050.45198	1404.14563	28454.59761
Co-efficient Filter	1	29009.77936	5616.58252	34626.36188
MCM based Filter	2	15383.18436	5616.58252	20999.76688
Digit Serial Adder Filter	1	13273.21216	151.114597	13424.32676
MCM based Digit serial Adder Filter	1	837.700495	151.114597	988.815092

TABLE II.
Comparison Table for Power

Filter Name	Cell Internal Power	Net Switching Power	Total Dynamic Power
Filter0	3.4263 mW	2.4014 mW	5.8277 mW
Co-efficient Filter	7.7737 mW	5.0117 mW	12.7854 mW
MCM based Filter	1.4735 mW	871.5258 uW	2.3450 mW
Digit Serial Adder Filter	4.2176 mW	3.0952 mW	7.3128 mW
MCM based Digit serial Adder Filter	113.2492 µW	35.9731 µW	0. 1492223 mW

Simulation result for proposed MCM based Digit Serial adder filter in Active HDL is shown in Fig 10.

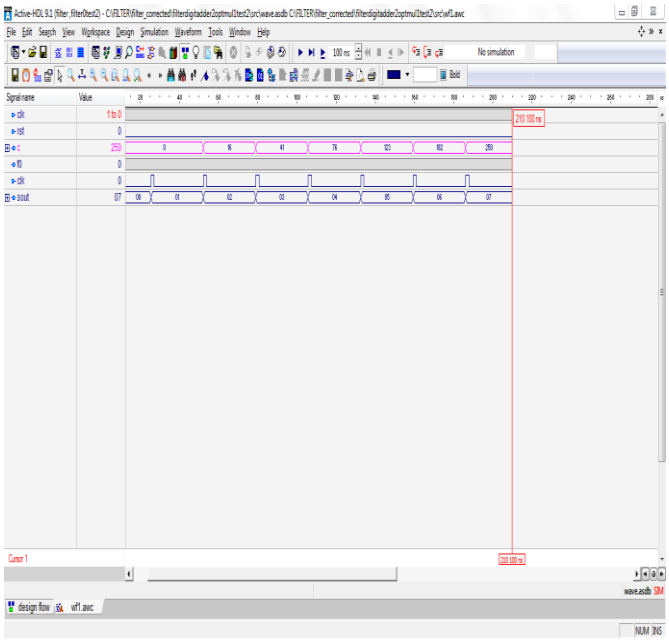

Figure 10. Simulation result for proposed MCM based Digit Serial adder filter

V. CONCLUSION

In this paper various FIR filter are implemented and their speed, power and complexity of the designs are compared. It has been seen that transposed form FIR filter using Digit Serial Adder and MCM with shift and add technique reduces the complexity and area. Proposed design technique for the digit serial architecture in the design of digit-serial operations and FIR filter, yield better performance, with high efficiency. The proposed activity evaluation method leads to consumed low power estimation with fast estimation time. Also the proposed design is an area efficient multiplier useful in decreasing area consequently which reduces the cost.

REFERENCES

[1] T. Arslan, et al. “Low power implementation of high throughput FIR filters”, IEEE International Symposium on Circuits and Systems, 2002, vol. 4, pages 373-376
[2] Ludwig J. T., et al. “Low power digital filtering using approximate processing”, IEEE Journal of Solid-State Circuits, vol. 31, no. 3, pp. 395-399, 1996
[3] Manish Bhardwaj, et al. “Quantifying and EnhancingPower Awareness of VLSI Systems”. IEEE Transactions on VLSI Systems. 2001, Volume 9, Issue 6, pages 757-772.
[4] H. J. G. Chung and K. K. Parhi, “Frequency spectrum based low-area low-power parallel fir filter design,” EURASIP Journal on Applied Signal Processing 2002, vol. 31, pp. 944-953.
[5] A. F. Shalash and K. K. Parhi, “Power efficient folding of pipelined LMS adaptive filters with applications,” Journal of VLSI Signal Processing, pp. 199-213, 2000.
[7] K. Tarumi, A. Hyodo, M. Muroyama, and H. Yasuura, “A design method for a low power digital FIR_lter indigital wireless communication systems,” 2004.
[8] A. Senthilkumar, A. M. Natarajan, and S. Subha, “Design and implementation of low power digital FIR filters relying on datatransition power diminution technique,” DSP Journal, vol. 8, pp. 21-29, 2008.
[9] Uwe Meyer-Baese, “Digital Signal with Field Programmable Gate Arrays”, Springer-Verlag Berlin Heidelberg 2007
[10] Y. Tsao and K. Choi, “Area-efficient VLSI implementation for parallel linear-phase FIR digital filters of odd length based on fast FIR algorithm,” IEEE Transactions on Circuits and Systems
II: Express Briefs, vol. 59, no. 6, pp. 371–375, 2012.
[11] K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, JohnWiley & Sons, 2007.
[12] H. Nguyen and A. Chatterjee, "Number Splitting with Shift-and-Add Decomposition for Power and Hardware Optimization in Linear DSP Synthesis," IEEE Trans
[13] R. Hartley,” Subexpression Sharing in Filters using Canonic Signed Digit Multiplier,” IEEE TCASII
[14] L. Aksoy, E. Costa, P. Flores, and J. Monteiro "Exact and Approximate Algorithms for the Optimization of Area and Delay in Multiple Constant Multiplications," IEEE TCAD.
[15]A. Dempster and M. Macleod’ “Use of Minimum Adder Multiplier Blocks in FIR Digital Filters," IEEE TCAS II.”
[16] Y. Voronenco and M Piischel,” Multiplierless Multiple Constant Multiplier”, ACM Transactions on Algorithms.
[17] R. Hartley and K. Parhi, Digit Serial Computation, Kluwer Academic Publications,1995.

Ms.Rashmi Patil received her B. Eng. Degree in Electronics & Communication fromS.S.G.M.C.E.Shegaon, India in 2010 and M.Tech degree in Electronics from R.T.M.N.U.Nagpur, India. Currently she is a research scholar in B.D.C.O.E.,Sewagram, India. Her area of interest are applied electronics,VLSI, VHDL, and Low Power optimization.

Dr.M.T.Kolte has completed his B.Tech, M.E., and Ph.D in Electronics and Telecommunication.He is working as Head of Dept.in M.I.T.C.O..E.,Pune,India.He has presented and published many papers in National and International Conference.