Optimize the Speed and Power of A/D converter using Multistage pipelining Architecture

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***Abstract*— In this project, I optimized the power and speed of analog to Digital converter using pipe lining Power dissipation has emerged the most critical design constraint in morden VLSI system while traditionally more critical for battery-operated applications, power dissipation has become a universally important design metric due to growing power density in today's VLSI as well as the limited cooling and power delivery capacity of the package .this thesis present a multilevel design optimization of a pipelined analog to digital converter**

***Index Terms*— Analog to Digital converter ,Pipelining, VHDL, Xilinx.**

I. INTRODUCTION

An A/D converter does the inverse function of a D/A converter. It converters an analog signal in to its equivalent n-bit binary coded digital output signal .The analog input is sampled at a frequency much higher than the maximum frequency component of the input signal. The output from an A/D converter can be in serial or parallel from

II. EDA TOOL

A. OBJECTIVES OF THE TOOL:-

1. To calculate The delay of Analog to digital converter
2. To get Test bench wave form .
3. We will use Xilinx and Power estimator to calculate the speed and power

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B. TYPES OF ANALYSIS THAT CAN BE PERFORMED:-

Three basic types of analysis are:

1. Speed(ns)
2. Power(Mw)
3. Area on Device (%)

III. RESULTS:

A. Analog To Digital converter without Pipeline

I am taking the Analog to Digital converter in which Input is the sine wave .The voltge level of Sine wave is the 15Volt.

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The Delay is calcuted by using Xilinx , The calculated Delay of Analog to Digital Converter is 17.516ns The main Aim to Reduce that Delay . This Delay is reduced by Pipeline method in Analog to Digital converter.

The RTL of Analog to Digital converter is Simulated by Xilinx so The RTL of Analog to Digital converter is given in following Fig.

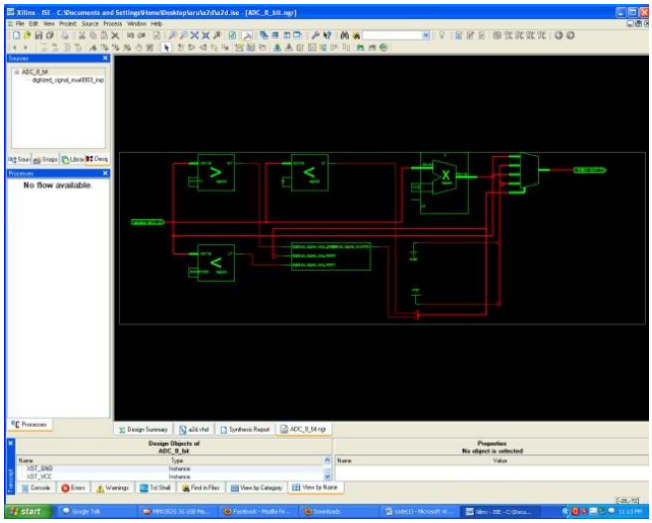

Fig 3.1: RTL Diagram of Analog to Digital converter

In this RTL Digram , there is input which is in Analog form and that Analog signals are converted in Digital form

The test bench of Analog to Digital converter is given below

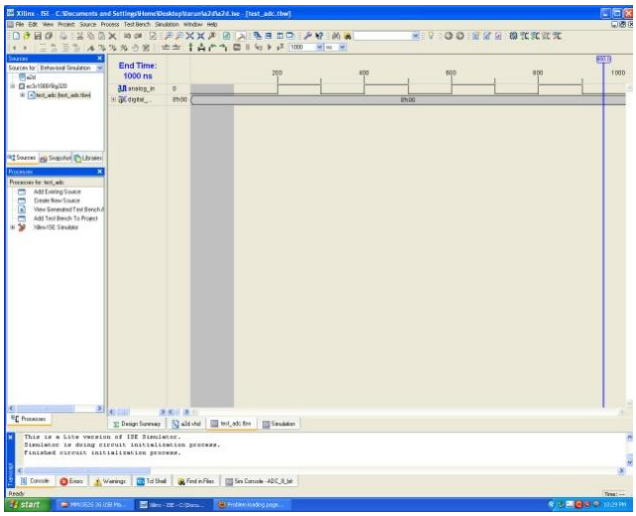

Fig 3.2 : Test bench of Analog to Digital converter

Simulation wave form of Analog to Digital converter

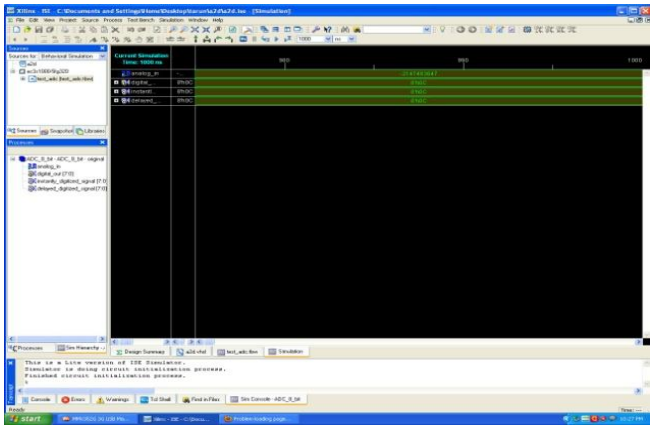

Fig3.3: Simulation of Analog to Digital converter

Power Calculation In Analog to Digital Converter

The power is calculated by using X Power Estimator which is provided by Xilinx ISE,This is looks like Excel sheet. Before Calculating the Power , We have to Create the Adc_8bit _map.mrp file by clicking the option "Generate programming file " option on the Xilinx window.After calculation the Power by Xilinx Power Estimator(XPE)_11.1

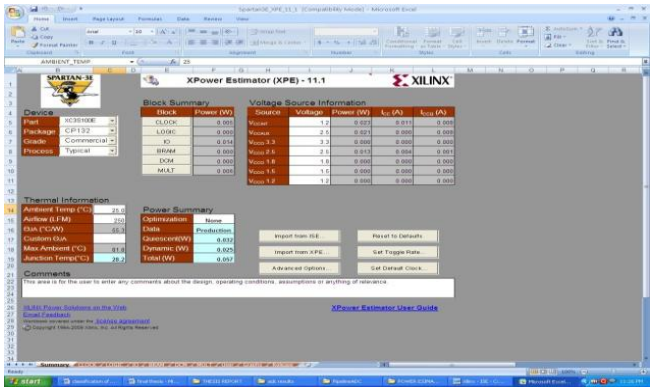

Fig 3.4 Xilinx Power Estimator window(XPE)_11.1

The power consumed by Power Calculation In Analog to Digital Converter **57 mili volt**,which is reduced by using pipe line Method .

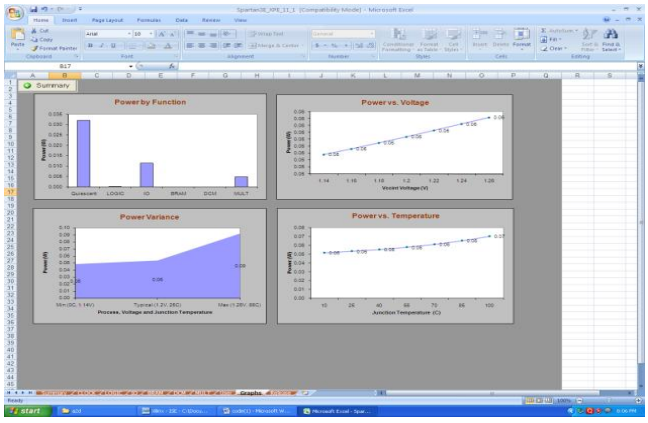

Fig 3.5: Power Function Graph

This is the Power Function Graph, wich is Created by X Power Estimator window(XPE)_11.1 also.

B. Analog To Digital converter with Pipeline

A pipeline is a set of data processing elements connected in series, so that the output of one element is the input of the next one. The pipeline created by dividing a complex operation into simpler operations. We can also say that instead of taking a bulk thing and processing it at once, we break it into smaller pieces and process it one after another.

In previous Result in simple ADC , The speed was 17.516ns that was too high. Bt the speed is The most important parameter for Any Analog to Digital converter .so We have to reduced Delay And increased the speed of Analog to Digital converter

From The Synthesis Report ,the Total Delay of Analog to Digital converter is About **6.216ns**. This achieve by Using Pipeline .

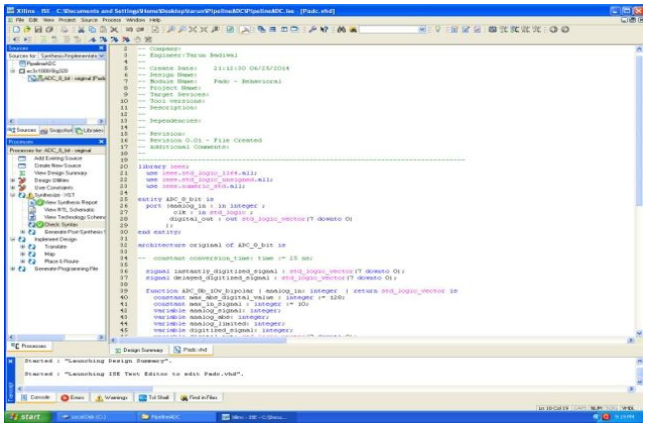

Fig 3.6: Xilinx Window of Pipe line Analog to Digital converter

RTL Logic Diagram of Pipe line ADC

The RTL of Analog to Digital converter is Simulated by Xilinx Fig

In this RTL Digram , there is input which is in Analog form and that Analog signals are converted in Digital form.The main difference between RTL of ADC and Pipeline ADC is Clock Plus .

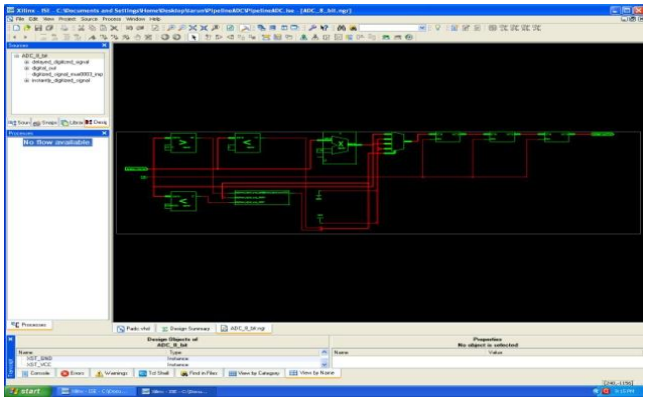

Fig3.7: RTL Diagram of Pipe line Analog to Digital converter

Power Calculation In Pipe lined Analog to Digital Converter:-

The power is calculated by using X Power Estimator which is provided by Xilinx ISE,This is looks like Excel sheet. Before Calculating the Power , We have to Create the Adc_8bit _map.mrp file by clicking the option "Generate programming file " option on the Xilinx window

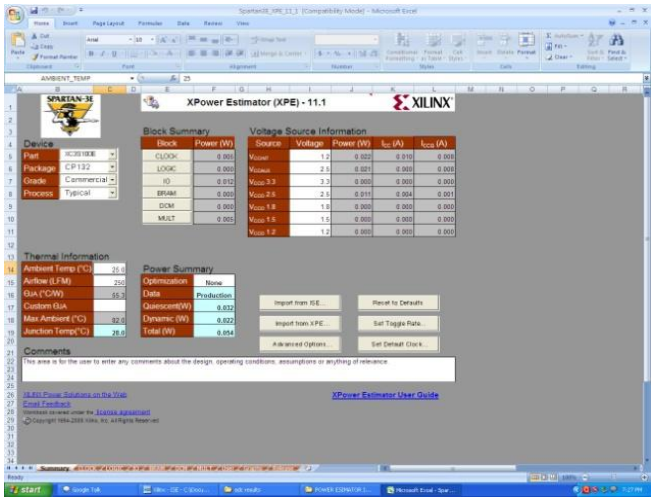

Fig 3.8: Power Calculation In Pipe line Analog to Digital Converter

After calculation the Power by X Power Estimator(XPE)_11.1, The power consumed by Power Calculation In Analog to Digital Converter **54 mili volt**,which is less then Analog to Digital converter Without pipe line

C. Conclusion and Future Scope

The Aim is to increased the speed and optimization of Power dissipation in A to D converter because the A to D converter is the important part in any digital circuit .To increase the Power and speed We have increased signal to noise ratio.

	Speed (ns)	**POWER (Mw)**	**AREA on Device (%)**
Analog to Digital Converter	17.516 ns	58 (Mw)	0.46
Pipe line Analog to Digital Converter	6.216 ns	54(Mw)	0.31

Table 3.1: The comparison of Speed(ns) and Power(Mw) And Area between ADC and Pipe line ADC

As we know that Power minimization play important role in any Digital system and Analog to Digital converter can be apply in Real time application so it can be more beneficial in many application. so Finally I Reduced the delay of ADC(which was **17.516 ns** before using Pipe line) to the **6.216 ns.** With the Reduction of Delay I reduced the Power from **58 mw** to the **54 mw** using Pipe line method.

D. Results in Graph Form

a) Comparison of Speed

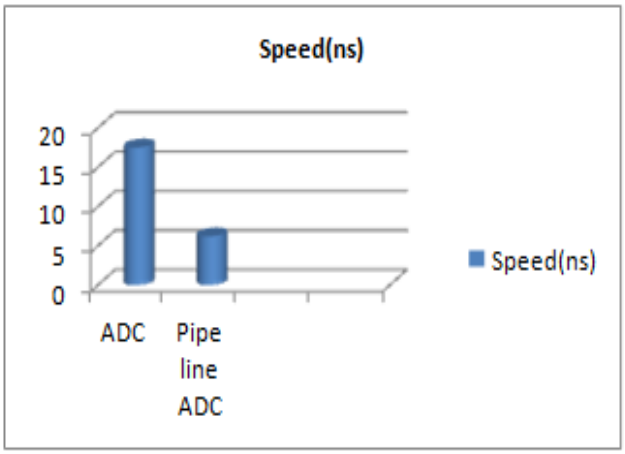

Fig 3.9:The comparison of Speed between ADC and Pipeline ADC

b) Comparison of Power

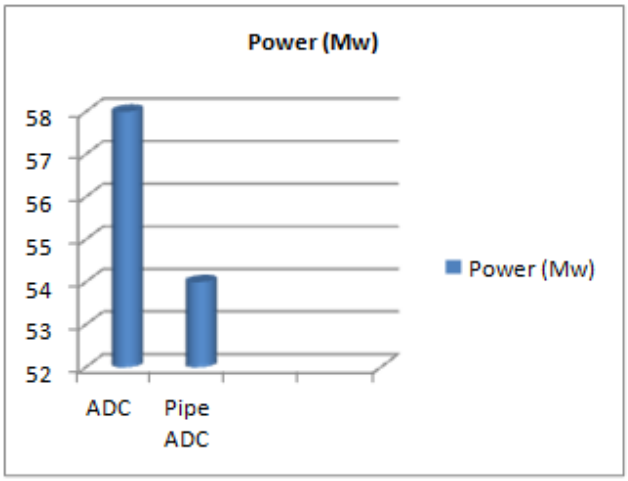

Fig 3.10: The comparison of Power(Mw) between ADC and Pipeline ADC

c) Comparison of Speed and Power

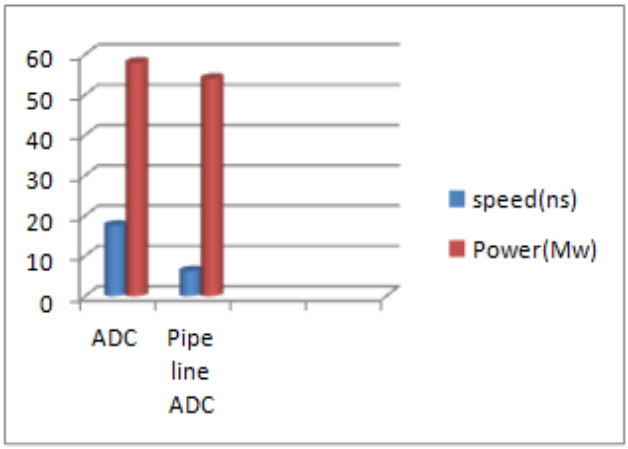

Fig : 3.11The comparison of Speed and Power(Mw) between Analog to Digital converter and Pipe line ADC

This is comparison of Speed and Power(Mw) between Analog to Digital converter which is Representing by Graph and it's the final Result of Thesis.

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