Power Optimized Memory Organization Using Clock Gating

Lucky Khandelwal, Arpan Shah, Ramesh Bharti

***Abstract*— This project presents circuit design of a low-power dual port memory. The planned memory uses new techniques to reduce its power consumption. Since memories are accessed sequentially, it adopts a separate address bus for read and writes process. A novel gated-clock-driver is then applied to further reduce the activity along the clock allocation network. Moreover, the gated-driver idea is also employed in the input ports of the memory block to decrease their loading, thus saving even more power. A D-flip flop and AND gate circuit is used for driver.**

***Index Terms*—A D FlipFlop, and gate circuit, clock allocation network.**

I. INTRODUCTION

Portable multimedia and communication devices have experienced explosive growth recently. Longer battery life is one of the crucial factors in the extensive success of these products. As such, low-power circuit design for multimedia and wireless communication applications has become very important. In many such products, memories make up a significant portion of their circuits [1]–[3]. Such serial access memory is needed in temporary storage of signals that are being processed, e.g., delay of one line of video signals, delay of signals within a fast Fourier transform (FFT) architectures [4], and delay of signals in a delay correlator [2]. Currently, most circuits adopt static random access memory (SRAM) plus some control/addressing logic to implement delay buffers. In this paper, we propose to use clock gating technique. A novel approach using the D-flip flop instead of the R–S flip-flops in the control logic for generating the clock-gating signals is adopted to avoid increasing the loading of the global clock signal. In the proposed new memory, we use a tree hierarchy for the read/write circuitry of the memory module. For the write circuitry, in each level of the driver, only one driver along the path leading to the addressed memory word is activated. Simulation results show the effectiveness of the above become very important. Such serial access memory is needed in temporary storage of signals that are techniques in power reduction. As an example, a 256 8 delay buffer chip is designed and fabricated. Measured results indicate its much better power performance than the same-size delay buffer based on existing commercial SRAM. The rest of this paper is organized as follows. Section II first introduces the conventional architecture for implementing Memory. Next, the proposed memory and gated driver for the read and write circuits of the memory module is described in Section III.Section then presents experimental results of the new memory. Also, comparison in power and area of the new delay buffer with conventional SRAM are given. Section IV then concludes this paper.

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II. CONVENTIONAL MEMORY

A RAM is a dedicated two port memory containing 256x8 bit. A conventional memory is designed in VHDL the simulation result are calculated on Xilinx 9.2 simulator which is as Follow

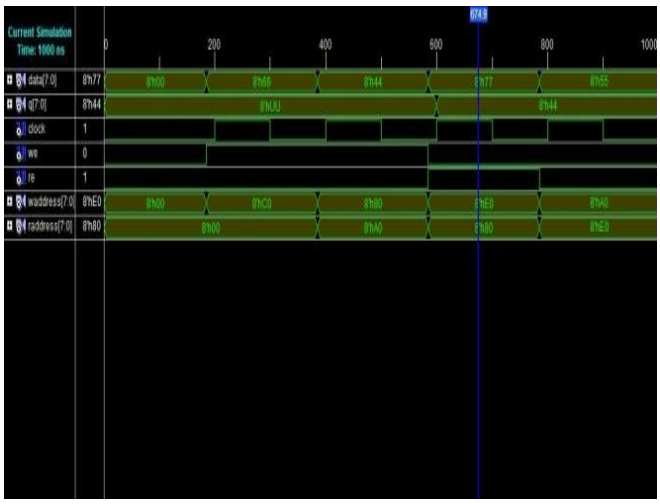

Fig 1- Simulation result of basic memory

RTL diagram of conventional memory is shown below.

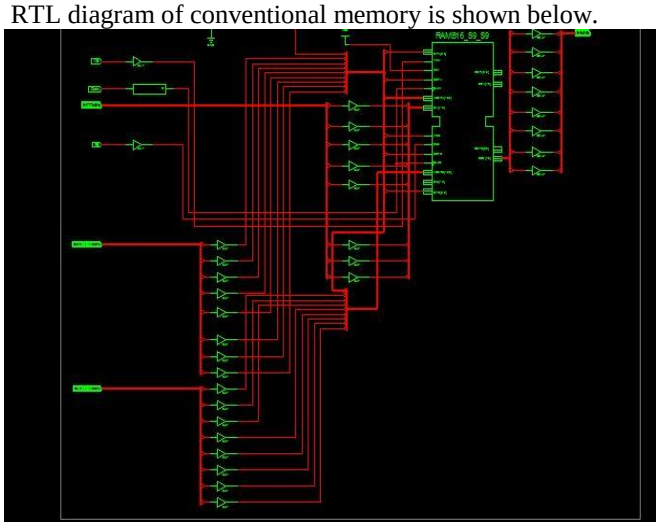

Fig 2- RTL Schematics of basic memory

A two port memory is design by conventional method the power consumption is as follow

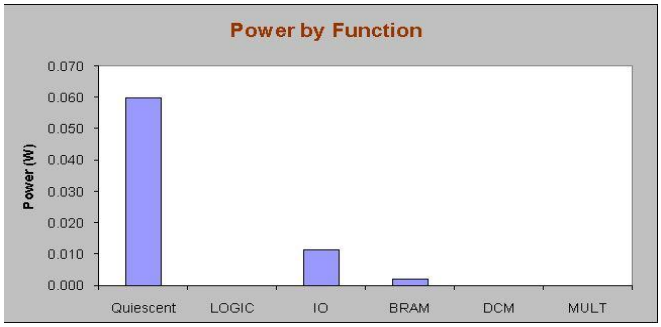

Fig 3- Power analysis of basic memory

The quiescent power of above describe design is .060 w and dynamic power is 0.019w the total consumption is 0.079w.

Resource Utilization

Number of Slices: 0 out of 3584 0%
Number of IOs : 35
No. of bonded IOBs : 35 out of 173 20%
Number of BRAMs :1 out of 16 6%
Number of GCLKs : 1 out of 8 12%

III. PROPOSED MEMORY

Although some power is indeed saved by gating the clock signal in inactive blocks, the extra D flip-flops still serve as loading of the clock signal and demand more than necessary clock power. We propose to replace the R–S flip-flop by a D flip-flop and to use tree structured clock drivers with gating so as to greatly reduce the loading on active clock drivers. Additionally, D flip-flops are used to reduce the clock spikes and thus also reduce the power consumption on the clock signal.

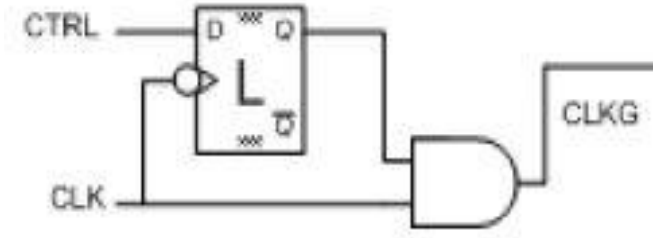

Fig 4 Concept of clock Gating

The proposed memory clock gating and the control logic is shown in Fig. 5. Each block contains one D-flip flop to control the delivery of the local clock signal "CLK "to the memory, and only the "Latch signals along the path passing the global clock source to the local clock signal are active. The output of D- flip flop and global clock feed to AND gate which generate local clock signal for memory.

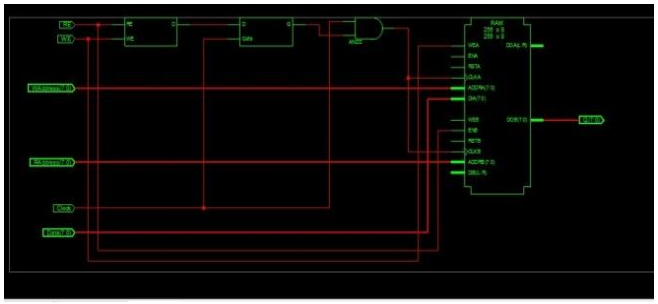

Fig 5- RTL Schematic of proposed memory

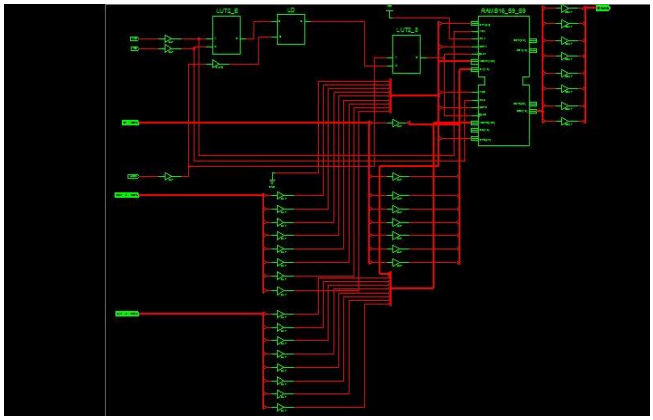

Fig 6- Detail RTL Schematics

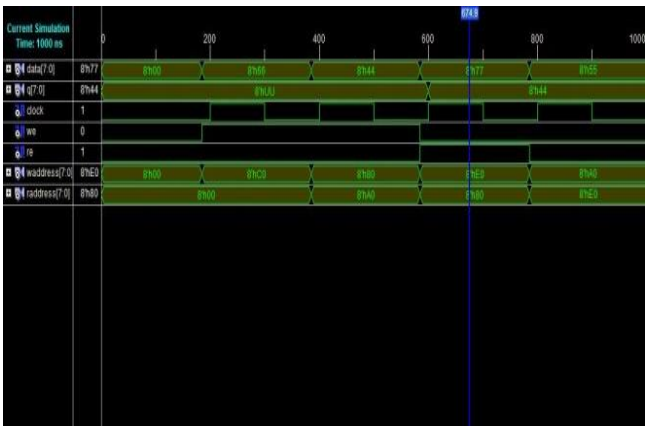

Fig 7- Simulation result of proposed memory

The power analysis is done with Xilinx power estimator (XPE) The static power of proposed design is same as conventional memory but dynamic power is reduced and total power consumption decreases.

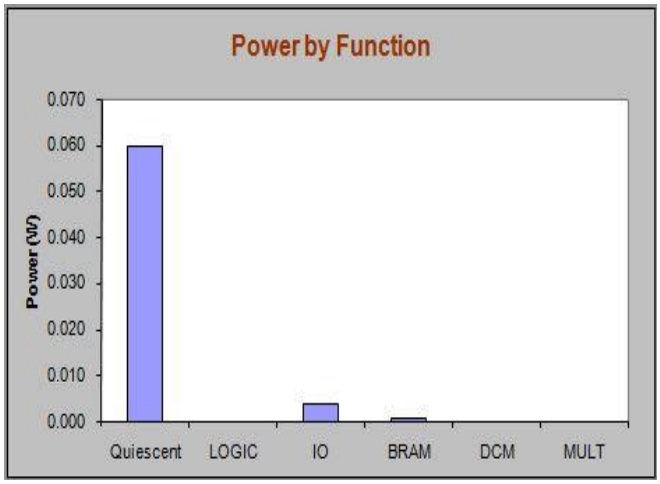

Fig 7- Power analysis of proposed memory

The quiescent power of above describe design is .060 w and dynamic power is 0.008w the total consumption is 0.068w.

Resource Utilization

Number of Slices : 1 out of 3584 0%
Number of Slice Flip Flops: 1 out of 7168 0%
Number of 4 input LUTs : 2 out of 7168 0%
Number of IOs : 35
Number of bonded IOBs : 35 out of 173 20%
Number of BRAMs : 1 out of 16 6%
Number of GCLKs : 1 out of 8 12%

IV. RESULTS

As per the Xilinx Power Estimator(XPE) the total power consume in proposed memory is 0.068w and conventional memory is 0.079.

	Quiescent Power	Dynamic	Total
Memory	0.060w	0.019w	0.079w
Optimized Memory	0.060w	0.008w	0.068w

Table-1 Comparative results

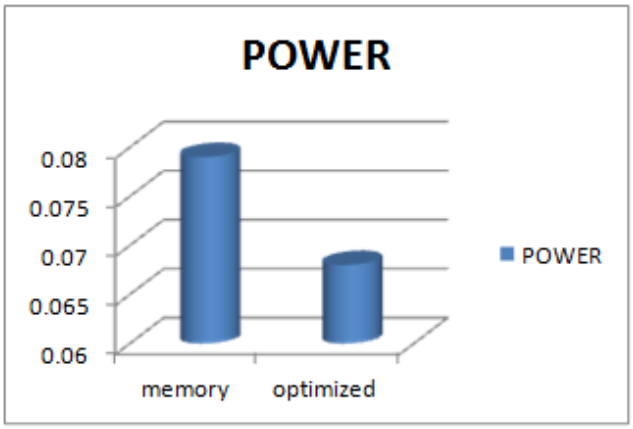

Fig 8- Comparative power graph

This results state that proposed design has better power consumption than conventional.

V. CONCLUSION

Multimedia and communication devices have experienced explosive growth recently. Longer battery life is one of the crucial factors in the widespread accomplishment of these products. As such, low-power circuit design for multimedia and wireless communication applications has become very vital. In order to achieve low power memory, our planned design saves 13.9% of power than a conventional design.

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