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Technical Summary on Non-Volatile ROMs

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***Abstract*—In this paper, several types of Read Only Memory arrays used in VLSI are investigate and discuss in detail their operations and design issues related to area, speed, and power consumption for each type.**

***Index Terms*—MROM, PROM, EPROM, EEPROM, Flash.**

I. INTRODUCTION

The term memory identifies datastorage that comes in the form of electronic device or disks or tapes(Fig.1). The type of application specifies, the required amount of memory in a particular system, in general, the number of transistors for the data storage function is much larger than the number of transistors used for logic operations and other purposes. The ever increasing demand for the larger data storage capacity has driven the fabrication technology and memory development toward more compact design rule and consequently toward higher data storage densities. Thus maximum realizable data storage capacity of single-chip semiconductor memory arrays approximately double, every two years.

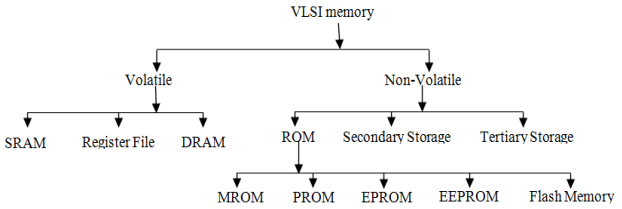

Fig. 1: VLSI Memory tree.

II. READ ONLYMEMORY SPECIFICATIONS

The overall storage capacity depends on the area efficiency of the memory array, i.e., the number of data stored in bits per unit area and consequently the memory cost per bit. Another important design parameter is memory access time, i.e., the time required to store and /or retrieve a particular data bit in/from the memory array, memory speed measures in nanoseconds. Finally, static and dynamic power consumption of the memory array is a significant factor for designerdue to the increasing importance of low-power VLSI applications.

III. READ ONLY MEMORY ARCHITECTURE

Memory Core is consist of memory cells arranged in an array of horizontal 2^N rows for word lines and vertical 2^M columns for bit lines (Fig. 2), each cell can store only one bit of binary information. Thus total number of memory cells in this array is $2^N \times 2^M$. To access a particular data bitfrom the array, the responsible word line and bit line must be selected based on the address coming from the outside of the memory array. As TTL signal on memory board and CMOS signal in the memory chip of the memory array are not same, thusinput address buffers convert the level of address. The row decoder circuit selects one out of 2^N word lines according to an N-bit row address whereas column decoder circuit selects one out of 2^M bit lines according to an M-bit column address. Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) control signals are also provided to activate the read or write operation of the particular memory chip out of the memory.

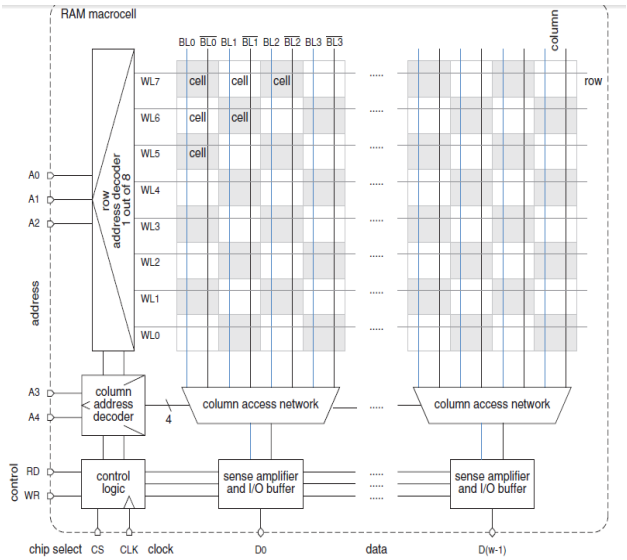

Fig.2: Read Only Memory architecture overview

Computers always contain read-only memory (ROM) that holds instructions for starting up the computer as only retrieval of stored data and is possible in ROM.During normal operation it does not allow any changes of the stored information contents. It is non-volatile; the information is still there once turned off and refresh operation is not required.

Fig.3: ROM

IV. READ ONLY MEMORY TYPES

Depending on the type of data programming ROM can be categorized as:[4]

4. A. Mask ROM

Mask ROM in which data is written during chip fabrication by using a photo mask.MROM can be programmed using any of the following ways[1]

- Metal Programming
- Via Programming

- Diffusion Programming

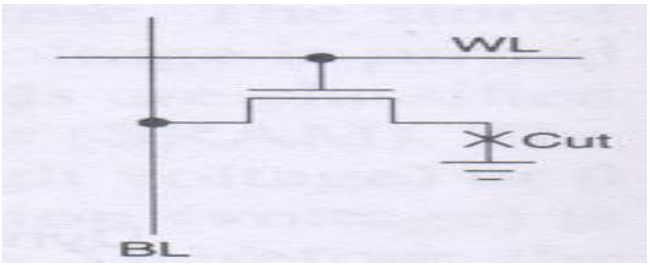

Fig.4: - Mask (Fuse) ROM

4. B. Programmable ROM (PROM)

Data are written electrically after the chip is fabricated. PROM programmer or PROM burner used to write data onto a PROM chip[2].

4. C. Erasable PROM (EPROM)

Data can be erased by exposing it to ultraviolet light (typically for 10 minutes or longer) through the crystal glass on the package (Fig.5).

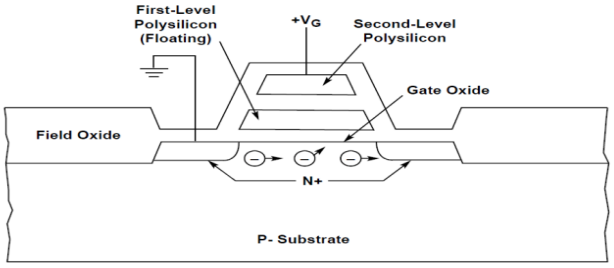

Fig.5: - EPROM

4. D. Electrically Erasable PROM (EEPROM)

It is similar to a PROM, but requires only electrical voltage to erase data (Fig.6). Like other types of PROM, EEPROM retains its contents even when the power is turned off.

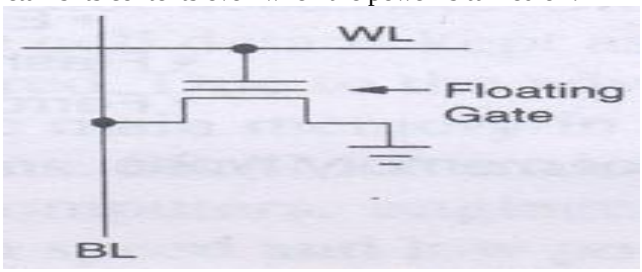

Fig.6: - EEPROM

4. E. Flash Memory

Flash memory technology is a combination of technology used in EPROM and EEPROM. The term flash signifies that a large chunk of memory could be erased at one time unlike EEPROMs, where each byte is erased individually.

4.E. (i). Flash Memory Cell

Flash cell consists of one transistor with a floating gate having thinner gate oxide between the silicon and the floating gate. Source and drain diffusions are different which allow the flash device to be programmed and erased electrically. Fig.14 shows a comparison between a flash memory cell and an EPROM cell from a same manufacturer (AMD) with the same technology complexity[3].

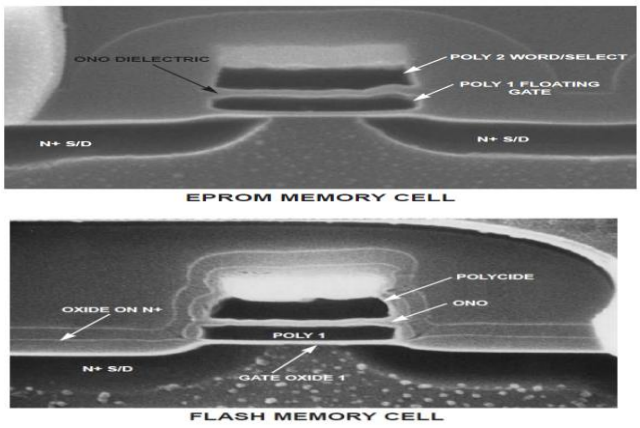

Fig.7: AMD EPROM vs. AMD Flash Memory Cells

Other flash cell concepts are based upon EEPROM technology. Fig. 8 shows a split-gate cell and Fig. 9 shows a transistor with the tunnel oxide in only a part of the oxide under the floating gate.

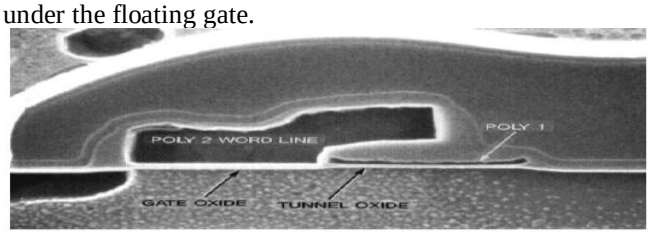

Fig. 8: Split Gate Flash Cell

These cells are far smaller than the conventional two-transistor EEPROM cell and larger than the conventional one-transistor cell.

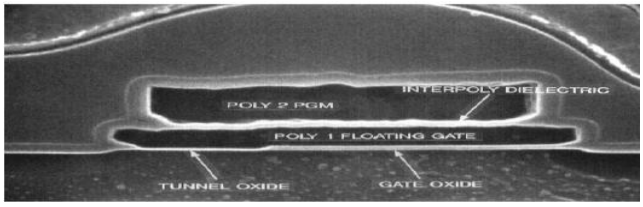

Fig.9: Tunnel Window Flash Cell

Fig.10 summarizes the different modes of flash programming.

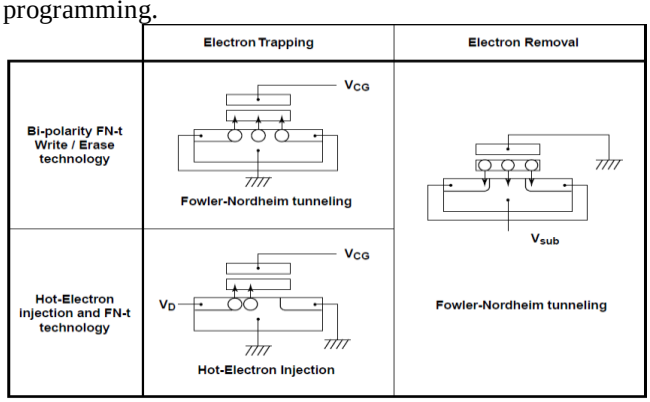

Fig.10: Comparison Between the different types of Flash Programming

4. E. (ii). Flash Architecture

Based on die size and speed, designers have developed multiple flash memory array architectures; NAND, DINOR, and AND are the main architectures developed for flash memories.

NOR Flash: The NOR architecture is commonly used in EPROM and EEPROM designs. The metal to diffusion contacts and active transistors are the largest contributor to area in the cell array. NOR architecture requires one contact per two cells. Hot-electron injection method is used for electron trapping in the floating gate. By Fowler-Nordheim tunneling electrons are removed.

NAND Flash: To reduce cell area, the NAND configuration was developed. Fig.11 shows the layouts of NOR and NAND configurations for the same feature size. As there is no metal to diffusion contact per pair of cells the NAND structure is more compact.

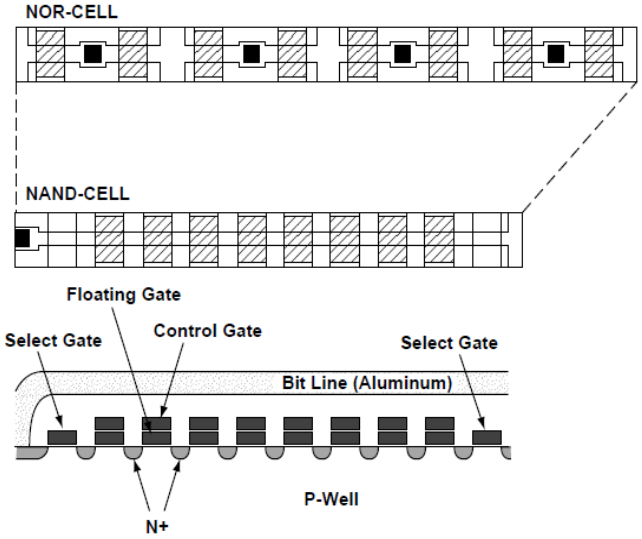

Fig.11: Comparison of NOR and NAND Architectures

A drawback to the NAND configuration is that when a cell is read, the sense amplifier sense a weaker signal than that on a NOR configuration since several transistors are in series. Fig.12 and Table-1 describe the NAND architecture from Toshiba. Table-2 shows a speed differences between NOR and NAND devices.

DINOR Flash :DINOR (divided bit-line NOR) and AND architectures are two other flash architectures that attempt to reduce die area compared to the conventional NOR configuration.

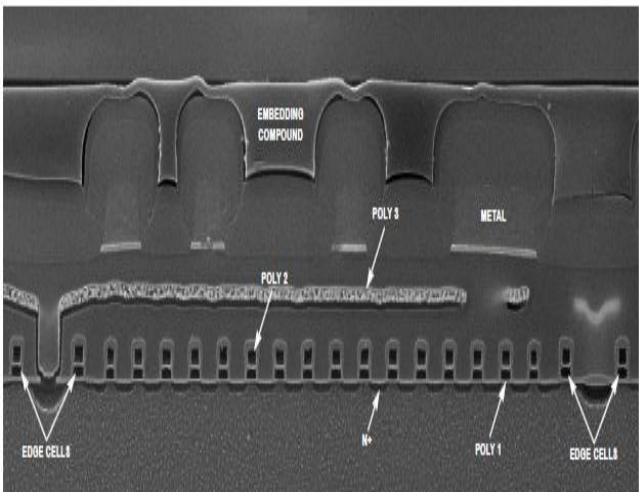

Fig.12: Toshiba Flash NAND Cell

Architecture	NAND
Date Code	9528
Cell Size	1.3µm^2
Die Size	103mm^2
Min Feature Size (Gate)	Cell: 0.25µm Periphery: 0.5µm

Table 1: Toshiba's 32Mbit Flash Characteristics

Architecture	NOR	NAND
Random Access Time	80ns	20µs
Serial Access Time	—	80ns

Table 2: NOR vs. NAND Access times

The DINOR design uses sub-bit lines in polysilicon as 0.5µm CMOS triple well, triple-level polysilicon, tungsten plugs, and two layers of metal having low power dissipation, sector wise erase, and high data transfer rate as fast access timewith 3V operation. Fig.13 shows the DINOR architecture.

AND Flash: Herean embedded diffusion line replaced the metal bit line with the benefit of reduced cell size. The 32Mbit AND-based flash memory device proposed by In random access mode, it is slower than a NOR-based device.

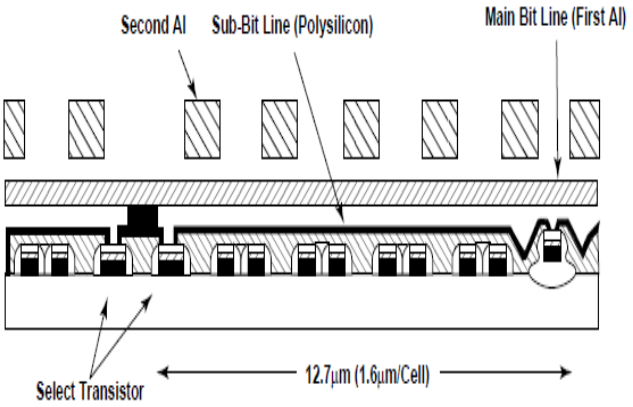

Fig.13: DINOR Architecture

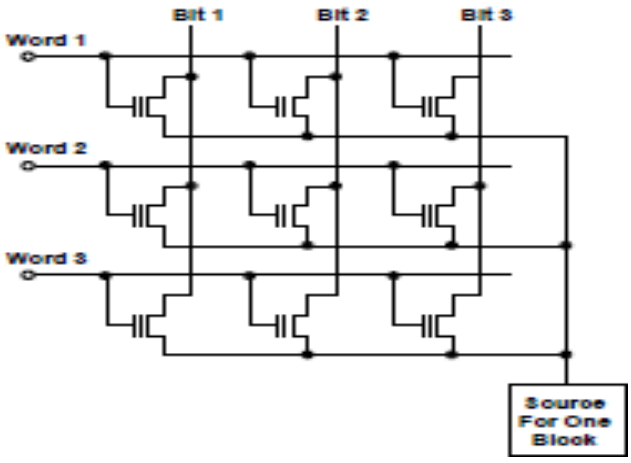

Fig.14a:NOR Architecture

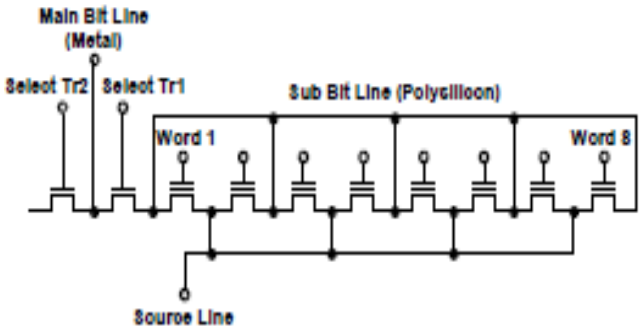

Fig.14b: NAND Architecture

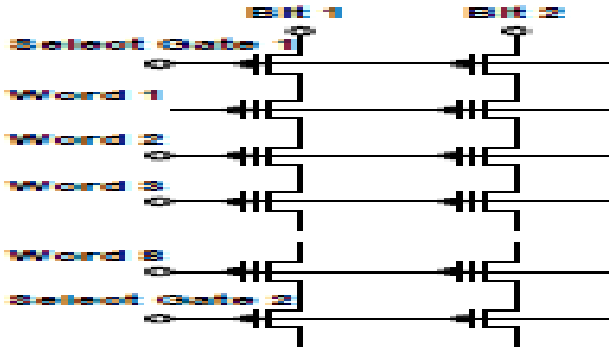

Fig.14c: DINOR Architecture

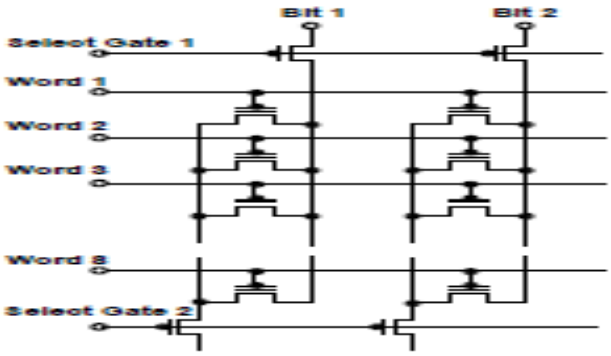

Fig.14d: AND Architecture

Fig.14 presents a review of the different flash architectures.

4. D. (iii). Flash Power Supply Requirements

Flash power supplies range from 5V/12V down to 2V. There are two main reasons for this variation. With different types of flash architectures and designs, different program/erase techniques (Fowler-Nordheim tunneling or hot-electron injection) exist. The source/drain current of hot-electron injection requires an external power supply. Some applications may require low-voltage flash devices while others operate well using flash device with high-voltage characteristics. Manufacturers can propose different types of power supplies that best fit a specific application.Read voltage may be 2.7V, 3.3V or 5.5V and programming voltage may be 3.3V, 5V or 12V.

V. CONCLUSION

The present paper is the literature survey of the most commonly used data storage technologies are semiconductor, magnetic, and optical, while paper still sees some limited usage as of 2011. Media is a common name for what actually holds the data in the storage device.

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