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Power Optimization through Material Variation in CMOS Integrated Circuit

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***Abstract*—This paper provides the simulation of 3 state inverter with different materials and compare the Leakage Current. Material which has the less Leakage Current is considered as better material for the designing of inverter. In previous time the mosfet is design by the combination of silicon and silicon oxide now we are using gallium arsenide and silicon dioxide as one combination and gallium arsenide and silicon nitride as another combination and different combinations of materials having high –K dielectric and semiconductor.**

***Index Terms*—Gallium arsenide, high-k., power consumption,silicon nitride.**

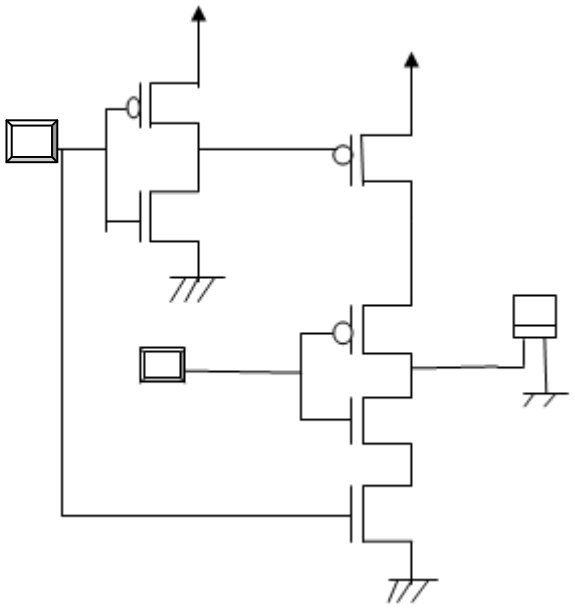
I. INTRODUCTION

The CMOS inverter design is consist of one p-channel MOS and one n-channel MOS transistors are used as switches. All the symbols produced the value logic '0' and logic '1'. However, if several inverters share the same node, such as bus structure conflicts will rise. In order to avoid multiple access at the same time, specific circuits called 3-state inverters are used, featuring the possibility to remain in a 'high impedance' state when access is not required The 3-state inverter symbol consists of the logic inverter and an enable control circuit. The output remains in 'high impedance' (Logic symbol 'X') as long as the enable *En* is set to level '0'.

The truth table is reported below.

In	En	Out
0	0	×
0	1	1
1	0	×
1	1	0
×	0 or 1	×
0 or 1	×	×

The basic CMOS inverter is no more connected to the supply lines VDD and VSS directly.
In contrary, pass nMOS and pMOS devices are inserted to disconnect the inverter when the cell is disabled .we see that when *Enable*=1 the cell acts as a regular CMOS inverter, while when *Enable*=0 the output "floats" in an unpredictable voltage value, which tends to fluctuate at the switching of the input, mainly due to parasitic leakage and couplings.



II. PROPERTIES OF MATERIAL

2.1Gallium Arsenide

1. It has direct band gap, which means that it can be used to emit light efficiently.

2. Higher carrier mobilities and lower resistive device parasitic.

3. GaAs is an excellent material for space electronics and optical windows in high power application.

2.2 Silicon nitride

1. Silicon nitride is an important material in microelectronics due to its high resistivity, higher dielectric constant compared to silicon dioxide, mechanical strength and chemical inertness.

2.It is used as a gate insulator in thin film transistor that are in flat panel display.

2.3 Silicon

1. Silicon is the existence of a native oxide (silicon dioxide), which is used as an insulator in electronics devices.

2. It has much higher hole mobility. This high mobility allows the fabrication of higher speed p-channel field effect transistor, which are required for CMOS logic

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III. RESULT

DIELECTRIC CONSTANT	OXIDE	SEMICONDUCTOR1	SEMICONDUCTOR 2	CURRENT 1	CURRENT 2
K=3.9	SiO_2	GaAs	Ge	0.422mA	0.049 mA
K=7.5	Si_3N_4	GaAs	Ge	0.422mA	0.049 mA
K=9	Al_2O_3	GaAs	Ge	0.418mA	0.049 mA
K=22	Ta_2O_5	GaAs	Ge	0.419mA	0.049 mA
K=25	HfO_2	GaAs	Ge	0.418mA	0.049 mA
K=30	$LaAlO_3$	GaAs	Ge	0.414mA	0.049 mA

OUTPUT RESULT :-

GALLIUM ARSENIDE = 0.414

GERMANIUM = 0.049

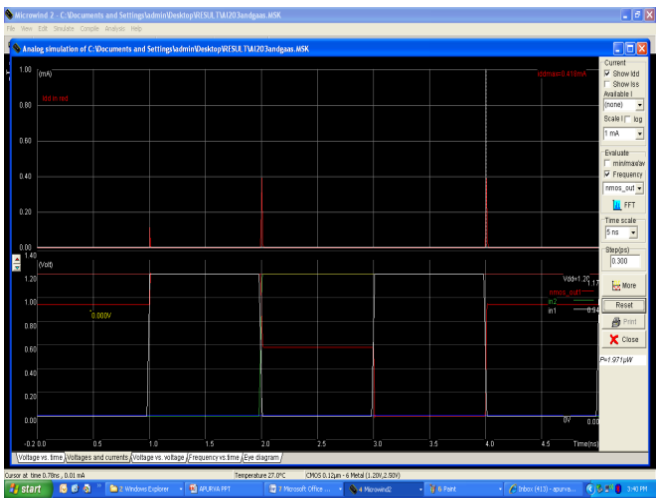
ERROR 0.365

$$\text{OUTPUT IN PERCENTAGE} = \frac{0.365}{0.049} \times 100$$

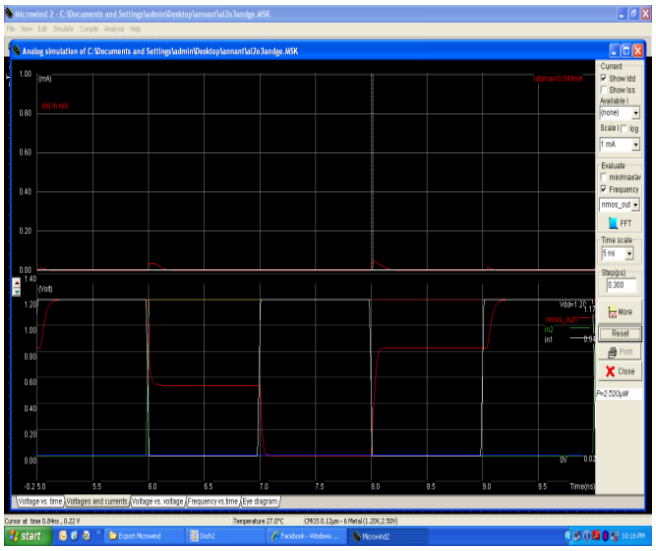
$$= 88\ \%$$

IV. SIMULATION

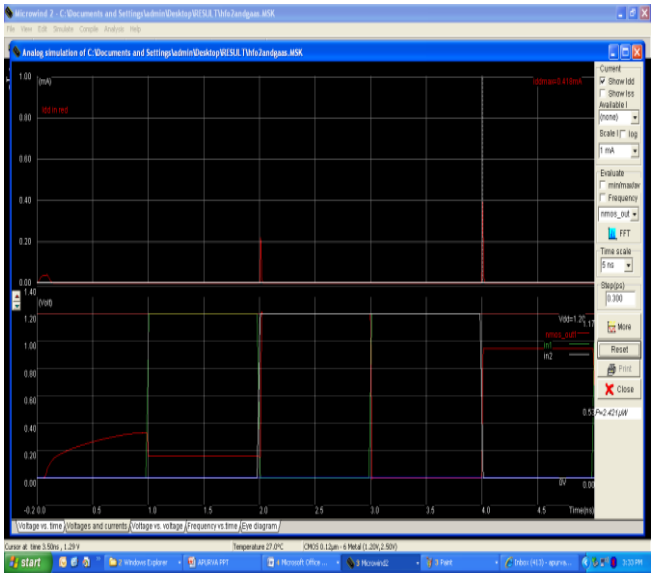
3.1 *GaAs and Al_2O_3*



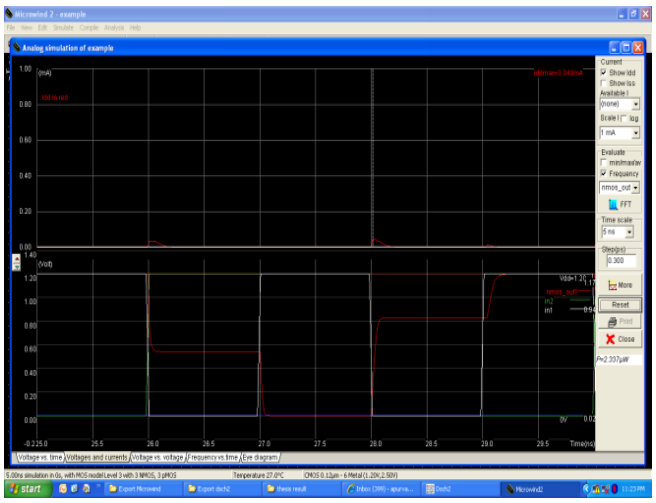
3.2 *Ge and Al_2O_3*



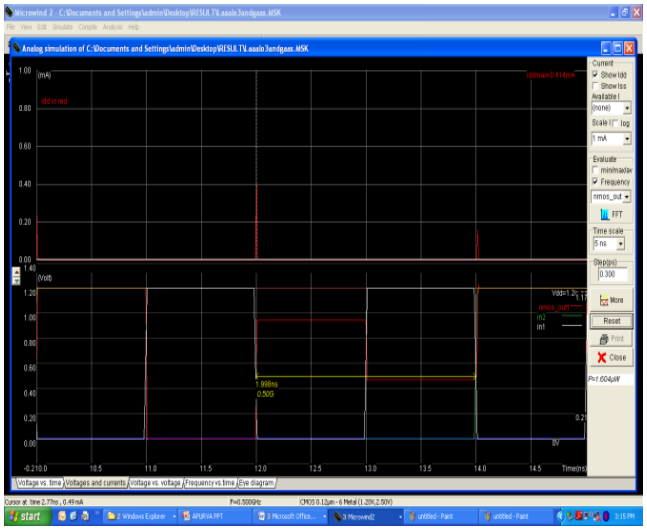
3.3 *GaAs and HfO_2*



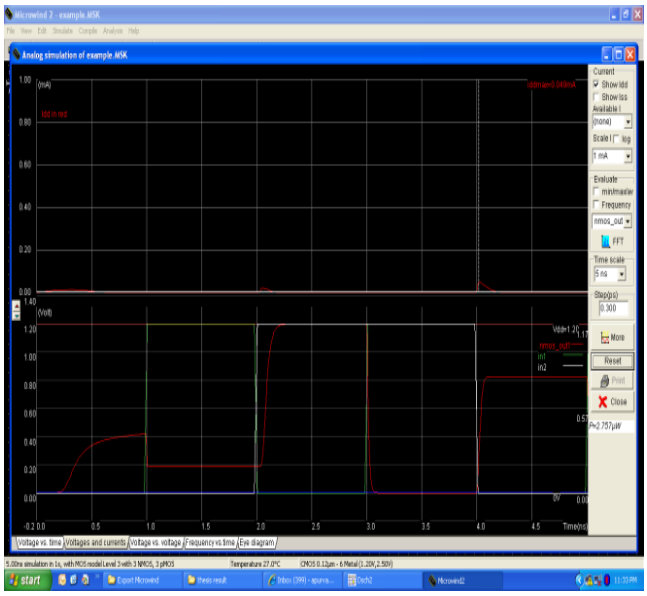
3.4 *Ge and HfO_2*



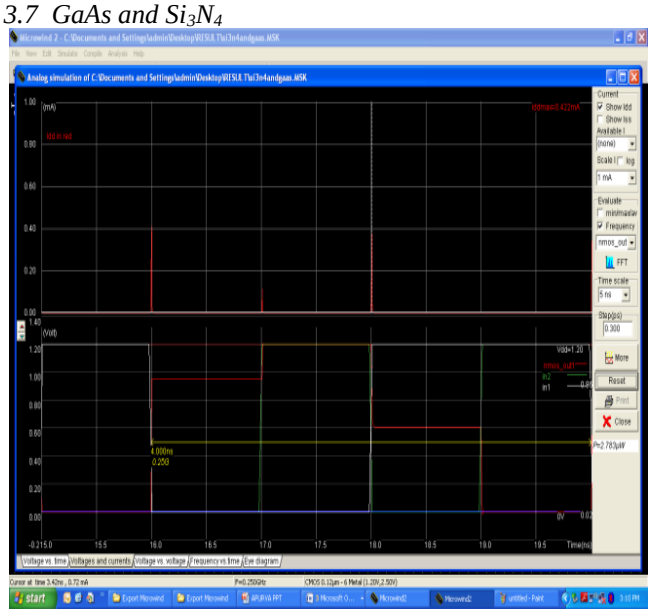
3.5 GaAs and $LaAlO_3$



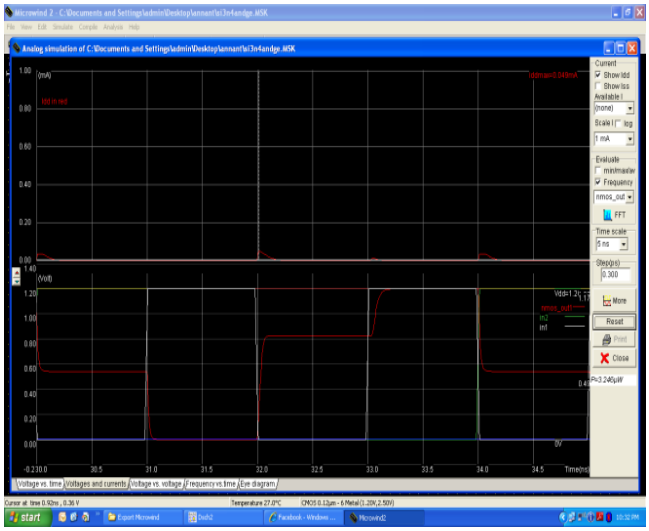
3.6 Ge and $LaAlO_3$



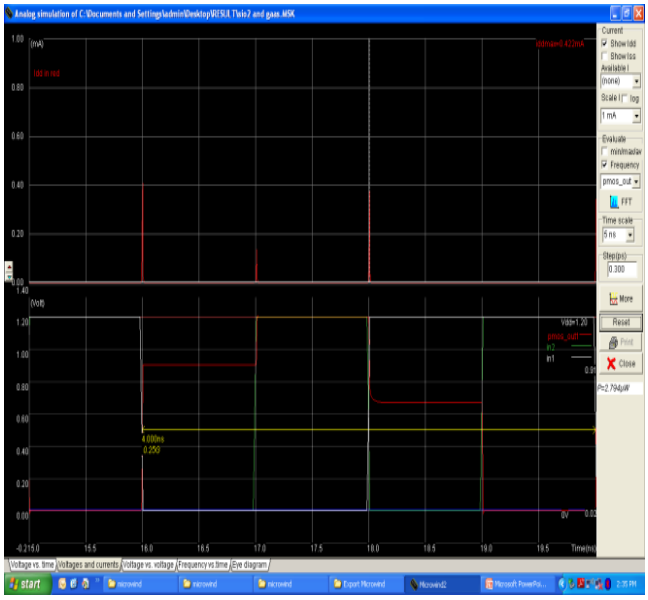
3.7 GaAs and Si_3N_4



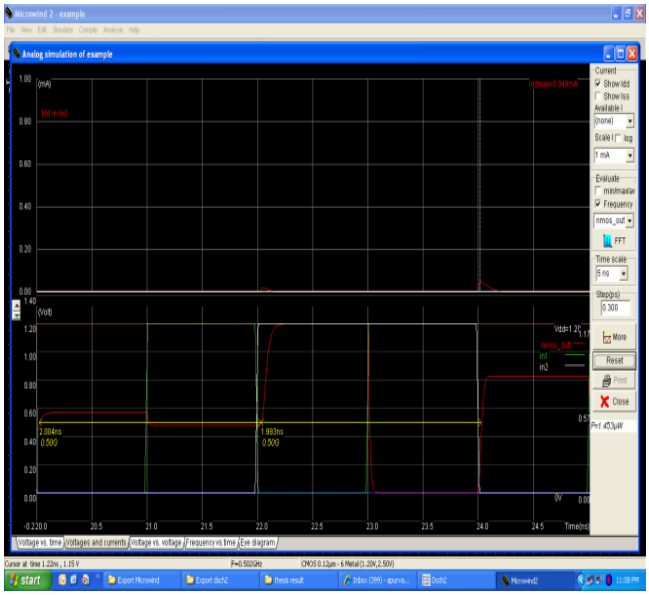
3.8 Ge and Si_3N_4



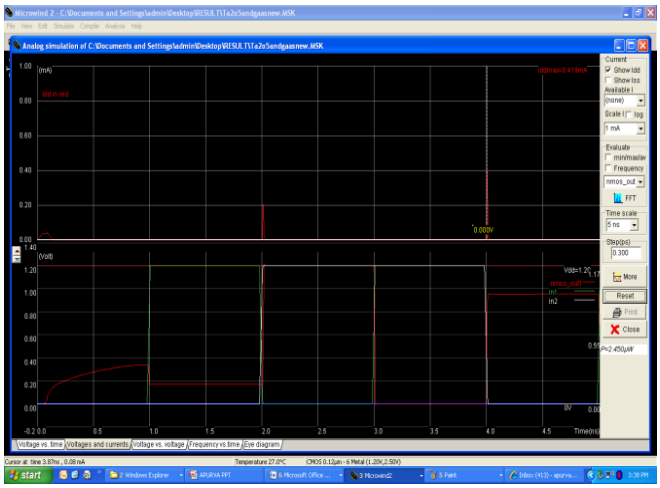
3.9 GaAs and SiO_2



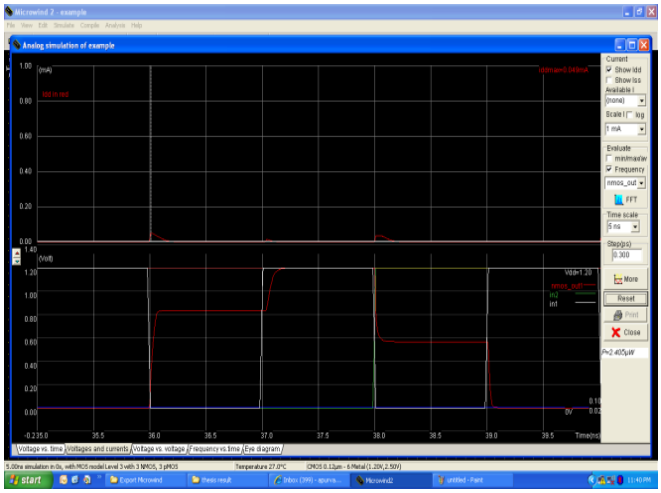
3.10 Ge and SiO



3.11 GaAs and Ta_2O_5



3.12 Ge and Ta_2O_5



V. CONCLUTION

CMOS technology has seen an excellent high speed performance achieved through improved design, use of high quality materials and processing innovations over the past decade. Silicon dioxide gate dielectric is replaced with various high-k dielectric materials. The choice of the high-k dielectric and the knowledge of its physical properties helps in changing the various characteristics of the oxide layer in respect to power, current and the layout area covered. It is observed that the leakage of the device decreases by about 88% .The study of the properties of these material was used in modeling the tri-state inverter and its various parameters were tabulated. The modeled inverter with high-k dielectric as gate dielectric material can be used for high gain and for low power applications in various electronic fields. Lanthanum is considered as better dielectric material.

REFERENCES

[1] D Nirmal,P Vijay Kumar,"Nanoscale Tri Gate MOSFET for Ultra Low power applications Using High-K Dielectrics" Nanoelectronics Conference (INEC),2013 IEEE 5th International.

[2] D Nirmal,P Vijay Kumar,"Nanoscale Channel Engineered Double Gate MOSFET for Mixed Region "International Journal of Circuit Theory and Application, 10 Mar 2012

[3] J.Conde,A. Cerdeira et al," 3D Simulation of Triple Gate MOSFET with Different Mobility Region" Microelectronics engineering Vol 88, Issue 7,pp.1633-163,July 2011

[4] KUMAR, M.P GUPTA ,S.K PAUL,"CORNER EFFECTS IN SOI TRI GATE FINFET STRUCTURE BY USING 3D PROCESS AND DEVICE SIMULATION"COMPUTER SCIENCE AND INFORMATION TECHNOLOGY (ICCSIT),

[5] X. Zhou, "Exploring the novel characteristics of hetero-material gate field-effect transistors (HMGFETs) with gate-material engineering," IEEE Trans. Electron Devices, vol. 47, 2000.

[6] V. Kilchytska, A. Nève, L. Vancaillie, D. Levacq, S. Adriaensen, H. van Meer, K. De Meyer, C. Raynaud, M. Dehan, J.-P. Raskin, and D. Flandre, "Influence of device engineering on the analog and RF performance of SOI MOSFETs," IEEE Trans. Electron Devices, vol. 50, 2003.

[7] J. P. Colinge, "Multiple-gate SOI MOSFETs," Solid State Electron., vol. 48, 2004.

[8] C.R.Manoj and V.Ramgopal Rao,"Impact of High k dielectrics on the device and circuit performance of nanoscale FinFETs," IEEE Electron Device Lett, vol. 28, 2007.

[9] W. Long, H. Ou, J. Kuo, and K. K. Chin, "Dual-material gate (DMG) field effect transistors," IEEE Trans. Electron Devices, vol. 46, 1999.

[10] Integrated Systems Engineering (ISE) TCAD Manuals, Integr.Syst. Eng., Zurich, Switzerland, 2006. Release 10.0. International Technology Roadmaps for Semiconductor (ITRS). 2008 edition.

[11] N.Mohankumar, Binit Syamal, and Chandan Kumar Sarkar, "Influence of Channel and Gate Engineering on the Analog and RF Performance of DG MOSFETs," IEEE Transactions On Electron Devices, Vol. 57, 2010

[12] A. P. Huang1,2, Z. C. Yang1 and Paul K. Chu2, "Hafnium-based High-k Gate Dielectrics, " Advances in Solid State Circuits Technology.

[13] J. Yuan and J. C. S.Woo, "A novel split-gate MOSFET design realized by a fully silicided gate process for the improvement of transconductance and output resistance," IEEE Electron Device Lett., vol. 26, 2005.

[14] Nirmal, Vijaya Kumar, Sam Jabaraj," Nand Gate Using Finfet For Nanoscale Technology", International Journal of Engineering Science and Technology, Vol. 2(5), 2010.