Design and Implementation of Signal Information Descriptor Word

Biyappu Chinmayi Roopa, N.V.K. Ramesh, Challa Yasaswini, Dr. A. Sreenivas, Mr. S.R. Pankaj Kumar

***Abstract*— EM waves are propagated in any medium such as air, water, etc. When a EM wave hits the target (RADAR), different pulses are obtained from 360 deg, where it selects a specific phase for about 90 deg, so single pulse is selected based on the maximum amplitude. The information is in the form of RF pulse which specifies frequency, amplitude and phase. From the RF pulse, parameters like pulse width, time of arrival and direction finding are measured. Further all these parameters are packed into a 192 bit Signal Information Descriptor word (SIDW) format. This 192 bit is designed and developed in VHDL language and implemented in Xilinx ISE Design Suite.**

***Index Terms*— EM wave, RADAR, RF pulse, 192 bit Pulse Parameter Word format**

I. INTRODUCTION

Electronic Warfare (EW) system is used to protect military resources from enemy threats. It is defined as a military action involving the use of electromagnetic energy to determine, exploit, reduce or prevent hostile use of the EM spectrum and action which retains friendly use of the EM spectrum. EW can be applied from air, sea, land, and space by manned and unmanned systems, and can target humans, communications, radar, or other assets. It includes three major subdivisions: electronic attack (EA), electronic protection (EP), and electronic support (ES).

Electronic attack involves the use of EM energy, directed energy, or anti-radiation weapons to attack personnel, facilities, or equipment with the intent of degrading, neutralizing, or destroying enemy combat capability.

Electronic protection involves actions taken to protect personnel, facilities, and equipment from any effects of friendly or enemy use of the electromagnetic spectrum that degrade, neutralize, or destroy friendly combat capability.

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Biyappu Chinmayi Roopa, Embedded Systems, M. Tech., ECM dept., KL University, Guntur, Andhra Pradesh, India.

N.V.K. Ramesh, M. E., Associate Professor, ECM dept., KL University, Guntur, Andhra Pradesh, India.

Challa Yasaswini, Digital Systems & Signal Processing, M. Tech, ECE dept., GITAM University, Visakhapatnam, Andhra Pradesh, India.

Dr. A. Sreenivas, M. E., Ph.D., Associate Professor, ECE dept., GITAM University, Visakhapatnam, Andhra Pradesh, India.

Mr. S.R. Pankaj Kumar, Sc – 'F', Defence Electronics Research Laboratory (DLRL), Ministry of Defence, Govt. of India, Chandrayangutta lines, Hyderabad, India.

Electronic support is the subdivision of EW involving actions tasked by, or under direct control of, an operational commander to search for, intercept, identify, and locate or localize sources of intentional and unintentional radiated EM energy for the purpose of immediate threat recognition, targeting, planning, and conduct of future operations.

When number of EM waves of the Radar intercepts with homodyne receivers of the Electronic support (ES) system, the information here is carried out in the form of signal. The homodyne receiver is segregated into two bands i.e. low band and high band. A dedicated board is associated with each band of homodyne receiver. Each band consists of four independent homodyne receivers and is referred to as Q1, Q2, Q3 and Q4. On incidence of an external RF signal, each quadrant in itself being a fully fledged receiver, measures Frequency, Phase, and Amplitude and also generates a pulse i.e. signal presence (SP). The quadrant that has maximum amplitude is selected and the SP pulse output from the selected quadrant is used for measurement of pulse parameters as pulse width and time-of-arrival and direction of arrival. Various Timing signal are generated from both the leading edge and trailing edge of the SP which is used for pulse parameter measurements at different instances of time. After all the parameter measurements are done for a signal, a 192 bit of data is generated. These 192 bits are segregated into 6 words of 32 bits each and packed into a format called as signal information descriptive word. These 6 words of data are sent in parallel using 5 synchronizing signals.

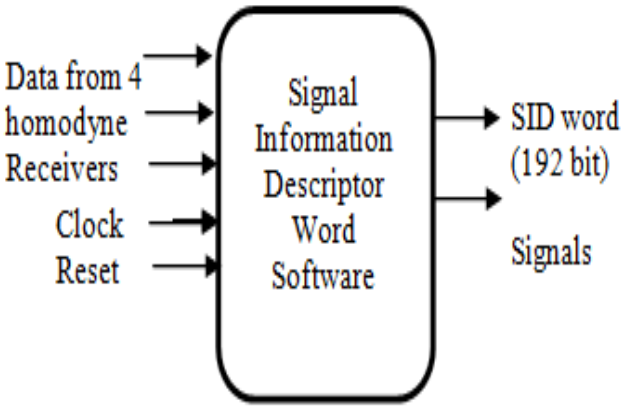


Fig. I/O details of SID Generation Software

II. DESIGN

The above functions are realized through following modules:

Quadrant Selection Module

Timing Generation Module
Pulse Width Measurement Module
Intra Pulse Analysis Module
Time of Arrival Module
Inhibit Module
Direction of Arrival Module
Pulse Parameter Formatter Module

A. *Quadrant Selection Module*

The SP's from each quadrant is deglitched by using D Flip Flop and then ANDing the delayed SP signal with incoming SP. The amplitude data from all the quadrants are latched using the amplitude strobes generated at regular intervals of time from the leading edge of SP, similarly frequencies, phase and sine from all the quadrants are also latched. The amplitudes of all quadrants which are latched are compared and Quadrant which has got maximum amplitude is selected.

B. *Timing Generation Module*

In timing generator, strobes are generated for other modules in a organized sequence ensuring the smooth and sequential running of the top module. SP is the reference signal to generate the following strobes namely toa_stb, pw_stb, busy_stb, sid_clk along with transmission controls signals and its delay set. From the leading edge of SP, toa_stb and busy_stb are generated. toa_stb strobe is used to measure the Time of Arrival of a signal which is generated from quadrant selection module. Busy_stb strobe is generated in order to keep the controls inactive until all the strobes are generated. From the trailing edge of SP, pw_stb and sid_clk, eopr are generated. Pw_stb strobe is used to measure the Pulse Width of a signal which is generated from quadrant selection module. sid_clk strobe is used as reference clock for SID word formatter in order to send the SID words sequentially. Eopr strobe is generated whenever the busy_stb is inactive which specifies end of operation. From the trailing edge of eopr, the controls are generated namely prns, wa2, wa1, wa0, wclk, eotr and its delay set.
For the controls to be generated, a clock of 133 MHz i.e. clk_133 is used. The control signal prns is nothing but presence which means complete 192 bit SID word is present. The control signals wa2, wa1, wa0 signifies word address which will be used further in remaining modules based on which particular word to be sent out. The control signal wclk signifies word clock, 6 wclk clocks will be generated. For every wclk, single SID word will be sent out. When wa2, wa1, wa0 are all 0's, first wclk clock will be generated and first word will be sent out. Similarly the remaining word address follow till 101, all six wclk clocks will be generated and sends the last word out. All the words are sent out, eotr control signal will be generated which specifies end of transmission of 192 bit SID word. Delay set of control signals are used in order to match the hardware timings, one clock cycle delay will be occurred and the controls are dprns, dwa2, dwa1, dwa0, dwclk. Fig represents the input and outputs of timing generation module. The inputs to this module are: reset, SP, clk_50, clk_133. The outputs of this module are: toa_stb, busy_stb, pw_stb, sid_clk, eopr, prns, wa2, wa1, wa0, wclk, eotr, dprns, dwa2, dwa1, dwa0, dwclk.

C. *Pulse Width Measurement Module*

In this module we can calculate the pulse width of the input SP pulse by using counter. The count value is latched to the output only when pulse width strobe PW_STB is occurred in timing generation module. This value is then sent for the validation. The inputs to this module are: RESET, CLK_50 and PW_STB and the outputs are: PW (13 bit) and PW_valid flag. .The pulse width output is one of the pulse parameter values in SID word format which is also used for further processing too. The inputs to this module are: ORed SP, CLOCK, PW_STB, FREQ and AMP.

D. *Intra Pulse Analysis Module*

The function of this module is to analyse the various signal conditions like CHIRP, POP and CW which are present in the transmission.
CHIRP: Generation of chirp, up chirp and down chirp flags by taking frequency samples and subtracting them and comparing the subtracted value with equivalent code of particular frequency.
POP: Generation of POP by taking amplitude samples and subtracting them and comparing the subtracted value with equivalent code of amplitude.
CW: Generation of CW flag and if the CW flag is set we generate synthetic SP pulse until the SP is high.

E. *Time of Arrival Module*

To compute PRI of the intercepted emitters it is necessary to know the TOA of each pulse accurately. For every pulse that is received time data is generated which signifies the arrival time of each pulse. This Data is generated using 36 bit synchronous counter operating at a frequency. The output of this counter is latched in a 36-bit register using TOA_STB at the leading edge of the SP.

F. *Inhibit Module*

The inputs to this module are POP, POCW, DF_VALID, and PW_VALID. All the inputs are ORed to give the output inhibit signal. When anyone of the signal is '1' then the output is set to '1' and the SID word generation is stopped.

G. *Direction of Arrival Module*

In this module, DOA input is taken from the flash memory. This input along with the sector bits generated to validate the calculated DOA. The inputs to this module are sector bit, DF, CLK. The output of this module is DOA_VALID. Using generated sector bits, we know the range in which DF lies. The input DOA is then checked whether it lies in the expected range or not. If it lies in the range then DOA_VALID is set to '1' else it is set to '0'. This DOA_VALID signal is used to set inhibit signal in another module which inhibits the generation of SID Word.

H. *Signal Information Descriptor Word Formatter Module*

In this module, data that is calculated till now into a register and then pass onto the other sub-system with WCLK . The data is taken from the inputs, when SID_CLK comes. The inputs to this module are frequency, pulse width, doa, amp, time of arrival, inh, bite, le_freq, te_freq, SID_CLK, chirp, pop, cw, pocw, pd_val, eotr, wa0, wa1, wclk, prns. The output of this module is a SID word which is a 32 bit word. All the input data are already calculated by different modules , when SID_CLK input is set to '1' , then these values are stored into the register . When the SID_CLK is set to '1' it checks if the INH signal is '1' or not , if it is '1' then the data is not copied into the register . If the INH is '0' then the data is latched into the register. When the PRNS pulse is set then data in the register is sent out according to the signals wa0 and wa1 .Parity bit for the word that is sent out is calculated by XORing all the bits of the word and appended to the word and sent to the output. When PRNS signal becomes '0' and EOTR signal is set to '1' then the transmission of the data is stopped.

III. IMPLEMENTATION

Xilinx ISE (Integrated Software Environment) is a software tool produced by Xilinx Inc for Synthesis and analysis of HDL designs, enabling the developer to synthesize their design, performs timing analysis examine RTL schematics, simulates designs reaction to different stimuli and configure the target device with a programmer. It is a proprietary software. It current stable release is 14.7.

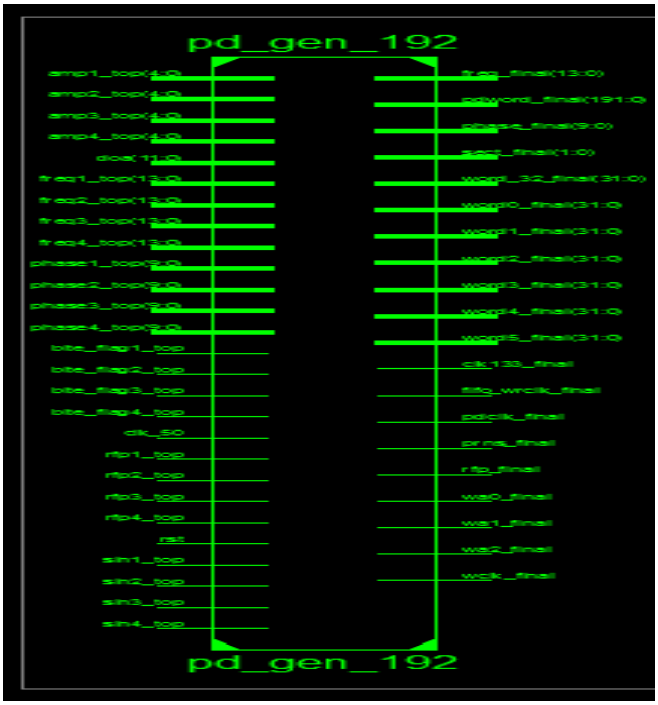
Compatibility: Although Xilinx of only officially supports Red hat enterprise 4,5,6 and SUSE Linux enterprise and many other GNU/Linux distribution can run Xilinx ISE web pack with some modifications or configurations. It also supports Microsoft Windows professional and Windows 7. The platform for it is either 32 or 64 bit.

ISE Design Suite: ISE web pack delivers a complete front to back design flow providing instant access to the ISE features and functionally at no cost.

Synthesis, simulation and implementation of the code are done using Xilinx ISim (ISim is an abbreviation for ISE Simulator, an integrated HDL simulator used to simulate Xilinx FPGA and CPLD designs).

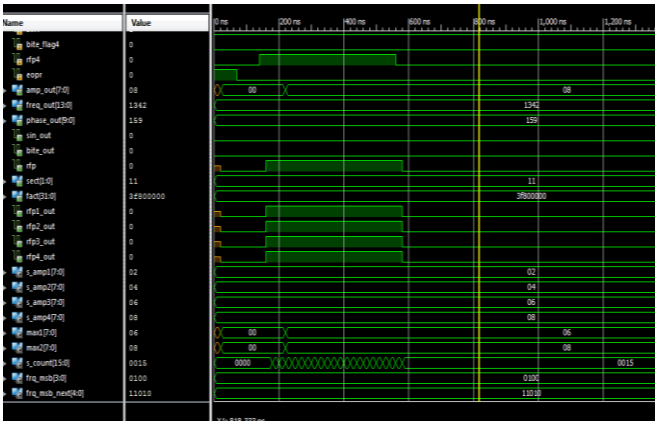
Synthesis is a process in which it checks the syntax and shows the errors if present, if errors are present RTL schematic and technology schematic cannot be generated, if no errors are there schematic will be generated. The second step is implementation in which the code written is translated, mapped, placed and routed according to the FPGA selected. The **Translate** process merges all of the input netlists and design constraints and outputs a Xilinx Native Generic Database (NGD) file, which describes the logical design reduced to Xilinx primitives. The **Map** process maps the logic defined by an NGD file into FPGA elements, such as CLBs and IOBs. The output design is a Native Circuit Description (NCD) file that physically represents the design mapped to the components in the Xilinx FPGA. The **Place and Route** process takes a mapped NCD file, places and routes the design, and produces an NCD file that is used as input for bit stream generation.

The simulation results are obtained after synthesize the VHDL code and then implementation is done i.e., translate, mapping, place and routing, Bit file generation and dumping the code into the FPGA using JTAG CABLE. The SID Generation Module is designed in such a way that it generates 192 bits width. The SID Generation is designed by using combinational logic, VHDL code is written to generate the required output.

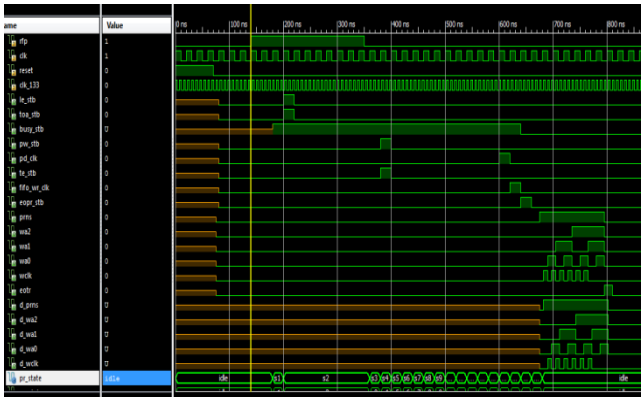


IV. RESULTS

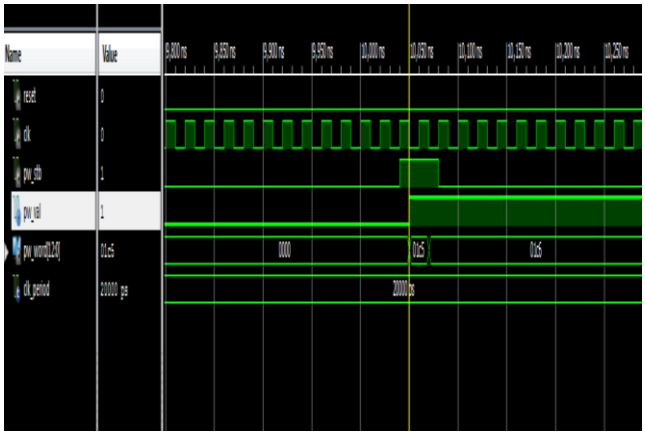
A. *Quadrant Selection Module*



B. Timing Generation Module

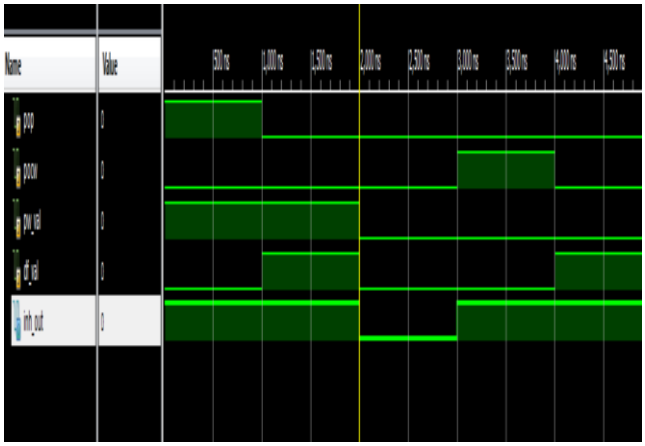


C. Pulse Width Measurement Module

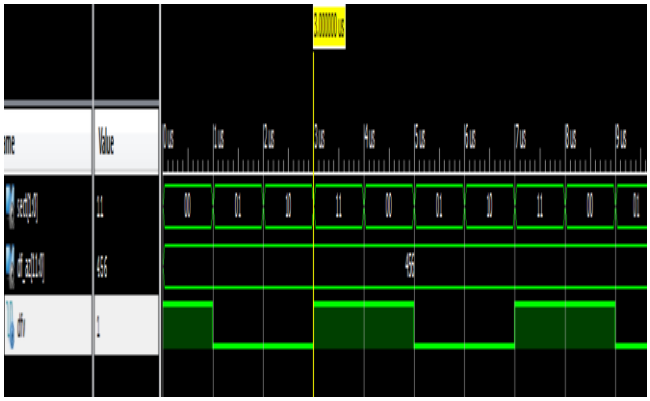


D. Time of Arrival Module

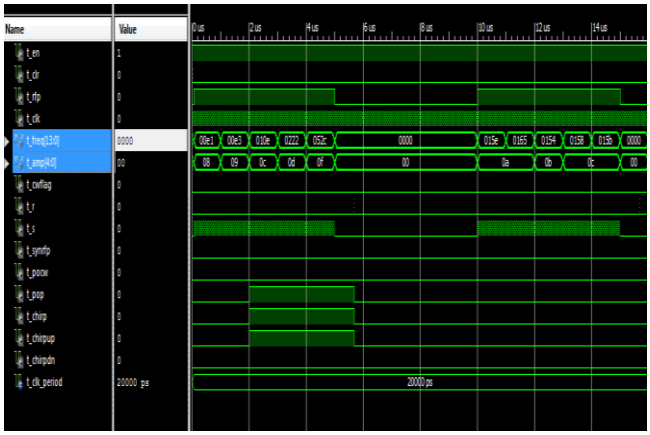
E. Inhibit Module



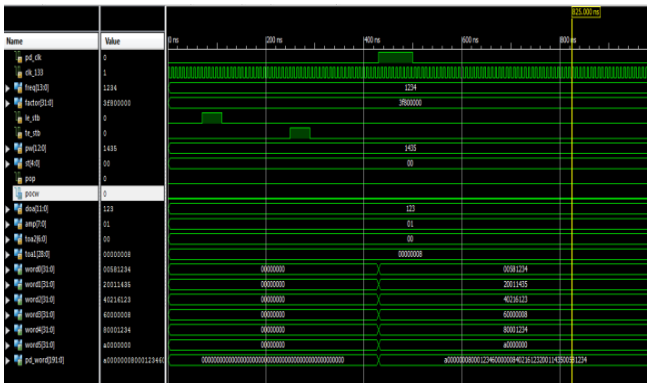
F. Direction of Arrival Module



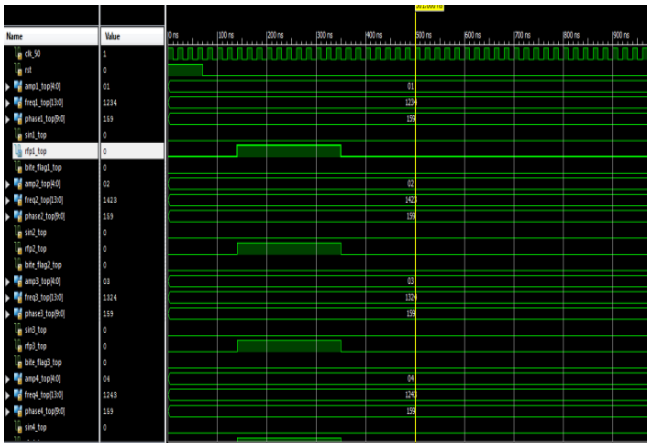
G. Intra Pulse Analysis Module

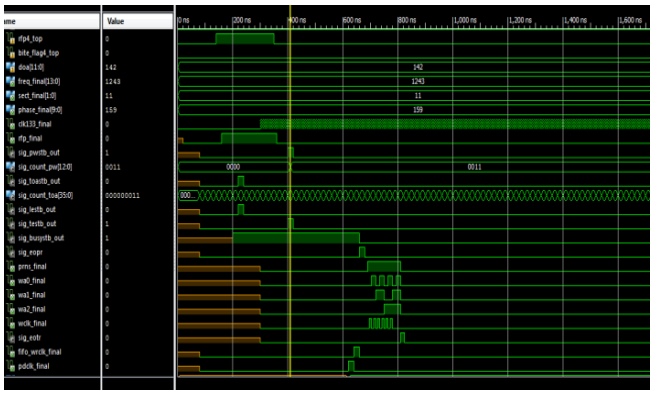


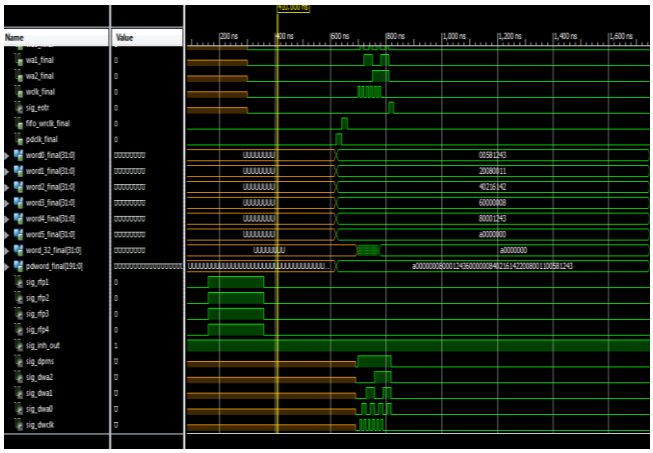
H. Signal Information Descriptor Word Formatter Module



I. SIDW Generation Module







V. CONCLUSION

The analysis of pulse based on different parameters is done and is also simulated in the ISim and the 128 bit is divided into six 32bits.

ACKNOWLEDGMENT

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