Analysis of SRAM bitcells using Ultralow-Voltage Schmitt-Trigger based Design

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***Abstract*— Schmitt-Trigger (ST) based differential sensing static random access memory (SRAM) bitcells for ultralow voltage operation is analyzed. The fundamental conflicting design requirement of the read versus write operation of a conventional 6T bit cell is addressed by ST-based differential sensing SRAM bitcells. The ST operation gives better read-stability as well as better read-failure probability compared to the standard 6T bitcell. The proposed ST based bitcells incorporate a built-in feedback mechanism. Balancing the trade-offs between small areas, low powers, fast reads/writes are an essential part of SRAM design. That is, SRAM design requires to balancing among the various design criteria such as minimizing cell area using smaller transistor, maintaining read/write stability, minimizing power consumption by reducing power supply, minimizing read/write access time, minimizing leakage current, reducing bit-line swing to reduce power consumption. A detailed comparison of 6T bitcell shows that the ST based bitcell can operate at lower supply voltages. Measurement results carried out in 180-nm CMOS technology and various SRAM metrics has been compared.**

***Index Terms*— Schmitt-Trigger, Static RAM, Read-stability, Read-failure, Power consumption.**

I. Introduction

The power requirement for battery operated devices such as cell phones and medical devices is even more stringent with the scaling of the device dimensions. Reducing the supply voltage reduces the dynamic power quadratic ally and leakage power linearly. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor. However, the reduction in supply voltage may lead to increased memory failures such as read-failure, hold failure and write-failure. For a stable SRAM bitcell operating at lower supply voltages, the inverter pair stability should be improved. The proposed Schmitt trigger based differential bitcell having built-in feedback mechanism for improve the stability of the inverter pair under low voltage operation.

Lowering the supply voltage is an effective way to achieve ultra-low-power operation. Here we evaluated ST-based SRAM bitcells suitable for ultra-low-voltage applications. The built-in feedback mechanism in the ST bitcell can be effective for nanoscaled technologies. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bitcell. For successful SRAM operation the cross-coupled inverter stability is important to achieve better Read & Write Stability. The main objective is to achieve Low power, Low voltage, and Lower Leakage Current design SRAM design and provide the better Read Stability & Write Stability.

To maximize the battery lifetime, each electronic devices consume very low power. Various techniques have been implemented to minimize the power consumption [1]. The significant impact on the overall power dissipation is Supply voltage scaling. In the supply voltage reduction, the dynamic power quadratically reduced while the leakage power reduces linearly [1]. Due to the supply voltage is reduction, the sensitivity of circuit parameters and process variations increases. This variation limits the circuit operation particularly for SRAM bitcells employing minimum-sized transistors [2], [3]. These minimum geometry transistors are vulnerable to inter-die as well as intra-die process variations. Intra-die process variations include line edge roughness (LER) and random dopant fluctuation (RDF). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4]. The effects of the lower supply voltage along with the increased process variations may lead to increased memory failures such as hold-failure read and write failure, and access-time failure [4]. Moreover, occupy a significant portion of the total die area, it is predicted that embedded cache memories, which are expected to failures with scaling [2].

In a given process technology, the maximum supply voltage (referred to as Vmax) for the transistor operation is determined by the process constraints such as gate-oxide reliability limits Vmax is reducing with the technology scaling due to gate-oxide thickness scaling. The get the minimum supply voltage for SRAM bitcells, for a given performance requirement (referred to as Vmin), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltage. In the technology scaling Vmin is increasing, and the gap between Vmax and Vmin is very close together [5]. For a wide voltage range to enable SRAM bitcell operation, Vmin has to be further lowered. Various design solutions such as read and write assist techniques and bitcell configuration techniques have been explored. Read and write assist techniques control the magnitude and the duration of different node biases (such as bit-line, word-line, bitcell VSS and VCC). In this case, SRAM Vmin can be lowered without adding extra transistors to the six–transistor (6T) bitcell. To enable low-voltage operation, various bitcell topologies are also proposed. In this work, focus only on various bitcell configurations and believe that read and write assist circuits can be applied to these bitcell configurations for further Vmin reduction.

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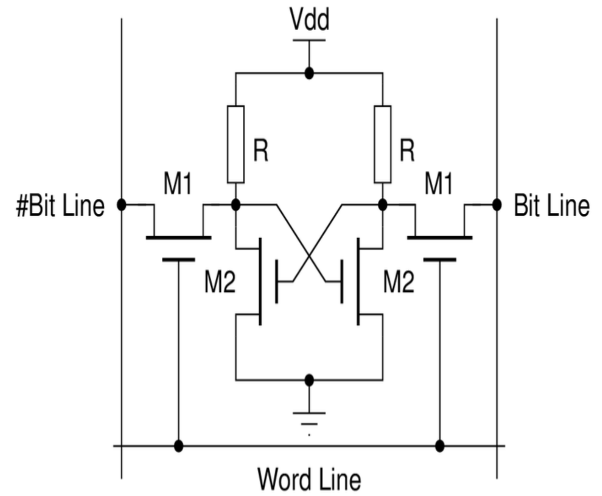
II. Different Sram Bitcell Configuration

Several SRAM bitcells have been proposed based on bit density, area, timing specification and low voltage operation. Fig. 1 lists the SRAM bitcells having four to ten transistors. In the four–transistor (4T) load less bitcell, pMOS devices act as access transistors [6]. The design requirement is such that pMOS OFF state current should be more than the pull-down nMOS transistor leakage current for maintaining the data value reliably “1”. With increasing process variations and the sub-threshold current on the threshold voltage is to satisfying this design requirement by the different process, voltage, and temperature (PVT) conditions may be challenging.

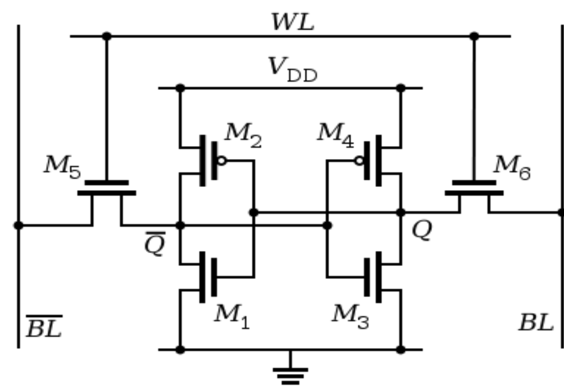
5T bitcell consists of asymmetric cross coupled inverters with a single bitline [7]. Separate bitline precharge voltages are used for read and write operations. The precharge voltage in the intermediate read bitline requires dc to ac converter. Across PVT corners to track the read precharge voltage would require additional design margins in bitcell sizing. A 6T bitcell comprises of two cross-coupled CMOS inverters, it can be accessed by two nMOS access transistors. A single-ended 6T bitcell uses a full transmission gate at one side [8]. Write-ability is achieved by modulating the virtual-VCC and virtual-VSS of one of the inverters. In the single-ended 7T bitcell consists of single-ended write operation and a separate read port.

The single-ended write operation in this 7T bitcell needs either asymmetrical inverter characteristics or differential VSS and VCC bias. The proposed another single-ended 7T bitcell in which an extra transistor is added in the pull-down path of one of the inverters. During this read mode, to isolating the corresponding storage node from VSS when the extra transistor is turned OFF. This gives results in read-disturb-free operation. The feedback between the two inverters is cut off during the write operation in differential 7T bitcell [12]. The successful write operation in an inverter sizing produces asymmetrical noise margins. The extra transistors are added to the conventional 6T bitcell to separate read and write operation, it gives the single-ended 8T bitcell. The 9T bitcell provides differential read-disturb-free operation [18]. In a single-ended 9T bitcell, separate read port is used to decouple read and write operation which is similar to the single-ended 8T bitcell. In 9T bitcell the stacked read access transistors are used to reduce the bitline leakage.

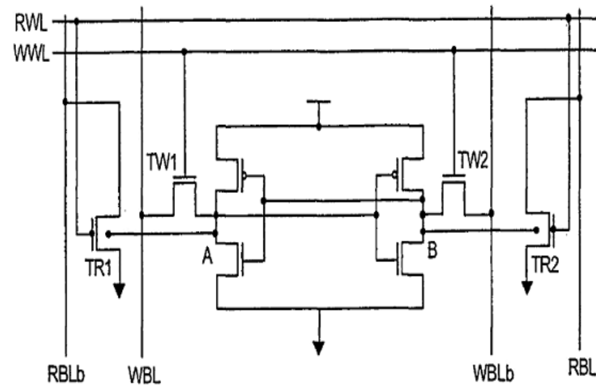
Recently, the differential 8T bitcells utilizing RWL/WWL cross-point array and data-dependent VCC have also been reported [13]. Single-ended 10T bitcells are similar to the single-ended 8T bitcell except for the read port configurations. Here to control the read bitline leakage the additional transistors are used [17], [18]. The single-ended transmission-gate 10T bitcell contents are buffered using an inverter and then transferred to the read bitline whenever the bitcell is accessed. To eliminate domino-style read-bitline sensing transmission gates are used.



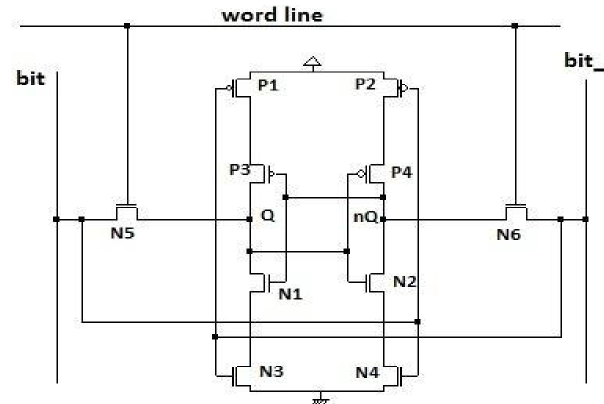
4TSRAM



6T SRAM



8T SRAM



10T SRAM

Fig.1 Different SRAM bitcell configurations

Thus, read bitline does not require precharge and keeper transistor. Also, the read-bitline toggling is avoided if the accessed data are unchanged. A differential 10T bitcell with two separate ports for read-disturb- free operation [19]. The read-disturb-free differential 10T bitcell is suitable for bit-interleaved architecture [20]. However, series-connected write access transistors degrade the write-ability of the bitcell and needs write-assist circuits such as word-line boosting for a successful write operation.

III. Schmitt Trigger (ST) SRAM Bitcells

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. To modulate the switching threshold of an inverter, Schmitt trigger is used and it depending on the direction of the input transition. The feedback mechanism is used only in the pull-down path in the proposed ST SRAM bitcells. During input transition, the feedback transistor (NF) tries to preserve the logic "1" at output node by raising the source voltage of pull-down nMOS (N1).

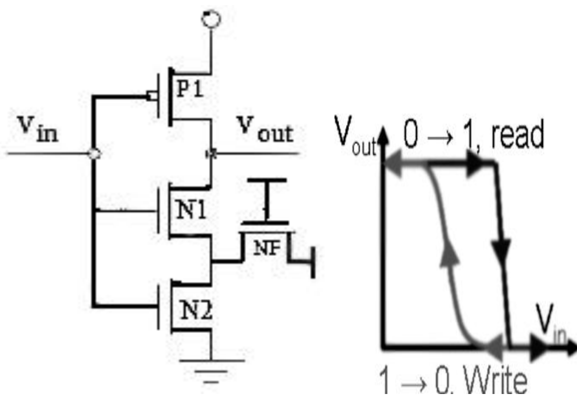


Fig.2 Conceptual ST schematics

Since a read-failure is initiated by an input transition for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation. This results in smooth transfer characteristics that are essential for easy write operation. In the SRAM bitcell, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-stability.

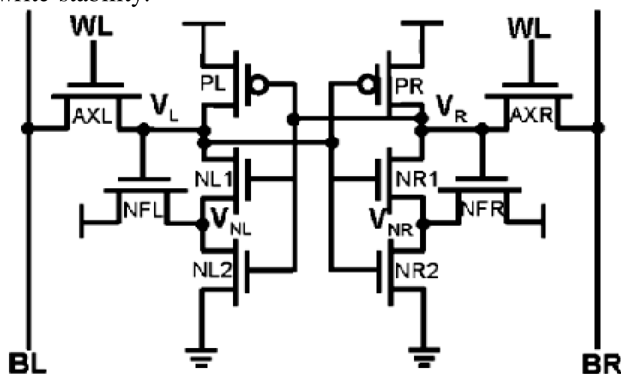


Fig.3 ST-1 Bitcell Schematics

Fig.3 shows the schematics of the ST-1 bitcell. The ST-1 bitcell utilizes differential sensing with ten transistors, one word-line (WL), and two bitline (BL/BR). Transistors PL-NL1-NL2-NFL forms one ST inverter while PR-NR1-NR2-NFR forms another ST inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the 0→1 input transition giving the ST action.

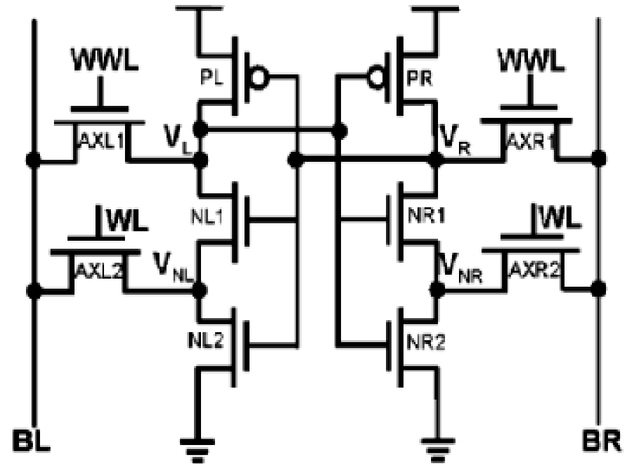


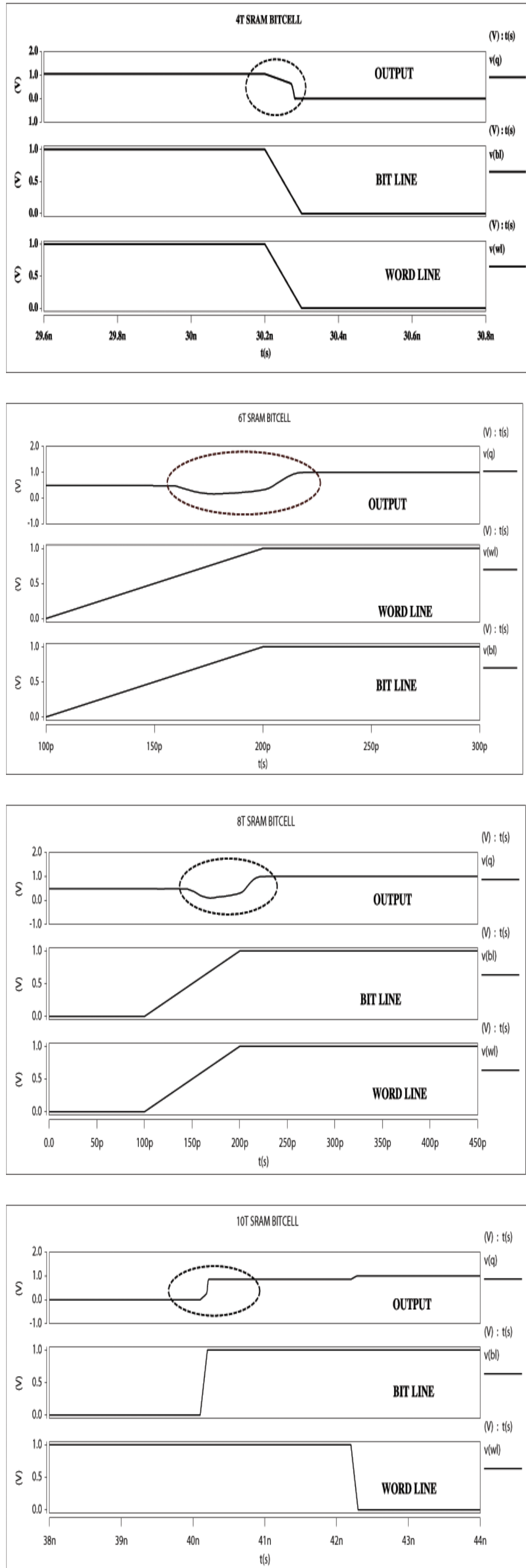
Fig.4 ST-2 Bitcell Schematics

The Fig.4 shows the ST-2 Bitcell Schematics. ST-2 bitcell utilizes the differential sensing with ten transistors, two word-lines (WL/WWL), and two bitline (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During the hold-mode, both WL and WWL are OFF. In the ST-2 bitcell, feedback is provided by separate control signal (WL) unlike the ST-1 bitcell, where in feedback is provided by the internal nodes. In the ST-1 bitcell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback.

IV. Results and Discussion

In this section, we present simulation results to demonstrate the different SRAM bitcell schematics output. The SRAM bitcell configurations are simulated using HSPICE in 180nm technology. Typical NMOS (PMOS) threshold voltage is 1V and temperature is 25˚c. The 6T and the proposed ST based bitcells are compared for various SRAM metrics. For the ST based SRAM bitcell, extra transistors AXL2/NL2 are of minimum width 180 nm while the other transistors have the same dimensions as those of the 6T cell.

The simulation results are shown below:



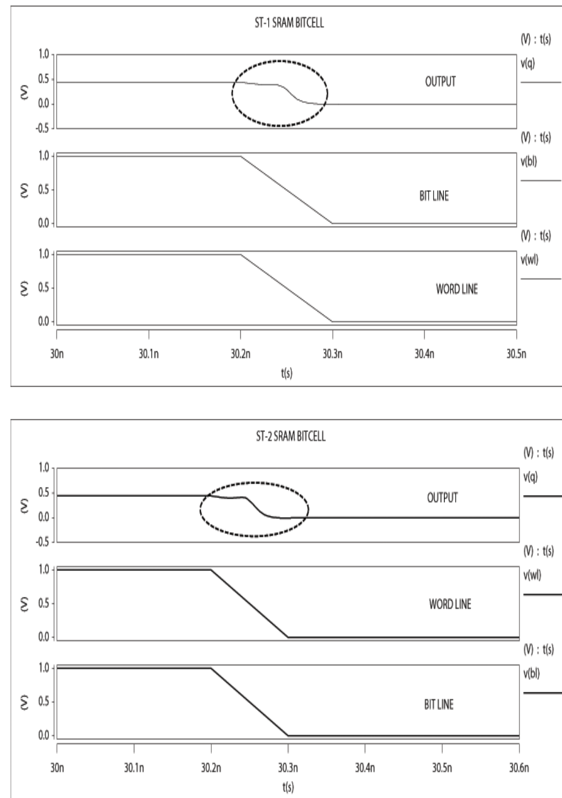


Fig. 5 Output Schematic waveforms for 4T, 6T, 8T, 10T & ST-1, ST-2 SRAM bitcell

No. of Transistor or SRAM Bitcell	Ivdd	Avg_ delay	Avg_ power	Tplh	Tphl
6T SRAM	95.857 n	7.023n	95.504n	1.928n	12.12n
ST-1 SRAM	2.838u	1.114n	2.747u	3.965n	6.19n
ST-2 SRAM	2.821u	2.005n	2.731u	10.200 n	6.189n

Table 1: Characterstic comparison of 6T, ST-1 & ST-2 SRAM

V. Conclusion

The proposed ST based SRAM bitcell gives more stability in read operation with reduced power supply voltage and correspondingly the read failure probability also decreases as compare to conventional 6T SRAM bitcell. Lowering the supply voltage is an effective way to achieve ultra-low-power operation. Here the evaluated ST based SRAM bitcells suitable for ultra-low voltage applications. The proposed ST based bitcell can be effective for process-tolerant, low-voltage SRAM operation in future nano scaled technologies. Simulation results show that the ST based bitcell can retain the data at low supply voltage.

REFERENCES

[1] K. Roy and S. Prasad, *Low Power CMOS VLSI Circuit Design*, 1st ed. New York: Wiley, 2000.
[2] N.Yoshinobu, H. Masahi, K. Takayuki, and K. Itoh, “Reviewand future prospects of low-voltage RAM circuits,” *IBM J. Res. Devel.*, vol. 47, no. 5/6, pp. 525–552, 2003.
[3] A. Bhavnagarwala, X. Tang, and J. Meindl, “The impact of intrinsic device fluctuations on CMOSSRAMcell stability,” *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, Apr. 2001.
[4] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, “Modeling of failure probability and statistical design ofSRAMarray for yield enhancement in nanoscaled CMOS,” *IEEE Trans. Comput.-Aided Design (CAD) Integr. Circuits Syst.*, vol. 24, no. 12, pp. 1859–1880, Dec. 2005.
[5] M. M. Khellah, A. Keshavarzi, D. Somasekhar, T. Karnik, and V. De, “Read and write circuit assist techniques for improving VCCmin of dense 6T SRAM cell,” in *Proc. Int. Conf. Integr. Circuit Design Technol.*, Jun. 2008, pp. 185–189.
[6] K. Noda, K. Matsui, K. Takeda, and N. Nakamura, “A loadless CMOS four-transistorSRAMcell in a 0.18-□mlogic technology,” *IEEE Trans. Electron Devices*, vol. 12, no. 12, pp. 2851–2855, Dec. 2001.
[7] I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, “A high density, low leakage, 5T SRAM for embedded caches,” in *Proc. 30th Eur. Solid State Circuits Conf/*, Sep. 2004, pp. 215–218.
[8] B. Zhai, D. Blaauw, D. Sylvester, and S. Hanson, “A sub-200 mV 6 T SRAM in 0.13 □m CMOS,” in *Proc. Int. Solid State Circuits Conf.*, Feb. 2007, pp. 332–333.
[9] S. Tawfik and V. Kursun, “Low power and robust 7T dual-Vt SRAM circuit,” in *Proc. Int. Symp. Circuits Syst.*, 2008, pp. 1452–1455.
[10] T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi, and H. Akamatsu, “A stable 2-port SRAM cell design against simultaneously read/writedisturbed accesses,” *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2109–2119, Sep. 2008.
[11] K. Takeda, Y. Hagihara, Y. Aimoto, M. Nomura, Y. Nakazawa, T. Ishii, and H. Kobatake, “A read-static-noise-margin-free SRAM cell for low- and high-speed applications,” in *Proc. Int. Solid State Circuits Conf.*, Feb. 2005, pp. 478–479.
[12] R. Aly, M. Faisal, and A. Bayoumi, “Novel 7T SRAM cell for low power cache design,” in *Proc. IEEE SOC Conf.*, 2005, pp. 171–174.
[13] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. R. Montoye, L. Sekaric, S. McNab, W. Topol, C. Adams, K. Guarini, and W. Haensch, “Stable SRAM cell design for the 32 nm node and beyond,” in *Proc. Symp. VLSI Technol.*, 2005, pp. 128–129.
[14] N. Verma and A. P. Chandrakasan, “65 nm 8T sub-Vt_ SRAM employing sense-amplifier redundancy,” in *Proc. Int. Solid State Circuits Conf.*, Feb. 2007, pp. 328–329.
[15] R. Joshi, R. Houle, K. Batson, D. Rodko, P. Patel, W. Huott, R. Franch, Y. Chan, D. Plass, S. Wilson, and P. Wang, “6.6+ GHz low Vmin, read and half select disturb-free 1.2 Mb SRAM,” in *Proc. VLSI Circuit Symp.*, Jun. 2007, pp. 250–251.
[16] V. Ramadurai, R. Joshi, and R. Kanj, “A disturb decoupled column select 8T SRAM cell,” in *Proc. Custom Integr. Circuits Conf.*, Sep. 2007, pp. 25–28.
[17] Y. Morita, H. Fujiwara, H. Noguchi, Y. Iguchi, K. Nii, H. Kawaguchi, and M. Yoshimoto, “An area-conscious low-voltage-oriented 8T-SRAM design under DVS environment,” in *Proc. VLSI Circuit Symp.*, Jun. 2007, pp. 14–16.
[18] Z. Liu and V. Kursun, “High read stability and low leakage cache memory cell,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 4, pp. 488–492, Apr. 2008.
[19] S. Lin, Y.-B. Kim, and F. Lombardi, “A highly-stable nanometer memory for low-power design,” in *Proc. IEEE Int. Workshop Design Test of Nano Devices, Circuits Syst.*, 2008, pp. 17–20.
[20] S. Verkila, S. Bondada, and B. Amrutur, “A 100 MHz to 1 GHz, 0.35 V to 1.5 V supply 256□64 SRAM block using symmetrized 9T SRAM cell with controlled read,” in *Proc. Int. Conf. VLSI Design*, 2008, pp. 560–565.

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