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Design and Simulation of an improved Strained Silicon P-MOS having Si_3N_4 cap layer

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***Abstract*— This paper describes the designing of an improved SSPMOS. A Detailed 2D Process simulation of SSPMOS and its electrical characterization has been done using TCAD (Athena and Atlas Process) Tool. For the oxide thickness, T_{ox} of 16nm and Silicon Nitride thickness (Si_3N_4) of 06 nm, the threshold voltage V_t is obtained to be -0.4V, and drain current value is 25.26 µAmp, which shows a better performance and low power consumption than previously made SSPMOS.v**

***Index Terms*— DIBL, SSPMOS, TCAD Tool.**

I. INTRODUCTION

For the past five to six years, channel length of the MOS transistors are kept reducing to almost half of its previous devices. Due to the reduction in the size of the MOS transistors resultant to the increasing packaging density in silicon chips and the clock speed in various electronic designs like motherboard of a computer, mobile phones, televisions, etc. The evolution of CMOS scaling technology had caused various problems in form of various factors.

1. First, the channel length of the MOS transistor is defined using optical lithography, which is limited by the wavelength of light.[1]
2. Short channel effects such as drain induced barrier lowering (DIBL) and punch-through problems become more difficult to manage.

2.1 **Drain induced barrier lowering (DIBL)-** When we decrease the channel length under certain condition then the space charge at the drain will interact with space charge that also present at the source leading to lowering in the potential barrier at the source to the channel. At the time when channel becomes shorter this lowering becomes pronounced. The result comes out from the source barrier lowering is to increase the drain current and decrease the threshold voltage.

2.2 Punch Through problem- The amount of punch through current depends on the potential distribution under the channel. If the depletion area around the drain well increases so far to the source side, due to that the potential barrier between source and drain will be lowered down and carriers will easily start to move from source to drain. Therefore, punch through current is highly depends on the applied drain voltage and on the source/drain junction depths.

Hetero junction MOSFETs may use a strained SiGe/SiGeC channel or strained Si or strained Ge channel. The substrate for a compressively (tinselly) strained channel would have a lower (larger) lattice constant. The channels may lie on the surface or be buried. The other freedom is to use a vertical channel. The choice of the cap layer for a buried SiGe channel is an important issue having bearing on the performance of the device. Strained Si alloy hetero structures are useful for reducing the scattering rate with carriers in the most populated band having a lower effective mass in the transport direction.[4]

The basic idea is to change the lattice constant of silicon layer on the SiGe compound layer. Changing the lattice constant changes the Energy-Band diagram considerably for such structures which cause a change in other intrinsic properties of the material.[2]

The choice of Si cap thickness plays an important role in the characteristics of the PMOS. It is preferable in design to keep the unconsumed Si cap layer as thin as possible for the following reasons:

1. To prevent carrier transport through the parasitic Si surface channel.
2. To maximize the gate-to-channel capacitance and hence to increase the SiGe MOSFET transconductance as the unconsumed Si cap in series with the oxide capacitance reduces the effective gate capacitance.

The Carrier mobility improvement has been one of the best alternatives for faster devices at lower power level. The energy band gap of Si-Ge scales almost linearly with Ge concentration and can be used to create a buried channel, where the carriers are confined. The SiGe layer is therefore capped by a Si layer that is partially oxidized to form the gate dielectric. If the size of Si cap layer is too thick, a parallel inversion layer is formed at the interface, thereby decreasing the effective mobility. If the size of cap layer is too thin, the holes in the SiGe channel begin to scatter from the Si/SiO interface. There has been considerable interest in SiGe channel p-MOS devices, where the carrier are confined in a narrow SiGe quantum well channel, rather than at the usual Si/SiOg interface. These Si/SiGe devices exhibited higher level carrier mobility and transconductance for two reasons:

1. The Si/SiGe interface is an improvement over the standard Si/oxide interface
2. The carrier mobility in the channel is higher because the in-plane effective mass in the lowest-lying (first) quantum well sub band is considerably smaller than in bulk Si.

Another significance of the SiGe p-MOS structure is that, the channel is buried, hot carrier degradation of the oxide is

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expected to be reduced. . In addition, the increased probability of impact ionization in the drain region in the lower band gap alloy might provide an energy dissipation mechanism, which would reduce the hot carrier population. The smaller band gap, however, leads to lowering of the breakdown field and increased drain leakage. So it is desirable to fabricate buried channel SiGe devices with an optimized Si cap.

II. Design Considerations for SiGe PMOS

The design parameters for SiGe channel FETs are the choice of gate material, the method of threshold voltage Vt adjustment, the SiGe profile in the channel, the channel and cap doping, and the gate oxide thickness.

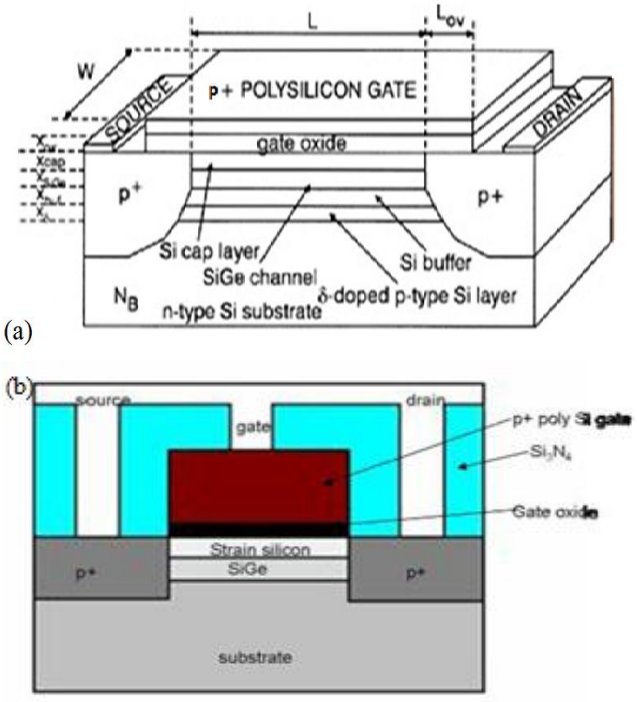

Figure-1: (a) Layer structure of a Si/SiGe/Si p-MOSFET. [2]
(b) The strain silicon PMOS Device structure.[1]

In a SiGe p-HFET, in addition to the oxide thickness t_{ox} the ratio of oxide layer thickness to Si cap thickness t_{cap} plays an important role in determining the hole confinement gate voltage range $V_{crit,}$ which is defined as the point at which the parasitic surface channel turns on in addition to the SiGe channel. It has been shown that V_{crit} increases as the ratio t_{ox}/t_{cap} increases.[2]

III. Experimental Considerations and Observations

The report is looking into the enhancement of conventional PMOS by incorporating a strained-silicon within the channel and bulk of semiconductor. A detailed 2D process simulation of Strained Silicon PMOS (SSPMos) and its electrical characterization was done using Silvaco TCAD tool [1].

The process manufacturing simulations are done using Athena environment and the device electrical characterization is done using Atlas environment. Theoretically, the mobility of holes in SiGe p-MOSFETs should show enhancement over that in bulk Si. The disproportionately large increase of the SiGe mobility relative to Si is due to the reduced surface scattering in the former. Surface scattering dominates due to the reduction of phonon scattering at low temperature. Therefore, the variation of surface scattering mobility (μ_{sr}) as a function of average separation of the carriers from the surface (Z_{avg}) needs to be known for designing the cap layer.[2]

IV. Strained p-MOS Design

A. Process Simulations and Parametric Analysis

The strained silicon PMOS with an added SiGe layer process simulation were carried out using ATHENA. Figure-2 & 3 shows the structure of device. The simulation process to create the strain silicon PMOS is similar to the conventional PMOS fabrication process.

The fabrication of SSPMOS device starts by creating a silicon substrate of <100> orientation with phosphorus doping of 2 $x10^{18}$ cm^{-3} and then a silicon layer with the thickness of 0.010 µm is deposited on the silicon substrate. The various models employed for diffusion [9] are:

1) advanced point defect model with full charge states for dopants and clusters, solubility defects,;
2) equilibrium model for fast simulations of large structures;
3) advanced calibration parameters;
4) poly-Si model for grain boundary diffusion;
5) epitaxy.

All these models are employed for simulations by Athena for second order effects always. Next a silicon germanium (SiGe) layer is deposited on the silicon layer, followed by the deposition of another silicon layer with 0.006 µm thickness onto the SiGe layer. After the deposition, strained silicon is created at the channel. Polysilicon is then deposited and patterned to form the gate.

The type of gate material strongly influences the degree of hole confinement to the SiGe channel. The strained Si p-MOSFET using an n^+-poly gate suffers from severe short-channel effects often leading to use of dual-work function poly-Si gates in modern Si-CMOS technology. However, the introduction of a SiGe channel can extend the p-channel MOSFET operation into the deep submicron regime. Here the use of p-poly is incorporated. Simulations have been performed for both type of electrodes. The process continues with the implantation of source/drain. The boron is implanted with the1.0 x 10^{15} cm^{-2} doping concentration and energy of 10KeV without tilt.

Monte Carlo, Pearson and Gaussian distribution functions have been employed and device is simulated for all these models. These models have been observed for energies upto 20KeV. Greater than that the threshold adjust is lost and the enhancement mode property is lost. Moreover the higher energy implantations cause greater dislocations and higher creation of interstitials and vacancies causing unwanted scattering and also very low voltage breakdown of the device. So, the model illustrated above is employed. All these processes were followed by a low temperature annealing using nitrogen ambient atmosphere at 900°C and 1 atm pressure. [2]

Next the silicon nitride (Si3N4) layer is deposited and patterned to cover the gate, source and drain. Then the aluminum is deposited and patterned to act as the metal contact. Finally, the final structure of the strained silicon PMOS is created as shown in Figure-2 & Figure-3. The

SSPMos structure is added a SiGe layer, thin Si layer and Si3N4 capping layer, created with 0.016 µm gate oxide thickness and 0.68µm (Which was 0.70 µm in previous one [2]) channel length.

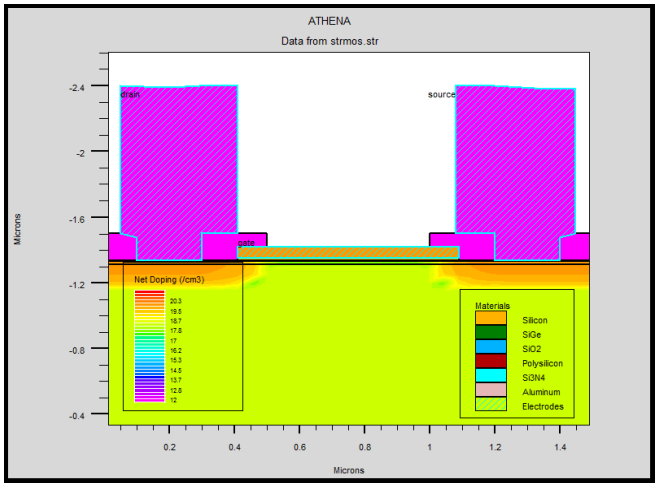

Figure-2: Strained Silicon PMOS (made using Athena)

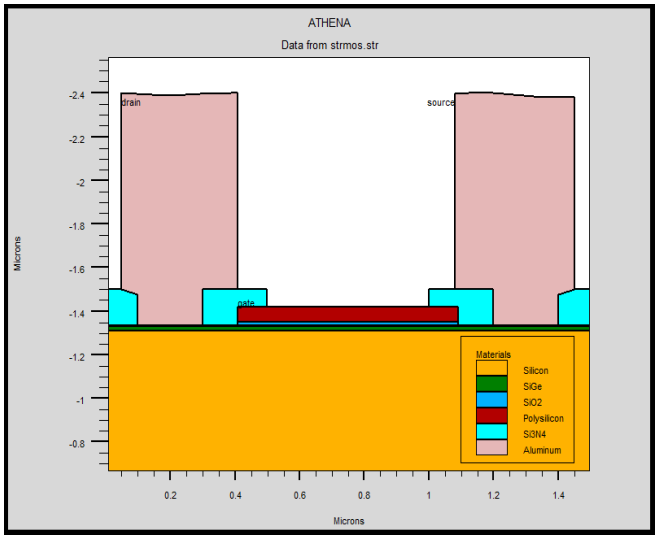

Figure-3: Strained silicon PMOS showing various regions of the SSPMOS

B. Electrical Characterizations And Comparisons

The characteristics of the strained silicon PMOS (SSPMos) is obtained by atlas process. The mobility models that are used to obtain the electrical characteristics are the parallel electric field dependence and concentration dependent mobility Structure. Except these, the carrier static lifetime of Si material is set at le-7 tau for both electron and hole. Meanwhile the Si-Ge material is set to le-8 tau for both electron and hole.

For the carrier statistic model, the band-gap narrowing and Boltzmann are chosen in this simulation. As for the recombination models, the auger and SRH concentration dependent lifetimes are chosen. Further, for simulation of breakdown phenomenon Impact Ionization model is chosen. The characteristics of the devices that was obtained from the simulation are the drain current versus gate voltage curve, threshold voltage, drain induced barrier lowering (DIBL) and drain current versus drain voltage curve.

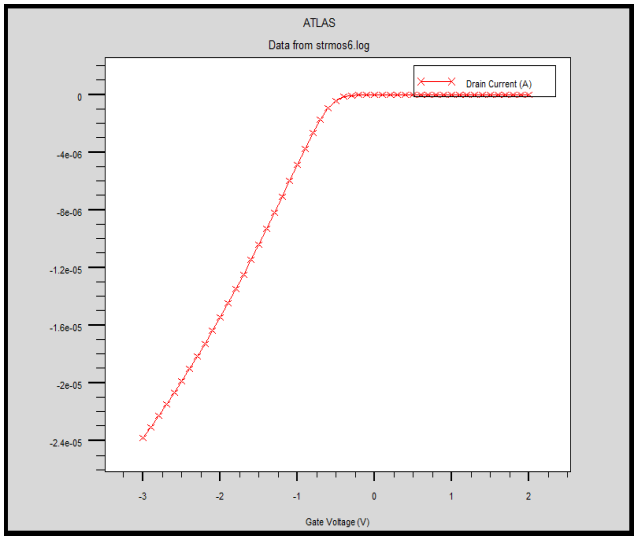

Figure-4: I_d v/s V_{gs} Characteristic for SSPMOS Device

from the simulation, the drain current, I_d v/s gate voltage, Vgs Characteristic with a drain voltage for the SSPMos devices is shown in figure 4. Meanwhile the extracted threshold voltage parameter from fig.4 is -0.4V and from base paper are -0.5V and -0.92902V for the strained PMOS (New), Previous SSPMOS and Conventional PMOS respectively. This indicates that the strained PMOS has lower threshold voltage then the Previous SSPMOS and conventional PMOS which translate to lower power consumption and it also indicates that as the Channel Length decreases, threshold voltage also decreases.

I_d v/s V_{ds} Characteristics from Atlas is also observed and shown in the figure-5.

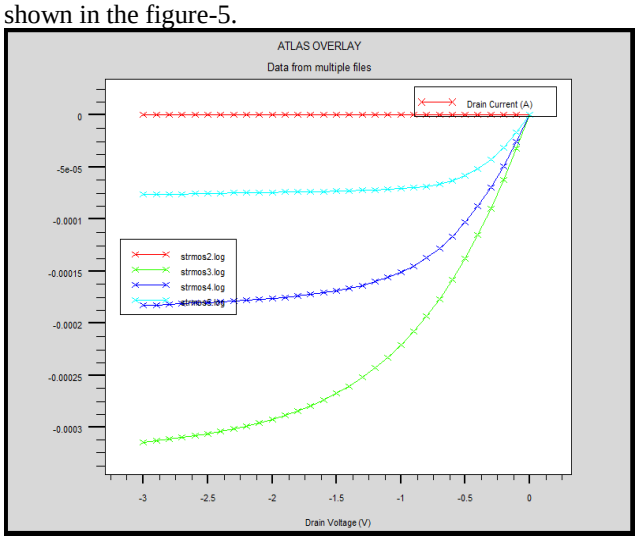

Figure-5: I_d v/s V_{ds} Characteristics for SSPMOS Device

Both structures are simulated to ramp the drain voltage, V_{ds} to -3.3V when various gate voltages Vgs (-1.1V, 2.2V and -3.3V) are applied. The simulation results are presented in Figure-5 which represents the graph of the drain current, I_d v/s drain voltage, V_{ds}. From Figure-4, it can be seen that the new strained PMOS device has a higher drive current i.e. 25.26 µamp is compared with the previous SSPMOS [2] i.e. around 22.83 µamp while it is also clear that the new SSPMOS has higher drive current than previous SSPMOS device. The graphical representation is shown in figure-6.

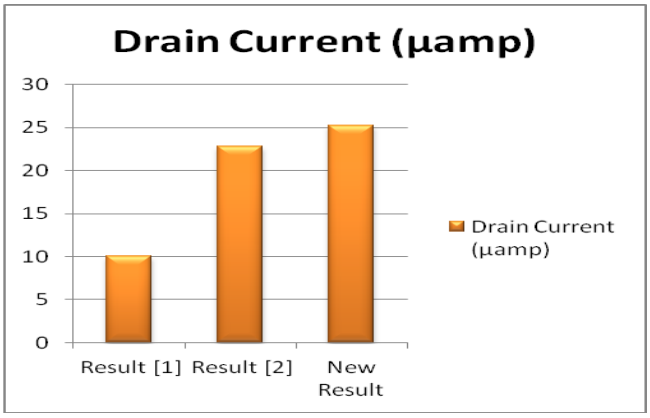

Figure-6: The graphical representation of previously made SSPMOS results and new SSPMOS result.

V. CONCLUSION

From the above results, it is worth considering some general features of the SSMOS devices simulated. Further improvements in the transconductance and a greater current driving capability further enhances the application of the device to compact and yet, faster devices. The low power operation also enables us to further visualize the advantage of the device for small supply voltage applications as the technology scales down.

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