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A 8x8 bit multiplier using Vedic Mathematics

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***Abstract*— Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved the efficiency of Urdhva Triyagbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels using Karatsuba algorithm with the compatibility to different data types. Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of all types of numbers, either small or large. Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Spartan 3E kit have been done and output has been displayed on LCD of Spartan 3E kit. The synthesis results show that the computation time for calculating the product of 8x8 bits is 15.05 ns.**

***Index Terms*—Vedic Mathematics, 8x8 bit, Urdhva Triyagbhyam.**

I. VEDIC MULTIPLICATION:

Vedic multiplication is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formula) and 16 sub formula after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself.

Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become

an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful [2, 3].The word "Vedic" is derived from the word "Veda" which means the store-house of all know.

II. VARIOUS SUTRAS FOR VEDIC MULTIPLICATION:

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc[15]. These Sutras along with their brief meanings are enlisted below alphabetically

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.

2. Chalana-Kalanabyham – Differences and Similarities.

3. Ekadhikina Purvena – By one more than the previous One.

4. Ekanyunena Purvena – By one less than the previous one.

5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.

6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.

7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.

8. Paraavartya Yojayet – Transpose and adjust.

9. Puranapuranabyham – By the completion or noncompletion.

10. Sankalana- vyavakalanabhyam – By addition and by subtraction.

11. Shesanyankena Charamena – The remainders by the last digit.

12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.

13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.

14. Urdhva-tiryagbhyam – Vertically and crosswise.

15. Vyashtisamanstih – Part and Whole.

16. Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trignometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome -looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on 16
which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial-parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

III. NIKHILAM SUTRA

Nikhilam Sutra stands for "all from 9 and last from 10"[18].Basically this method is use in all type of multiplication, but most efficiently use in large number multiplications. This method take a nearest base of number, larger the number lesser the complexity in multiplication.Lets take an example of 96x 93 where we take base 100 which is near to number and grater to number as shown below fig.

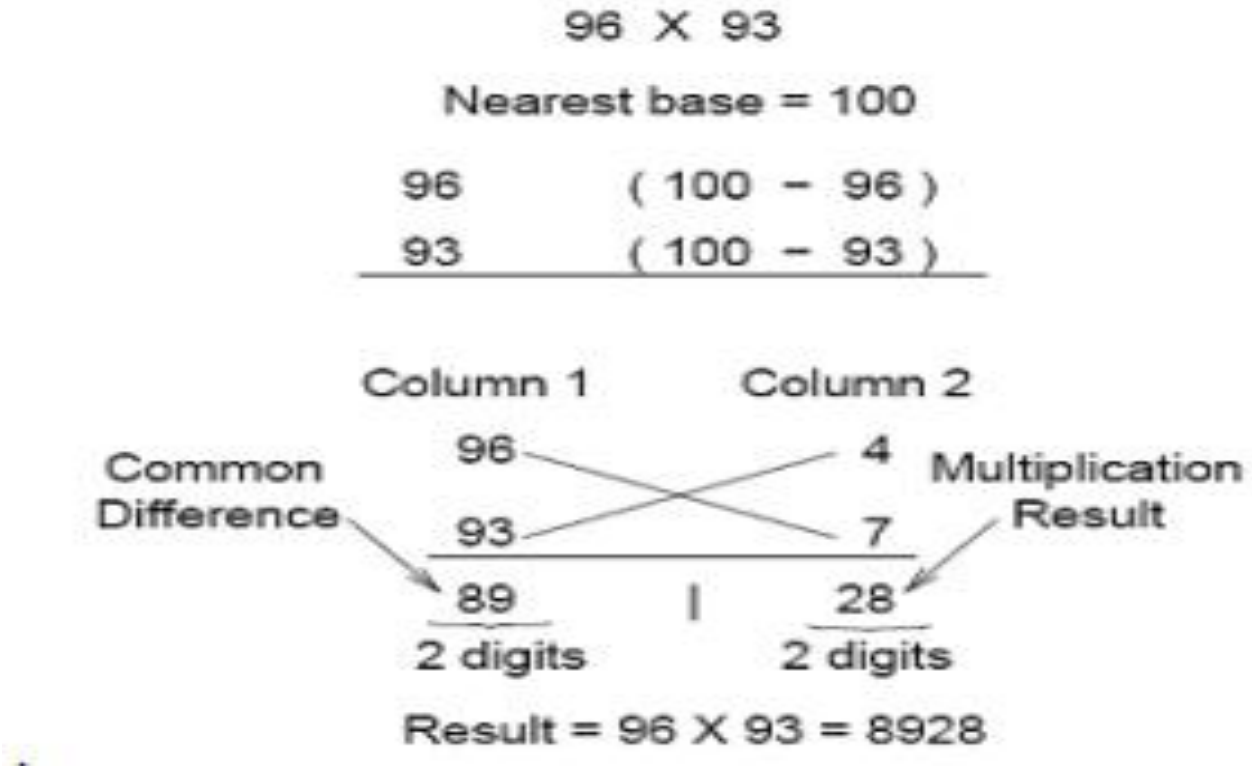


Fig. Nikhilam Line Diagram

The proposed Nikhilam sutra architecture is shown in Fig.1.4 and is based on the above illustration of the sutra.

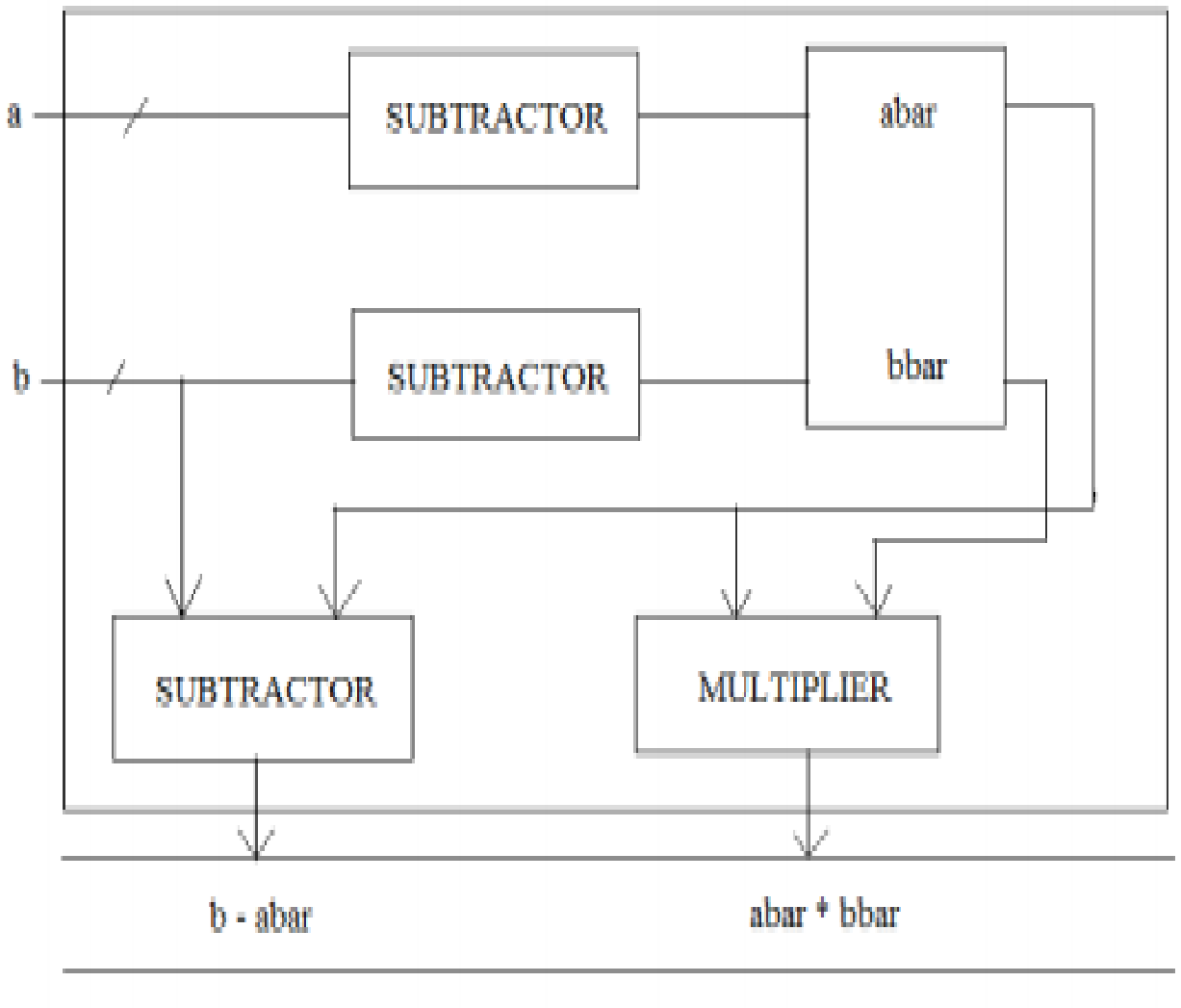


Fig: architecture of Nikhilam sutra multiplier

IV. YAAVADUNAM SUTRA

Whatever the deficiency subtract that deficit from the number and write along side the square of that deficit.It is also called as **Yaavadunam Sutra**

This sutra is helpful in finding squares and cubes of any two digit-numbers .It can extend up to any number of digits for finding the square and cubes of that particular number. But here its going to use this sutra with different methods for finding squares for any two-digit and three-digit numbers .

V. VEDIC MULTIPLICATION USING URDHAVA TIRYAKBHYAM SUTRA

In this project I have proposed the multiplication algorithm which avoids the need of large multipliers by reducing the large number to the smaller number multiplication‟s count which reduces the propagation delay. The structure of the proposed algorithm is based on the Urdhava Tiryakbhyam Sutra (formula) of Vedic mathematics which is simply means: “vertical and crosswise multiplication”.

Multiplication is based on an algorithm called Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. The Sanskrit term means “Vertically and crosswise”. The idea here is based on a concept which results in the generation of all partial products along with the concurrent addition of these partial products in parallel. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in Fig. Since there is a parallel generation of the partial products and their sums, the processor becomes independent of the clock frequency. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency.

Methodology of Parallel Calculation:

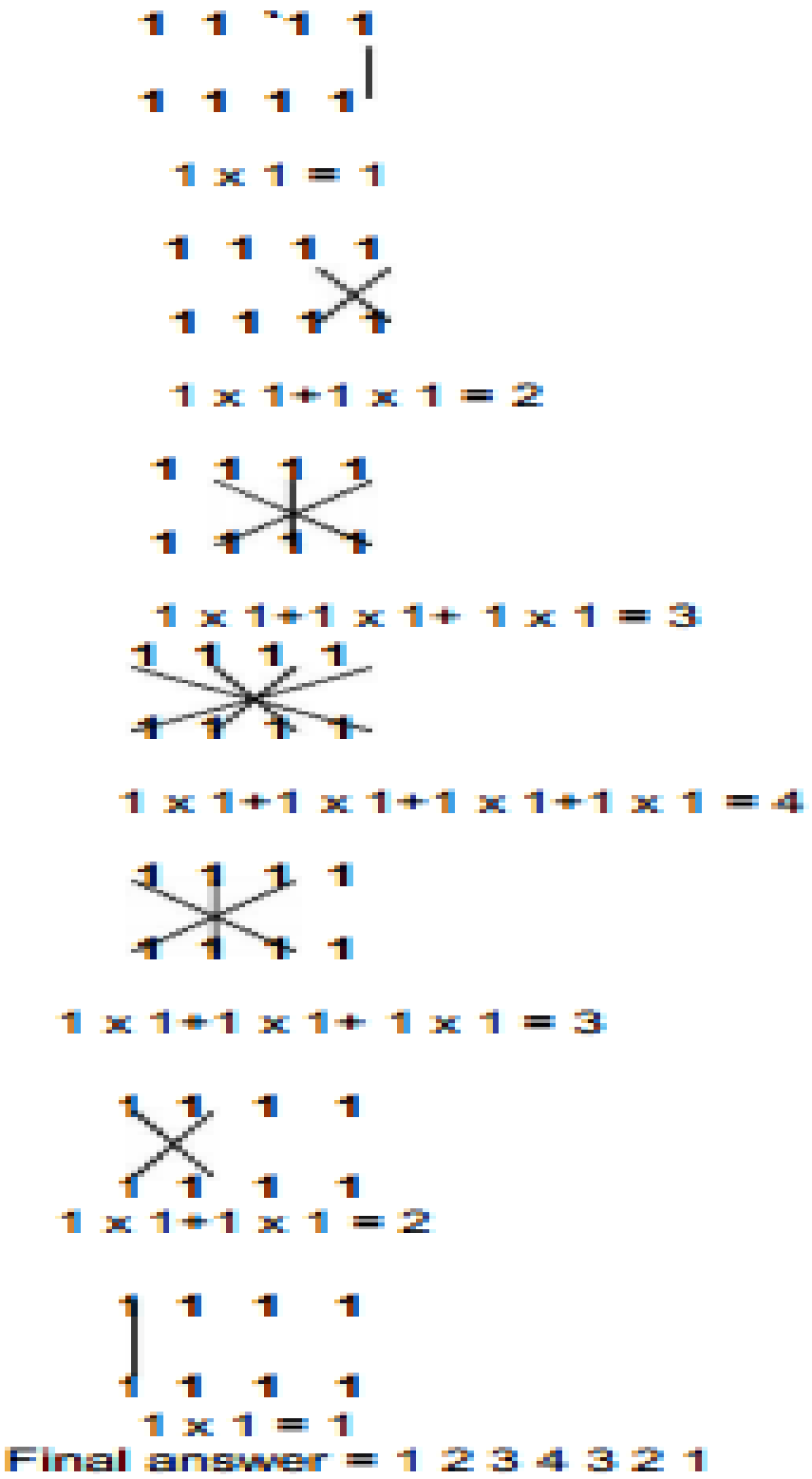


Fig: Methodology of Parallel Calculation

Multiplication of two decimal numbers- 325*738

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.3.3. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero. To make the methodology more clear, an alternate illustration is given with the help of line diagrams in fig.

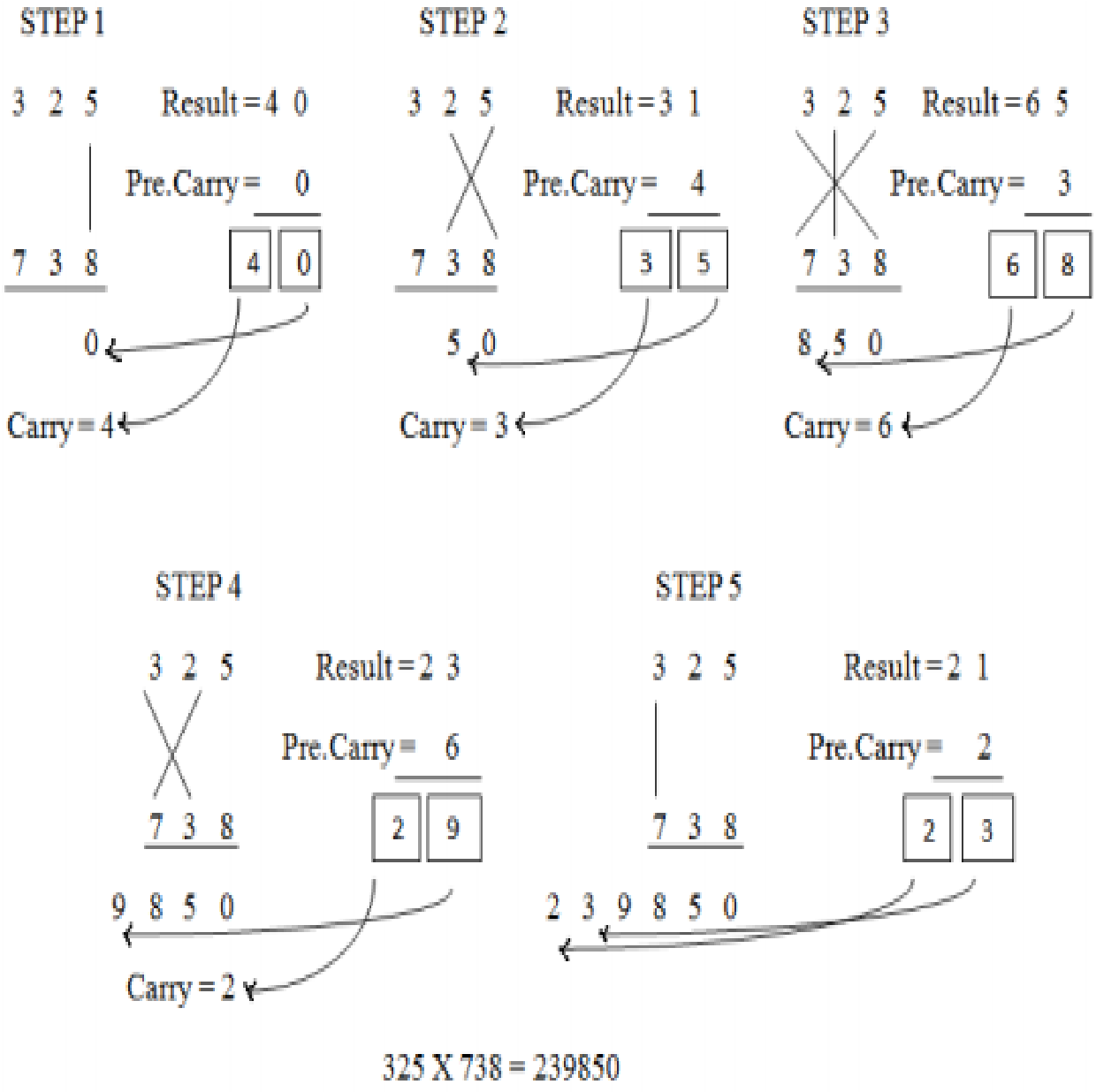


Fig. .3.4 Multiplication of two decimal numbers by Urdhva Tiryakbhyam

VI. DESIGN OF 8×8 BLOCK:

The design of 8×8 block is a similar arrangement of 4×4 blocks in an optimized manner as in Fig 3.9. The first step in the design of 8×8 block will be grouping the 4 bit (nibble) of each 8 bit input. These quadruple terms will form vertical and crosswise product terms. Each input bit-quadruple is handled by a separate 4×4 Vedic multiplier to produce eight partial product rows. These partial products rows are then added in an 8-bit carry look ahead adder optimally to generate final product bits. The figure 3.9 shows the schematic of an 8×8 block designed using 4×4 blocks. The partial products represent the Urdhva vertical and cross product terms. Then using or and half adder assembly to find the final product.

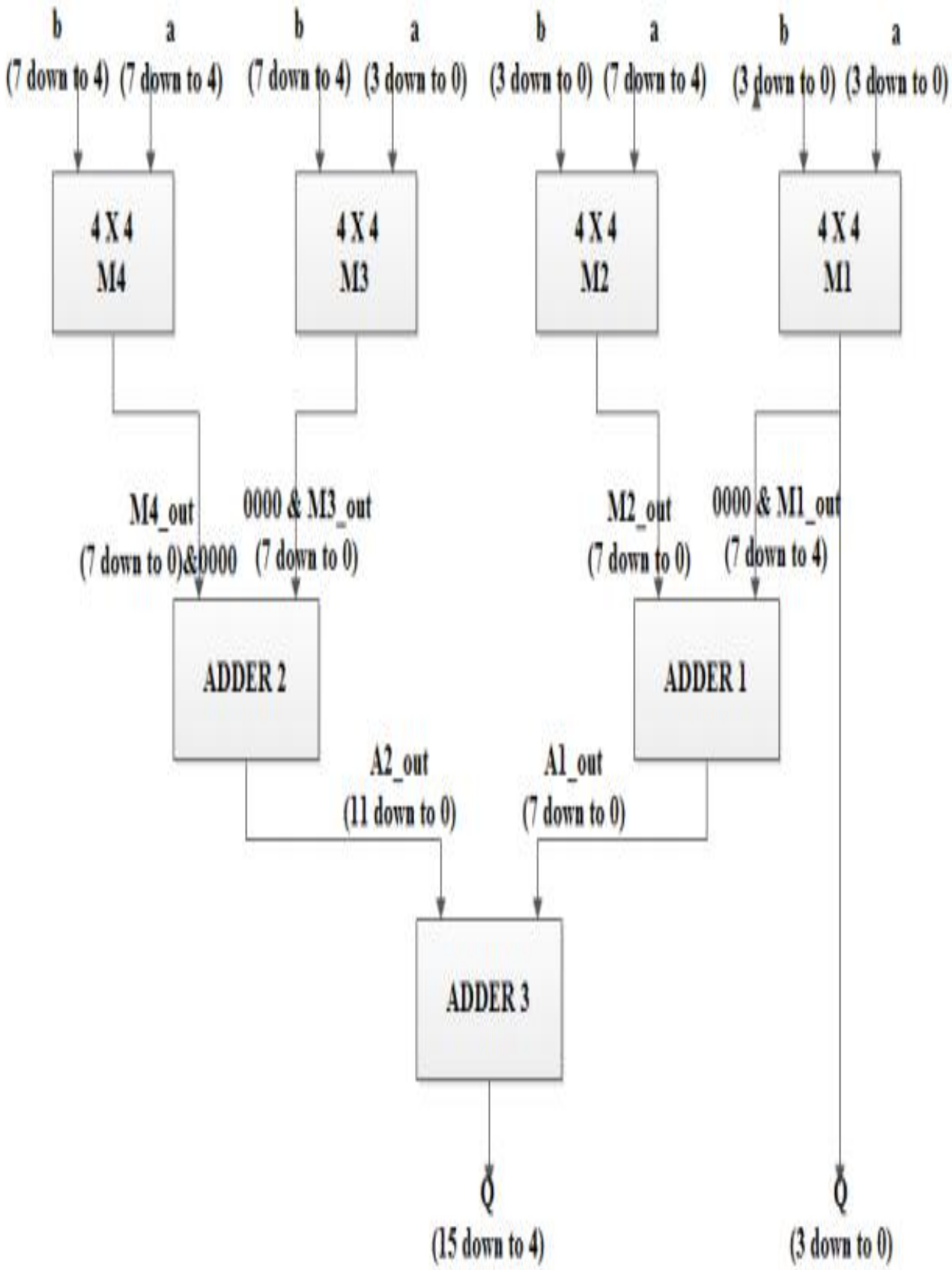


Fig.: Hardware realization of 8 x 8 multiplier

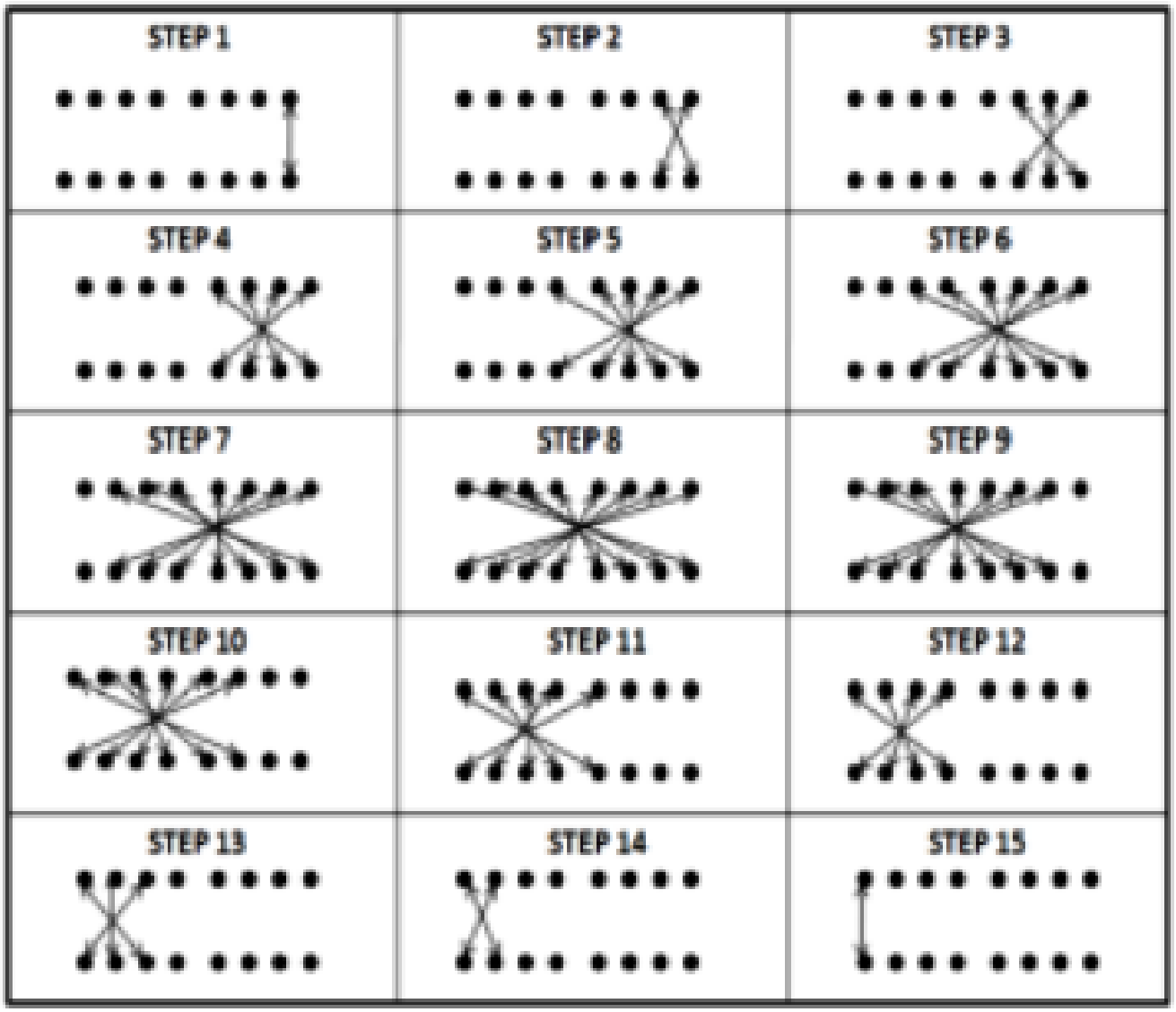


Fig.8-bit binary multiplication using Urdhva Tiryakbhyam Sutra

Algorithm for 8 X 8 Bit Multiplication Using Urdhva Triyakbhyam (Vertically and crosswise) for two Binary numbers

A = A7A6A5A4 A3A2A1A0

X1 X0

B = B7B6B5B4 B3B2B1B0

Y1 Y0

X1 X0

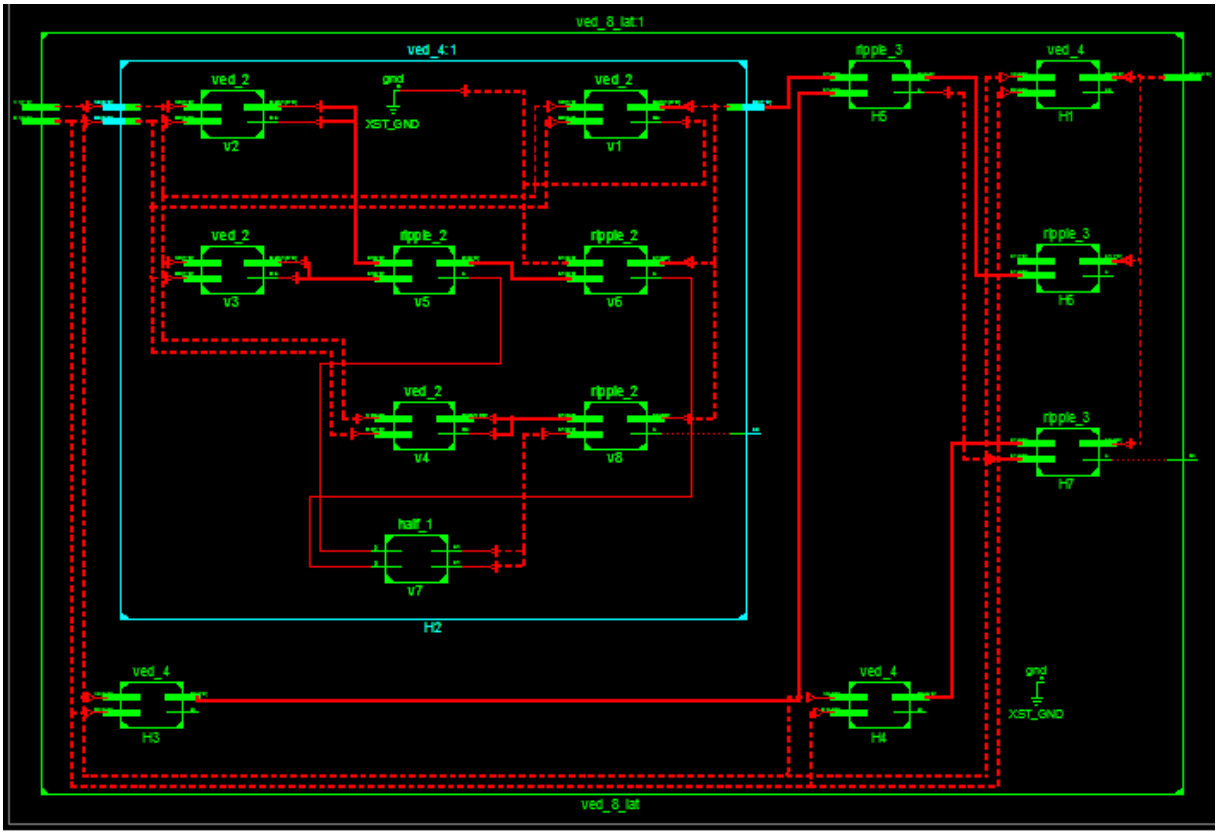
* Y1 Y0

F E D C

CP = X0 * Y0 = C

CP = X1 * Y0 + X0 * Y1 = D

CP = X1 * Y1 = E



RTL Schematics of 8x8 multiplier

ved_8_lat Project Status (05/29/2014 - 13:17:17)			
Project File:	ved_8_lat.xise	**Parser Errors:**	No Errors
Module Name:	ved_8_lat	**Implementation State:**	Programming File Generated
Target Device:	xc3s400-5pq208	**• Errors:**	No Errors
Product Version:	ISE 12.4	**• Warnings:**	6 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	171	7,168	2%	
Number of occupied Slices	95	3,584	2%	
Number of Slices containing only related logic	95	95	100%	
Number of Slices containing unrelated logic	0	95	0%	
Total Number of 4 input LUTs	171	7,168	2%	
Number of bonded IOBs	33	141	23%	
Average Fanout of Non-Clock Nets	3.40			

Performance Summary			
Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:			

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu May 29 13:16:41 2014	0	6 Warnings (0 new)	0
Translation Report	Current	Thu May 29 13:16:56 2014	0	0	0
Map Report	Current	Thu May 29 13:16:59 2014	0	0	2 Infos (0 new)
Place and Route Report	Current	Thu May 29 13:17:04 2014	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Thu May 29 13:17:07 2014	0	0	5 Infos (0 new)
Bitgen Report	Current	Thu May 29 13:17:14 2014	0	0	1 Info (0 new)

Secondary Reports		
Report Name	Status	Generated
ISIM Simulator Log	Out of Date	Wed May 28 14:53:31 2014
Post-Synthesis Simulation Model Report	Current	Thu May 29 13:16:51 2014
WebTalk Report	Current	Thu May 29 13:17:15 2014
WebTalk Log File	Current	Thu May 29 13:17:17 2014

Date Generated: 05/29/2014 - 13:17:18

VII. CONCLUSION

We can realize a high speed multiplier using Urdhva Tiryagbhyam sutra and carry skip addition technique. A 4-bit modified multiplier is designed. The 8-bit multiplier is realized using four 4-bit Vedic multipliers and modified ripple carry adders. Ripple carry adders are modified because not all bits have same weight and hardware can be reduced by reducing the number of full adders used. Though the number of gates used is fairly high, the increase in speed compensates for the increase in area. The proposed 8-bit multiplier gives a total delay of 15.050 ns which is less when compared to the total delay of any other renowned multiplier architecture. Results also indicate a 13.65% increase in the speed when compared to normal Vedic multiplier without carry-skip technique.

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