Realization of basic memory elements by bicmos logic and comparative study with cmos logic

Tarun Kumar Das, Avinash Kr. Jha

Abstract— **In recent years, improved technology has made it possible to combine complimentary MOS transistors and bipolar devices in a single process at a reasonable cost. BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies - those of the bipolar junction transistor and the CMOS transistor - in a single integrated circuit device. Our paper describes the designing of basic memory elements by BiCmos logic and comparative study with CMOS logic. An experiment was conducted through this components & the simulation results are presented. For the simulation transient analysis was performed for all the circuits & corresponding values of logic HIGH & logic LOW are measured from the graph.**

***Index Terms*— BJT, CMOS, BiCMOS**

I. INTRODUCTION

BJT logic: Bipolar transistors are so named because their operation involves both electrons and holes. These two kinds of charge carriers are characteristic of the two kinds of doped semiconductor material. In contrast, unipolar transistors such as the field-effect transistors have only one kind of charge carrier. BJTs come in two types, or polarities, known as PNP and NPN based on the doping types of the three main terminal regions. An NPN transistor comprises two semiconductor junctions that share a thin p-doped anode region, and a PNP transistor comprises two semiconductor junctions that share a thin n-doped cathode region.

A. Advantages:

- Higher switching speed
- Higher current drive per unit area, higher gain
- Generally better noise performance and better high frequency characteristics
- Improved I/O speed (particularly significant with the growing importance of package limitations in high speed systems).
- lower input impedance (high drive current)
- low voltage swing logic
- high g_m ($g_m \alpha$ Vin)
- high unity gain band width (f_t) at low currents

Manuscript received September 27, 2013

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B. Disadvantages

- Higher static power dissipation
- Lower noise margins
- Lower packing density – higher manufacturing cost per device
- Low yield with large integrated complex functions

C. CMOS Logic:

CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-channel and n-channel metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. It is called as complementary MOSFET because the pMOS & nMOS are connected in push pull arrangement. When nMOS is turned on, pMOS is turned off & the output pulls down to ground potential. Again when nMOS is turned off, pMOS is turned on & the output pulls up to power supply. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication.

D. Advantages

- Lower static power dissipation
- Higher noise margins
- Higher packing density – lower manufacturing cost per device
- High yield with large integrated complex functions
- High input impedance (low drive current)
- Scaleable threshold voltage
- Low output drive current (issue when driving large capacitive loads)
- Low transconductance, where transconductance, $g_m \alpha V_{in}$
- Bi-directional capability (drain & source are interchangeable)

E. Disadvantages

- Lower switching speed
- Lower current drive per unit area, Lower gain
- Generally reduced noise performance and reduced high frequency characteristics

- Reduced analogue capability
- Reduced I/O speed (particularly significant with the growing importance of package limitations in high speed systems).

F. The BiCMOS Logic:

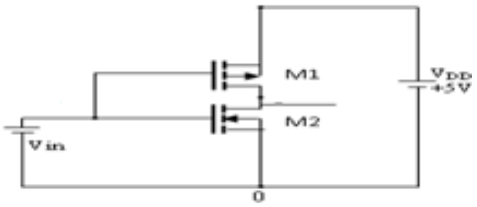
- BiCMOS Technology combines Bipolar and CMOS Circuits on one IC chip.
- CMOS (low-power, high input impedance, wide noise margins) + Bipolar (high current-driving capability).
- Particularly useful for logic with large fan-out (large capacitive load).

G. Combined advantages in BiCMOS Technology

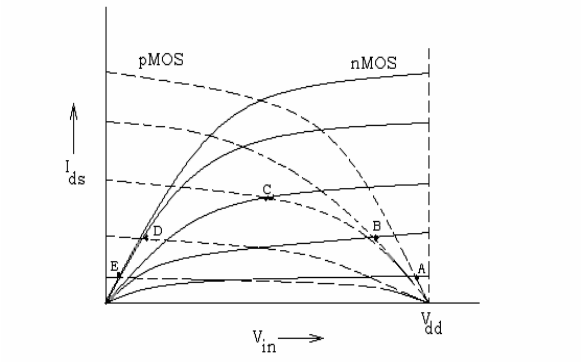
- Improved speed over purely-CMOS technology
- Lower power dissipation than purely-bipolar technology (simplifying packaging and board requirements)
  Flexible I/Os (i.e., TTL, CMOS or ECL) – BiCMOS technology is well suited for I/O intensive applications. ECL, TTL and CMOS input and output.

II. Results & Analysis

A. CMOS inverter realization:

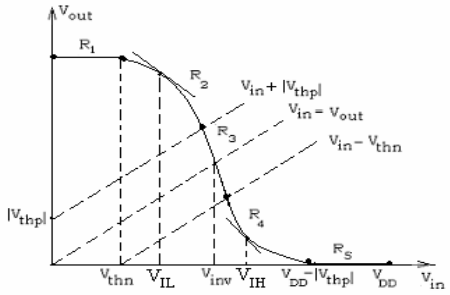


B. Current Voltage Characteristics:



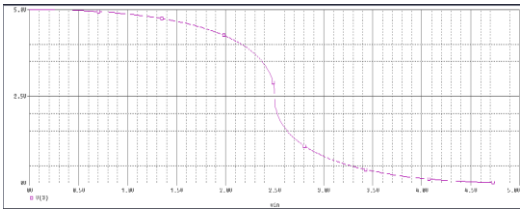
Drain-to-Source current characteristics with varying input voltages for n-MOS and p-MOS transistors.

C. CMOS inverter- Voltage Transfer Characteristics:

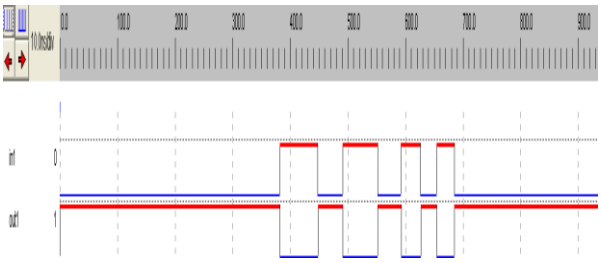


- **Region R1: 0 < Vin< Vthn**, NMOS transistor is off, PMOS device operates in the linear region.
- **Region R2: Vthn< Vin< VDD-|Vthp| and Vin + |Vthp| < Vout≤VDD**, NMOS transistor in saturation, and PMOS transistor still in the linear region.
- **Region R3: Vthn<Vin<VDD-|Vthp| and Vin-Vthn≤Vout≤Vin+ |Vthp|**, both the transistors are in saturation.
- **Region R4: Vthn< Vin< VDD–|Vthp| and Vout < Vin -Vthn**, NMOS transistor is in the linear region and PMOS remains in saturation.
- **Region R5: VDD–|Vthp| < Vin< VDD**, PMOS transistor in cut-off, NMOS in the linear region.

D. Voltage Transfer Characteristics curve.



E. Transient analysis of CMOS inverter:



F. CMOS NAND gate realization

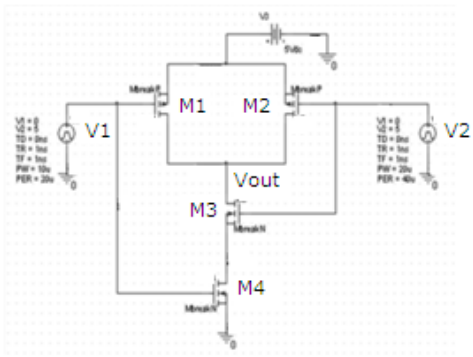
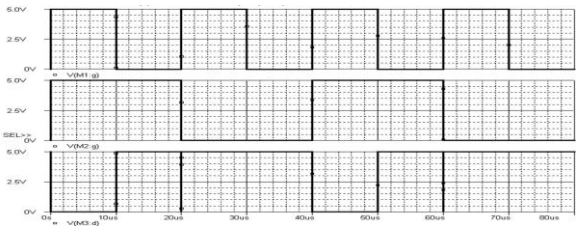


Table 1. Operating regions of the transistors:

V1	V2	Vout	Operating regions			
			NMOS		PMOS	
			M3	M4	M1	M2
0	0	VDD	Cut-off	Cut-off	Linear	Linear
0	VDD	VDD	Cut-off	Linear	Linear	Cut-off
VDD	0	VDD	Linear	Cut-off	Cut-off	Linear
VDD	VDD	0	Linear	Linear	Cut-off	Cut-off

G. Transient analysis of CMOS NAND gate:



From the transient analysis shown above
Vout=Vdd=5V(Logic HIGH)
Vout=0V(Logic LOW)

H. CMOS NOR gate realization:

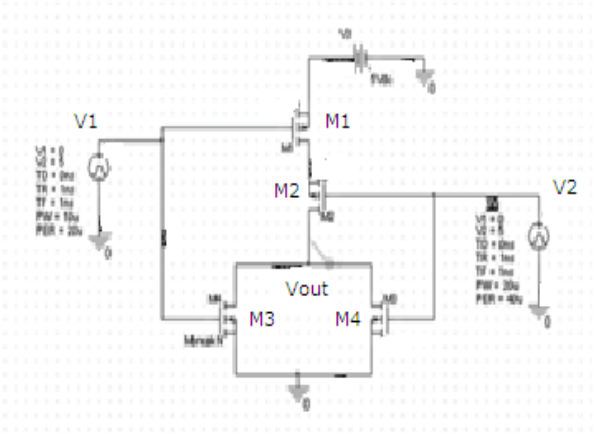
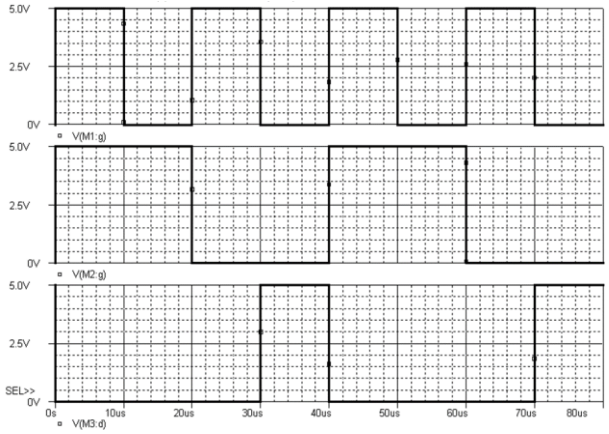


Table 2. Operating regions of the transistors:

V1	V2	Vout	Operating regions			
			NMOS		PMOS	
			M3	M4	M1	M2
0	0	VDD	Cut-off	Cut-off	Linear	Linear
0	VDD	0	Cut-off	Linear	Linear	Cut-off
VDD	0	0	Linear	Cut-off	Cut-off	Linear
VDD	VDD	0	Linear	Linear	Cut-off	Cut-off

I. Transient analysis of CMOS NOR gate:



From the transient analysis shown above
Vout=Vdd=5V(Logic HIGH)
Vout=0V(Logic LOW)

J. Logic Diagram of S'R' NAND Latch

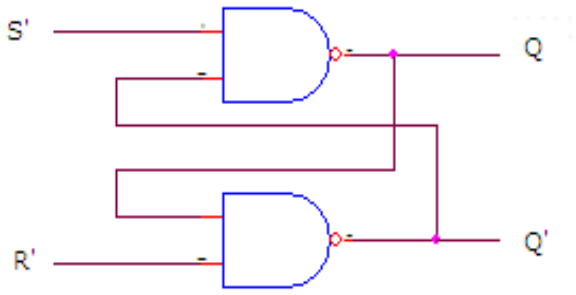
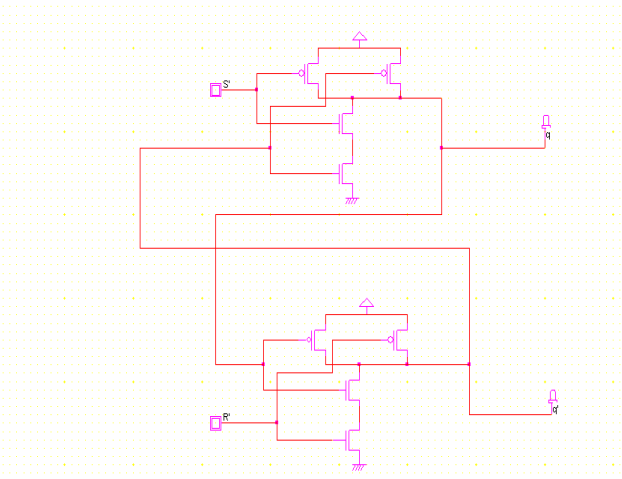


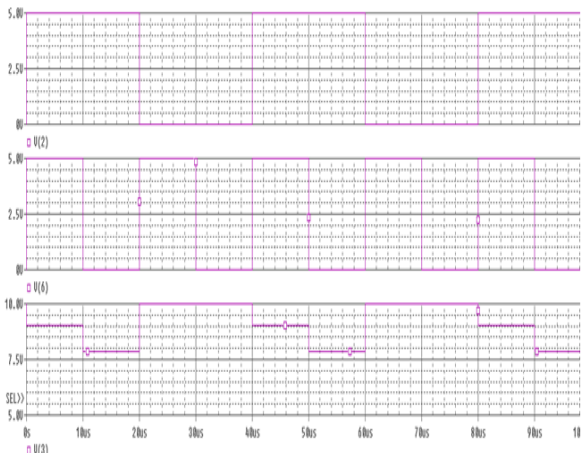
Table 3. Truth Table of S"R" NAND Latch

S'	R'	Q	Q'	Comment
0	0	1	1	Invalid
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	Q'	Unchanged

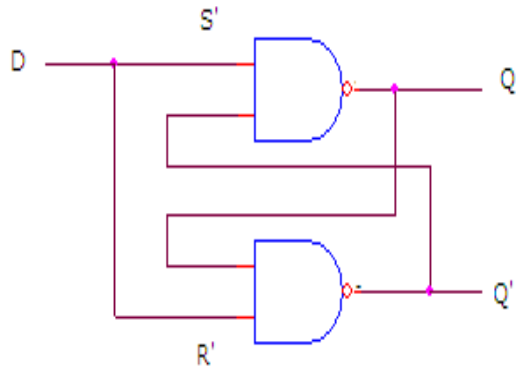
K. CMOS S'R' NAND latch realization:



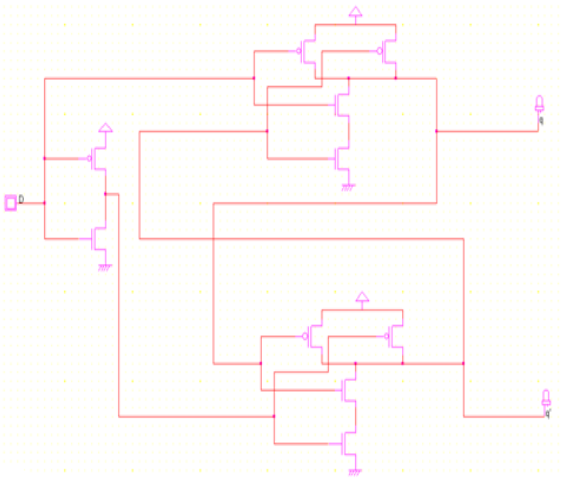
L. Transient analysis of CMOS S'R' NAND latch:



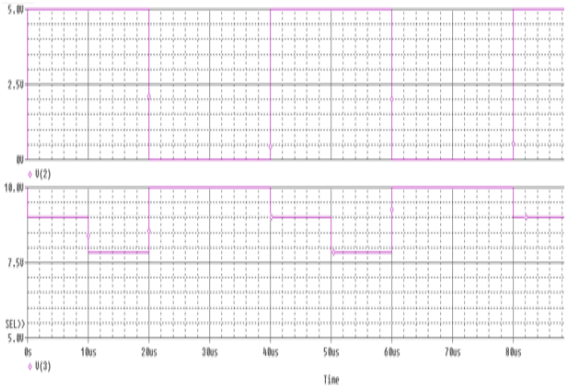
M. Logic Diagram of D-Latch



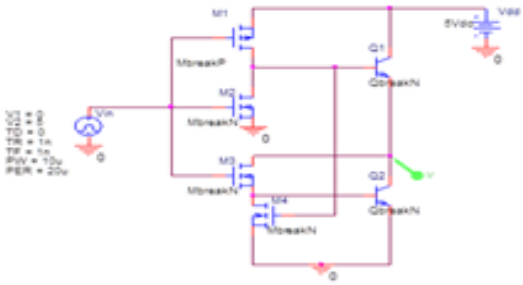
N. CMOS D latch realization



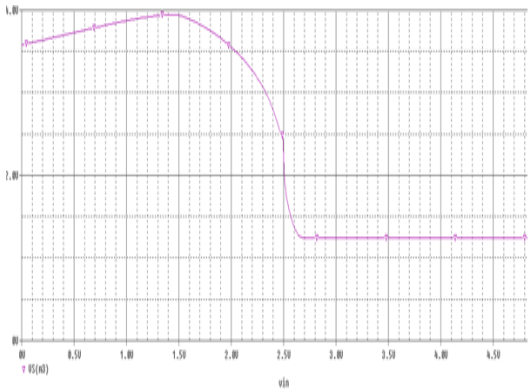
O. Transient analysis of CMOS D latch:



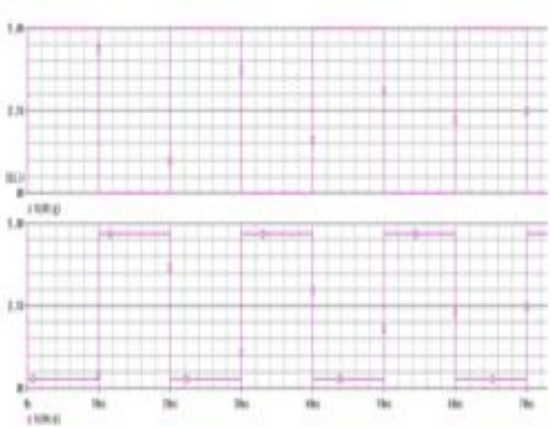
P. BiCMOS inverter realization:



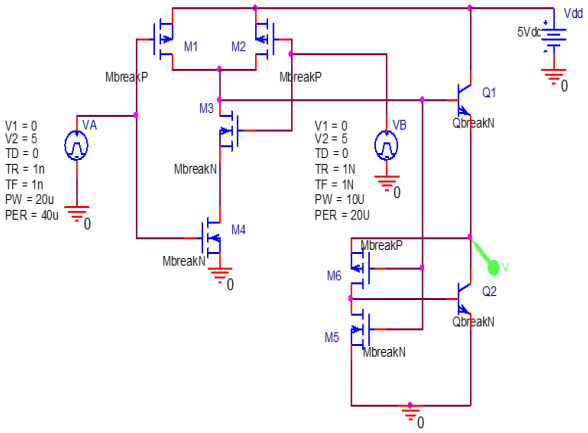
Q. VTC curve of BiCMOS inverter:



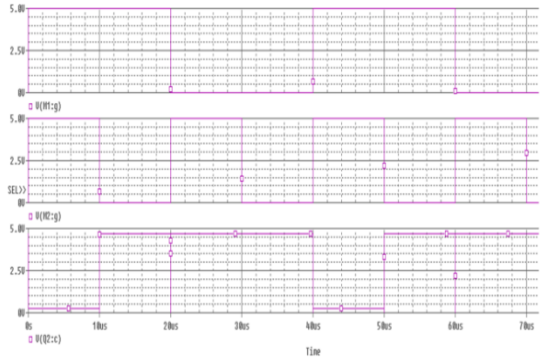
R. Transient analysis of BiCMOS inverter:



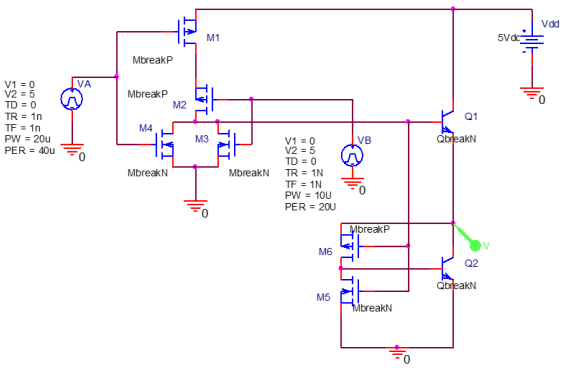
S. BiCMOS NAND gate realization:



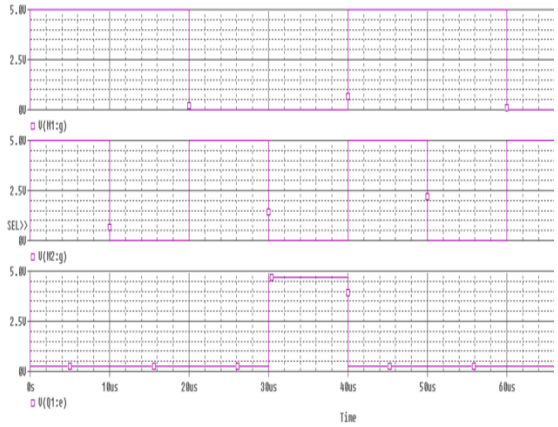
T. Transient analysis of BiCMOS inverter:



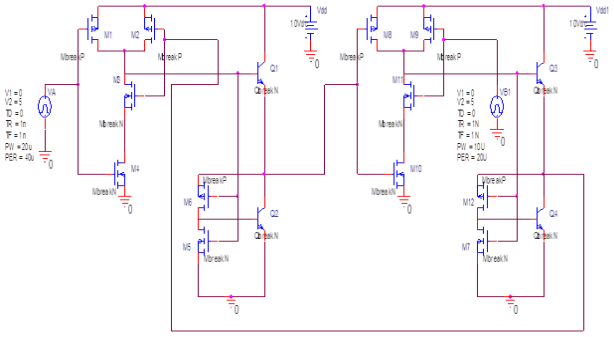
U. BiCMOS NOR gate realization:



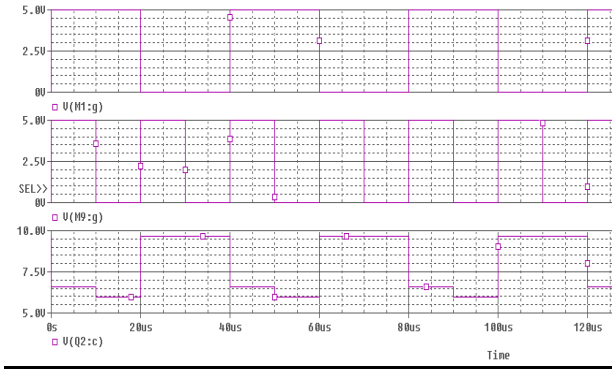
V. Transient analysis of BiCMOS NOR gate:



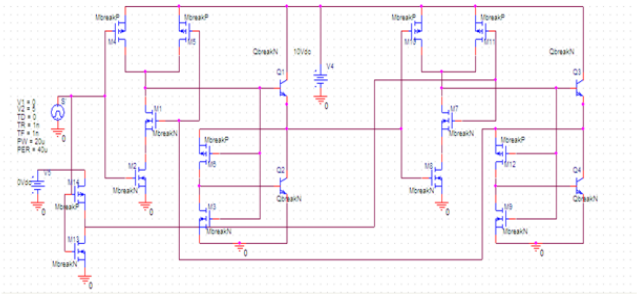
W. BiCMOS S'R' NAND latch realization:



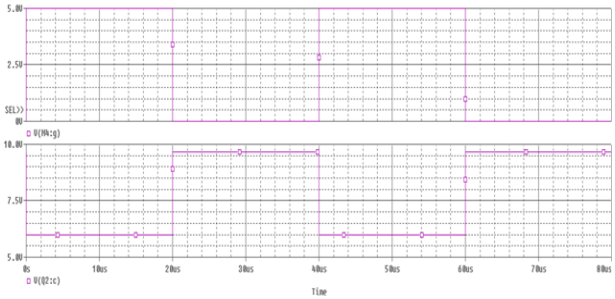
X. Transient analysis of BiCMOS S'R' NAND latch:



Y. BiCMOS D latch realization:



Z. Transient analysis of BiCMOS D latch:



COMPARATIVE STUDY BETWEEN CMOS LOGIC AND BiCMOS LOGIC

Table 4: Comparison of Logic Circuit results between CMOS& BiCMOS logic.

Sl No	Logic gate	CMOS		BiCMOS	
		Logic 0 (Volts)	Logic 1 (Volts)	Logic 0 (Volts)	Logic1 (Volts)
1	NOT	0	5	0.25	4.75
2	NAND	0	5	0.25	4.75
3	NOR	0	5	0.25	4.75
4	S'R' latch	7.7	10	6	10
5	D latch	7.7	10	6	10

Table 5: Comparison of VTC Curve between CMOS and BiCMOS Inverter

NM (low) = VIL – VOL

NM (high) = VOH – VIH

VTC Critical Voltages	CMOS Inverter (Volts)	BiCMOS Inverter (Volts)	NOISE MARGIN	
			CMOS	BiCMOS
VIL	2.2	2	0.7	0.5
VOL	1.5	1.5		
VIH	2.6	2.6	1.4	1.2
VOH	4	3.8		

Disadvantages of BiCMOS Logic

- BiCMOS is not currently as commercially viable for microprocessors, as with exclusively BJT or CMOS fabrication
- In the area of high performance logic, BiCMOS may not offer the (relatively) low power consumption of CMOS alone, due to the potential for higher standby leakage current.
- An inherent difficulty arises from the fact that optimizing both the BJT and MOS components of the process is impossible without adding many extra fabrication steps and consequently increasing the process cost.
- The Logic levels are not ideal i.e. Logic -0 corresponds to 0.25 Volts & Logic-1 corresponds to 4.75 Volts.

III. Future Scope

As compared to CMOS logic, BiCMOS circuits are more complicated in terms of design. But, we use BiCMOS logic due to the factors- high switching speed, high gain, high noise margin, & high packing density.

Since we are able to implement the basic logic circuits by using BiCMOS, we can also implement the further sequential memory elements like Flip Flops & further Counters, registers, memory devices like RAM, ROM, ALU, etc.

IV. Conclusion

This paper decribes how a CMOS & a BiCMOS can be used to realize basic memory elements like latch. But the limitations of latch is that it is asynchronous in nature, i.e. whenever the inputs are changed the outputs will be changed accordingly, & we will not gate stable outputs. This problem can be overcome by introducing en external clock signal which will control the circuits further to give stable outputs. So, this work can be extended by including an clock signal to design a Flip Flop by using our proposed memory elements. Again it can be noted that our proposed CMOS & BiCMOS S"R" latch are not giving the ideal output logic levels. Modifications can be done in this limitations also.

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